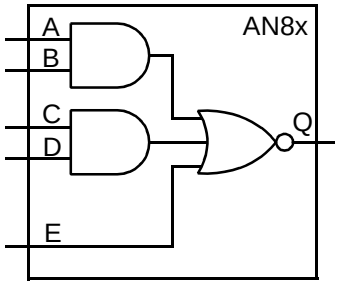
Description

AN8x is a family of AND-NOR circuits consisting of two 2-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	X	X	X	L
X	X	H	H	X	L
X	X	X	X	H	L
All other combinations					H

HDL Syntax

Verilog ..... AN8x *inst_name* (Q, A, B, C, D, E);

VHDL..... *inst_name*: AN8x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	AN82	AN84	AN86
A	1.0	1.0	2.1
B	1.0	1.0	2.1
C	1.0	1.0	2.1
D	1.0	1.0	2.1
E	1.0	1.0	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
AN82	5.0	TBD	9.7
AN84	5.0	TBD	10.4
AN86	11.0	TBD	21.5

a. See page 2-15 for power equation.

Core Logic

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

AN82	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.47 0.42	0.57 0.54	0.69 0.67	0.84 0.82	0.95 0.93
AN84	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.49 0.43	0.62 0.57	0.73 0.68	0.84 0.78	0.96 0.89
AN86	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.45 0.40	0.58 0.54	0.70 0.65	0.80 0.75	0.90 0.84

Delay will vary with input conditions. See page 2-17 for interconnect estimates.