AN884

Driving Capacitive Loads With Op Amps

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INTRODUCTION

Overview

Operational amplifiers (op amps) that drive large capacitive loads may produce undesired results. This application note discusses these potential problems. It also offers simple, practical solutions to each of these problems.

The circuit descriptions and mathematics are kept to a minimum, with emphasis on understanding rather than completeness. Simple models of op amp behavior help achieve these goals. Simple equations are included to help connect circuit design to overall circuit behavior.

Simple examples illustrate the concepts discussed. They give concrete results that can be used to better understand the theory. They are also practical to help develop a feel for real world designs.

Purpose

This application note is for circuit designers using op amps that drive capacitive loads. It assumes only a basic understanding of circuit analysis.

This application note has the goal of helping circuit designers quickly and effectively resolve capacitive loading issues in op amp circuits. It focuses on building a fundamental understanding of why problems occur, and how to resolve these problems.

LINEAR RESPONSE

Capacitive loads affect an op amp's linear response. They change the transfer function, which affects AC response and step response. If the capacitance is large enough, it becomes necessary to compensate the op amp circuit to keep it stable, and to avoid AC response peaking and step response overshoot and ringing.

An op amp's linear response is also critical in understanding how it interacts with sampling capacitors. These sampling capacitors present a non-linear, reactive load to an op amp. For instance, many A/D converters (e.g., low frequency SAR and Delta-Sigma) have sampling capacitors at their inputs.

Simplified Op Amp AC Model

In order to understand how capacitive loads affect op amps, we must look at the op amp's output impedance and bandwidth. The feedback network modifies the op amp's behavior; its effects are included in an equivalent circuit model.

OP AMP MODEL

Figure 1 shows a simplified AC model of a voltage feedback op amp. The open-loop gain is represented by the dependent source with gain $A_{OL}(s)$, where $s = j\omega = j2\pi f$. The output stage is represented by the resistor R_O (open-loop output resistance).

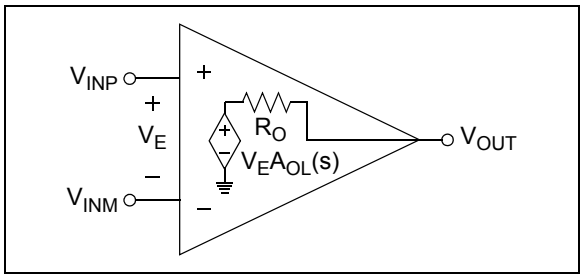

FIGURE 1: *Op Amp AC Model.*

We will include gain bandwidth product (f_{GBP}), the open-loop gain's "second pole" (f_{2P}) in our open-loop gain ($A_{OL}(s)$) model. Low frequency effects are left out for simplicity. f_{2P} models the open-loop gain's reduced phase (< -90°) at high frequencies due to internal parasitics (see **Section B.1 "Estimating f_{2P}"** for more information).

EQUATION 1:

$$A_{OL}(s) \approx \frac{\omega_{GBP}}{s(1 + s/\omega_{2P})}$$

CIRCUIT MODEL

Figure 2 shows the op amp in a non-inverting gain, and Figure 3 in an inverting gain. These circuits cover the majority of applications.

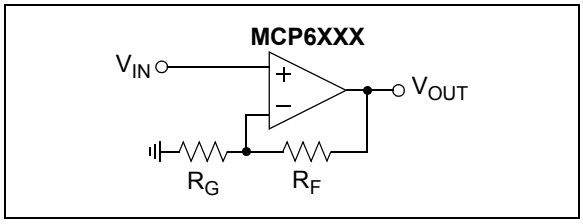

FIGURE 2: *Non-inverting Gain Circuit.*

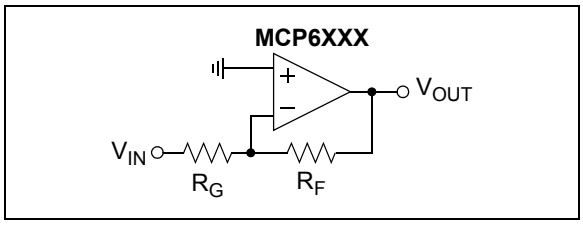

FIGURE 3: *Inverting Gain Circuit.*

These circuits have different DC gains (K) and a DC noise gain (G_N). G_N can be defined to be the gain from the input pins to the output set by the feedback network. It is also useful in describing the stability of op amp circuits. These gains are:

EQUATION 2:

$$K = 1 + R_F/R_G \text{ , non-inverting}$$
$$K = -R_F/R_G \text{ , inverting}$$
$$G_N = 1 + R_F/R_G$$

Note: Some applications do not have constant G_N due to reactive elements (e.g., capacitors). More sophisticated design techniques, or simulations, are required in that case.

The op amp feedback loop (R_F and R_G) causes its closed-loop behavior to be different from its open-loop behavior. Gain bandwidth product (f_{GBP}) and open-loop output impedance (R_O) are modified by G_N to give closed-loop bandwidth (f_{3dBA}) and output impedance (Z_{OUT}). We can analyze the circuits in Figure 1, Figure 2 and Figure 3 to give:

EQUATION 3:

$$f_{3dBA} \approx f_{GBP}/G_N$$
$$Z_{OUT} = \frac{R_O}{1 + A_{OL}(s)/G_N}$$

Figure 4 shows Z_{OUT}'s behavior. At low frequencies, it is constant because the open-loop gain is constant. As the open-loop gain decreases with frequency, Z_{OUT} increases. Past f_{3dBA}, the feedback loop has no more effect, and Z_{OUT} stays at R_O. The peaking at G_N = +1 is caused by the reduced phase margin due to f_{2P}.

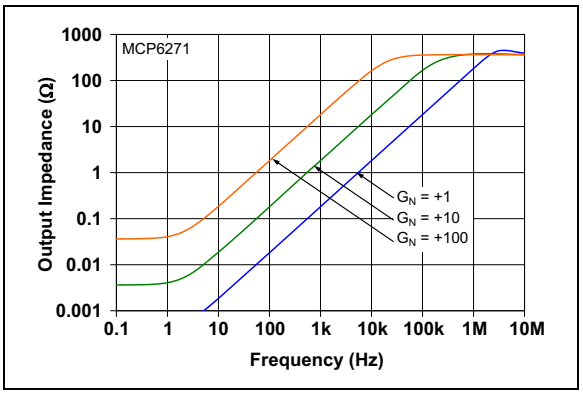

FIGURE 4: *MCP6271's Closed-Loop Output Impedance vs. Frequency.*

Figure 5 shows a simple AC model that approximates this behavior. The amplifier models the no load gain and bandwidth, while the inductor and resistor model the output impedance vs. frequency.

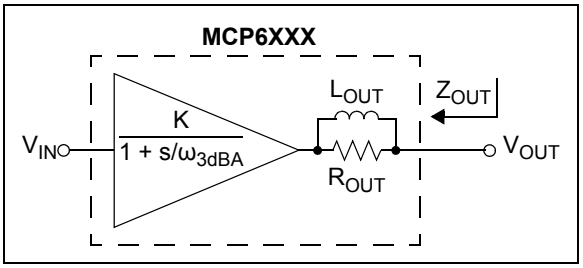

FIGURE 5: *Simplified Op Amp AC Model.*

R_{OUT} is larger than R_O because it includes f_{2P}'s phase shift effects, which are especially noticeable at low gain (G_N). The equations for L_{OUT} and R_{OUT} are:

EQUATION 4:

$$L_{OUT} = R_O/(2\pi f_{3dBA})$$
$$R_{OUT} \approx \frac{R_O}{max(1 - f_{3dBA}/f_{2P}\ ,\ 1/2)}$$

Uncompensated AC Behavior

This section shows the effect load capacitance has on op amp gain circuits. These results help distinguish between circuit that need compensation and those that do not.

THEORY

Figure 6 shows a non-inverting gain circuit with an uncompensated capacitive load. The inverting gain circuit is a simple modification of this circuit. For small capacitive loads and high noise gains (typically C_L/G_N < 100 pF), this circuit works quite well.

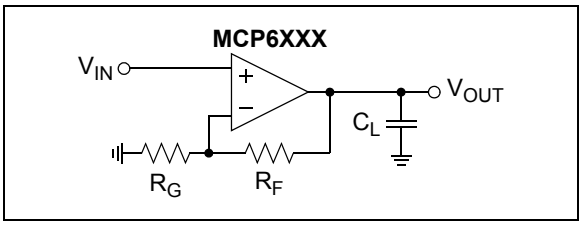

FIGURE 6: *Uncompensated Capacitive Load.*

The feedback network (R_F and R_G) also presents a load to the op amp output. This load (R_{FL}) depends on whether the gain is non-inverting or inverting:

EQUATION 5:

$$R_{FL} = R_F + R_G \text{ , non-inverting gain}$$
$$R_{FL} = R_F \text{ , inverting gain}$$

Replacing the op amp in Figure 6 with the simplified op amp AC model gives an LC resonant circuit (L_{OUT} and C_L). When C_L becomes large enough, $R_{OUT}||R_{FL}$ does a poor job of dampening the LC resonance, which causes peaking and step response overshoot. This happens because the feedback loop's phase margin is reduced by both f_{2P} and C_L.

A simplified transfer function is:

EQUATION 6:

$$\frac{V_{OUT}}{V_{IN}} \approx K \Big/ \left(1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}\right)$$

Where:

$$G_N = 1 + R_F / R_G$$
$$K = G_N \text{ , non-inverting}$$
$$K = 1 - G_N \text{ , inverting}$$
$$\omega_P = 2\pi f_P = 1 / \sqrt{L_{OUT} C_L}$$
$$Q_P = (R_{OUT} || R_{FL}) \cdot \sqrt{C_L / L_{OUT}}$$

We can now use the equations in **Appendix A: "2nd Order System Response Model"** to estimate the overall bandwidth (f_{3dB}), frequency response peaking (H_{PK}/G_N), and step response overshoot (x_{max}). Note that f_{3dB} is not the same as the op amp's no load, -3dB bandwidth (f_{3dBA}).

MCP6271 EXAMPLE

The equations above were used to generate the curves in Figure 7 and Figure 8 for Microchip's MCP2671 op amp. The parameters used are from **TABLE B-1: "Estimates of Typical Microchip Op Amp Parameters"**.

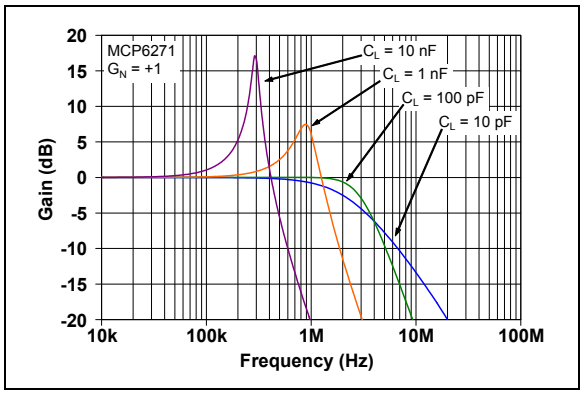

FIGURE 7: *Estimate of MCP6271's AC Response with G_N = +1.*

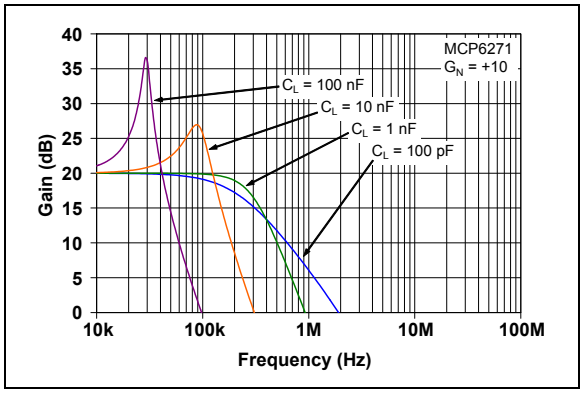

FIGURE 8: *Estimate of MCP6271's AC Response with G_N = +10.*

The peaking (H_{PK}/G_N) should be near 0 dB for the best overall performance. Keeping the peaking below 3 dB usually gives enough design margin for changes in op amp, resistor, and capacitor parameters over temperature and process. However, the performance is degraded.

For this example, our formulas give the estimated results shown in Table 1. As C_L increases, and gain decreases, there is more peaking.

TABLE 1: RESPONSE ESTIMATES

Circuit		Response				
G_N (V/V)	C_L (F)	f_P (Hz)	Q_P ( )	f_{3dB} (Hz)	H_{PK}/K (dB)	x_{max} (%)
1.0	10p	9.3M	0.23	2.3M	0.0	0
	100p	2.9M	0.73	3.1M	0.0	5
	1n	0.93M	2.3	1.4M	7.5	50
	10n	0.29M	7.3	0.46M	17.3	81
10.0	100p	930k	0.22	211k	0.0	0
	1n	294k	0.69	285k	0.0	4
	10n	93k	2.2	139k	7.0	48
	100n	29k	6.9	46k	16.7	80

Series Resistor Compensation

A series resistor (R_{ISO}) is inserted to reduce resonant peaking. It draws no extra DC current and does not affect DC gain accuracy when there is no load resistance. This compensation method only costs one resistor.

THEORY

Figure 9 shows the series resistor R_{ISO} loading the resonant circuit at the op amp's output, reducing frequency response peaking. The inverting gain circuit is very similar.

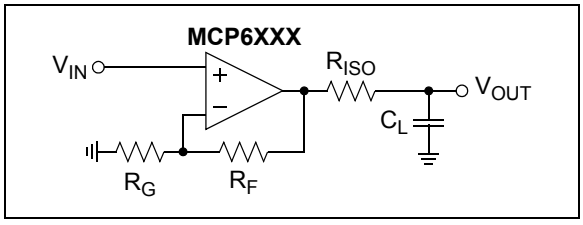

FIGURE 9: *Compensated Capacitive Load.*

The transfer function now includes R_{ISO}:

EQUATION 7:

$$\frac{V_{OUT}}{V_{IN}} \approx K \diagup \left(1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}\right)$$

Where:

$$G_N = 1 + R_F \diagup R_G$$

$$K = G_N, \quad \text{non-inverting}$$

$$K = 1 - G_N, \quad \text{inverting}$$

$$\omega_P = 2\pi f_P = 1 \diagup \sqrt{L_{OUT} C_L \left(1 + \frac{R_{ISO}}{R_{OUT} \| R_{FL}}\right)}$$

$$Q_P = 1 \diagup \left(\omega_P \left(\frac{L_{OUT}}{R_{OUT} \| R_{FL}} + R_{ISO} C_L\right)\right)$$

We can now find a reasonable R_{ISO} value. When $Q_P = 1/\sqrt{2}$, the response has the highest possible bandwidth without peaking, and the equations are in their simplest form:

EQUATION 8:

$$R_{ISO} = 0, \quad C_L \le C_X$$

$$R_{ISO} = (R_{OUT} \| R_{FL}) \cdot \frac{2C_X}{C_L} \cdot \sqrt{\frac{C_L}{C_X} - 1}, \quad C_L > C_X$$

Where:

$$Q_P = 1 \diagup \sqrt{2} \approx 0.707$$

$$C_X = \frac{L_{OUT}}{2(R_{OUT} \| R_{FL})^2}$$

MCP6271 EXAMPLE

These equations were used to compensate the MCP6271 circuit in Figure 9. The results are shown in Figure 10 and Figure 11 (compare to Figure 7 and Figure 8).

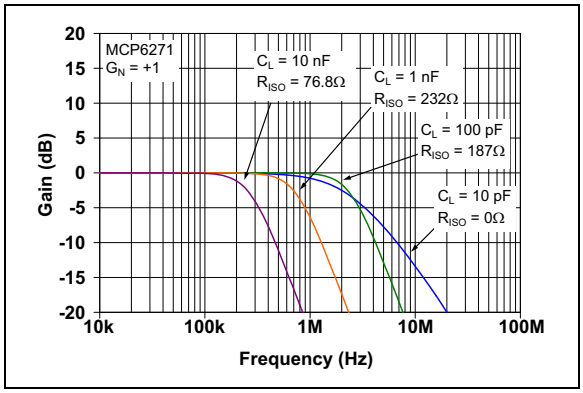

FIGURE 10: *Estimate of MCP6271's Compensated AC Response with G = +1.*

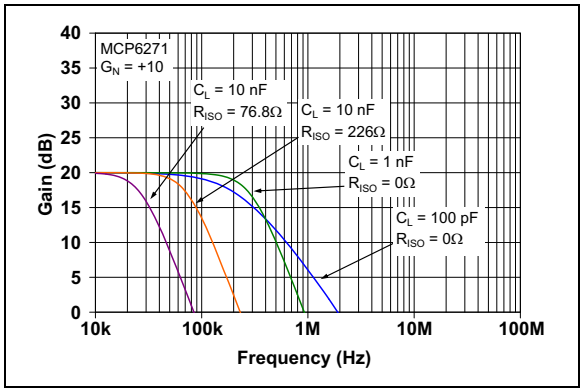

FIGURE 11: *Estimate of MCP6271's Compensated AC Response with G = +10.*

Our formulas give the estimated results shown in Table 2. R_{ISO} has limited the gain peaking. These results are much better than before (see Table 1).

TABLE 2: RESPONSE ESTIMATES (NOTE 1)

Circuit			Response			
G_N (V/V)	C_L (F)	R_{ISO} (Ω)	f_P (Hz)	Q_P ( )	f_{3dB} (Hz)	x_{max} (%)
1.0	10p	0	9.3M	0.23	2.3M	0
	100p	187	2.4M	0.71	2.4M	4
	1n	232	0.74M	0.71	0.74M	4
	10n	76.8	0.27M	0.71	0.27M	4
10.0	100p	0	930k	0.22	211k	0
	1n	0	294k	0.69	285k	4
	10n	226	73k	0.71	73k	4
	100n	76.8	27k	0.71	27k	4

Note 1: H_{PK}/K = 0 dB for all of these compensated examples.

Figure 12 shows the estimated R_{ISO} values for the MCP6271 (see Equation 8). The x-axis is normalized load capacitance (C_L/G_N) for ease of interpretation.

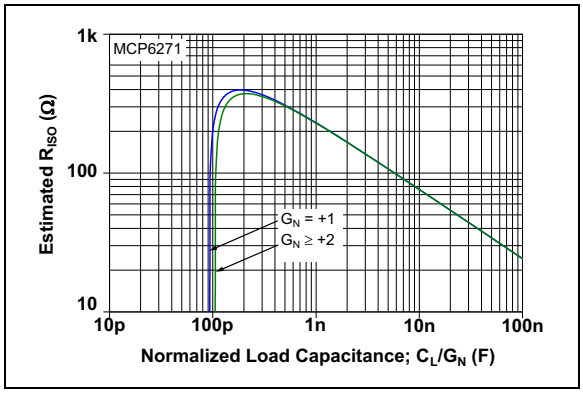

FIGURE 12: *Estimated R_{ISO} for the MCP6271.*

Shunt Resistor Compensation

A shunt resistor (R_{SH}) is placed on the output to reduce resonant peaking. A series capacitor (C_{SH}) can be included to prevent R_{SH} from drawing extra DC current, which reduces DC gain accuracy. The cost of this implementation is one resistor and (usually) one capacitor. R_{SH} and C_{SH} together can be considered an R-C snubber circuit.

THEORY

Figure 9 shows the shunt resistor R_{SH} loading the resonant circuit at the op amp's output, reducing frequency response peaking. C_{SH} blocks DC, which overcomes this approach's limitations. The inverting gain circuit is very similar.

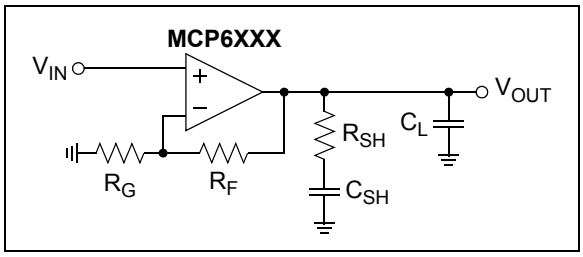

FIGURE 13: *Compensated Capacitive Load.*

The transfer function with R_{SH} only (C_{SH} is shorted) is:

EQUATION 9:

$$\frac{V_{OUT}}{V_{IN}} \approx K \diagup \left(1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}\right)$$

Where:

$$C_{SH} = \text{short}$$
$$G_N = 1 + R_F \diagup R_G$$
$$K = G_N, \quad \text{non-inverting}$$
$$K = 1 - G_N, \quad \text{inverting}$$
$$\omega_P = 2\pi f_P = 1 \diagup \sqrt{L_{OUT} C_L}$$
$$Q_P = (R_{OUT} \| R_{FL} \| R_{SH}) \cdot \sqrt{C_L \diagup L_{OUT}}$$

$Q_P = 1/\sqrt{2}$ gives a reasonable R_{SH} value:

EQUATION 10:

$$G_{XX} = \sqrt{\frac{2C_L}{L_{OUT}}} - \frac{1}{R_{OUT}} - \frac{1}{R_{FL}}$$
$$R_{SH} = \text{open}, \quad G_{XX} \le 0$$
$$R_{SH} = 1 \diagup G_{XX}, \quad G_{XX} > 0$$

Where:

$$C_{SH} = \text{short}$$
$$Q_P = 1 \diagup \sqrt{2} \approx 0.707$$

To keep the design simple, calculate C_{SH} so that it has minimal interaction with the resonant circuit:

EQUATION 11:

$$C_{SH} = \text{open}, \quad R_{SH} = \text{open}$$
$$C_{SH} \ge \frac{10}{\omega_P R_{SH}}, \quad R_{SH} < \infty$$

MCP6271 EXAMPLE

These equations were used to compensate the MCP6271 circuits in Figure 12. The results are shown in Figure 14 and Figure 15 (compare to Figure 7 and Figure 8); C_{SH} is not shown for convenience.

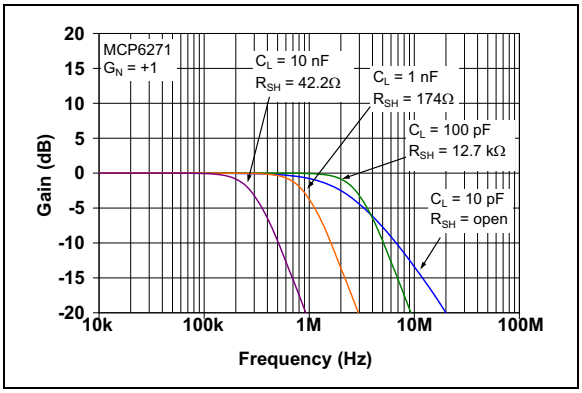

FIGURE 14: *Estimate of MCP6271's Compensated AC Response with G = +1.*

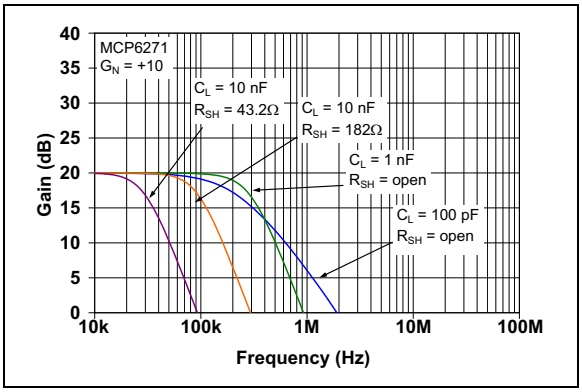

FIGURE 15: *Estimate of MCP6271's Compensated AC Response with G = +10.*

Our formulas give the estimated results in Table 3; they include C_{SH} values at each design point. As can be seen, R_{SH} has limited the gain peaking. These results are much better than before (see Table 1).

TABLE 3: RESPONSE ESTIMATES (NOTE 1)

Circuit				Response			
G_N (V/V)	C_L (F)	R_{SH} (Ω)	C_{SH} (F)	f_P (Hz)	Q_P ( )	f_{3dB} (Hz)	x_{max} (%)
1.0	10p	open	open	9.3M	0.23	2.3M	0
	100p	12.7k	47p	2.9M	0.71	2.9M	4
	1n	174	10n	0.93M	0.71	0.93M	4
	10n	42.2	120n	0.29M	0.71	0.29M	4
10.0	100p	open	open	930k	0.22	211k	0
	1n	open	open	294k	0.69	285k	4
	10n	182	100n	93k	0.71	93k	4
	100n	43.2	1.2µ	29k	0.71	29k	4

Note 1: H_{PK}/K = 0 dB for all of these compensated examples.

The R_{SH} and C_{SH} values for the MCP6271, estimated by Equation 10, are shown in Figure 16. It shows normalized load capacitance (C_L/G_N) and normalized shunt capacitance (C_{SN}/G_N) for convenience.

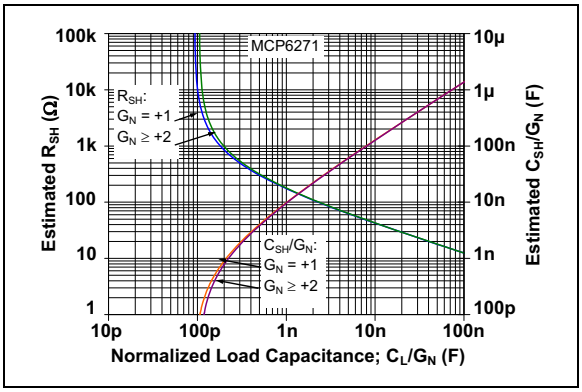

FIGURE 16: *Estimated R_{SH} for the MCP6271.*

DRIVING A/D CONVERTERS

Microchip's SAR and Delta-Sigma A/D converters (ADCs) use sampling capacitors at their inputs. Near DC, these switched capacitors interact with other internal capacitors as if they were large resistors. At high frequencies, their behavior is more complicated.

The ADCs' input impedance, as seen by other components in a circuit, is non-linear; it has Fourier components to very high frequencies.

This section shows different ways to analyze this phenomenon. It also gives simple design fixes.

Incorrect DC Analysis

An A/D converter input is usually described (modeled) as an input resistance. Unlike resistors, switched capacitors do not react to low frequency (i.e., DC) impedances; they react to high frequency impedances seen at the input.

Note: Switched capacitors do *not* present a DC resistance to the circuit driving them.

An op amp that drives an ADC with a sampling capacitor input may not behave as expected. The op amp's low frequency behavior does not determine circuit behavior; not even for "DC" applications.

EXAMPLE

A typical example of an incorrect circuit analysis is shown here. A MCP6031 op amp, at unity gain, drives the MCP3421 Delta-Sigma ADC; see Figure 17. The MCP3421 has a typical data rate between 3.75 SPS (18 bits) and 240 SPS (12 bits); it appears to operate at DC. For this reason, the MCP6031 seems like a good choice as a driver; it has low quiescent current (I_Q = 0.9 µA), low offset voltage ($V_{OS} \leq \pm 150$ µV), and low DC output resistance (see Table B-1):

EQUATION 12:

$$R_{ODC} = G_N(R_O \diagup A_{OL}) = 0.13\Omega$$

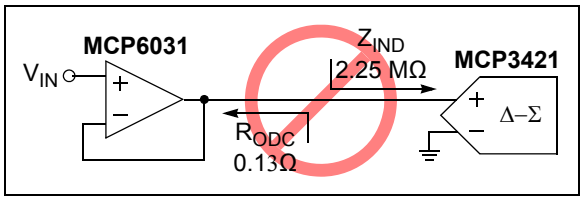

FIGURE 17: *Driving the MCP3421; Incorrect Model of Interaction.*

It would appear that the gain error caused by the interaction between R_{ODC} and Z_{IND} is about -0.06 ppm. *Reality is very different from this simple model.*

AC Analysis

The simplest useable model for the interaction between the op amp and ADC uses the op amp's gain and closed-loop output impedance (*at the ADC's sampling rate*), and the ADC's equivalent input resistance. We will ignore other harmonics to simplify the analysis.

FIRST EXAMPLE

The MCP3421's input sampling capacitor switches at a much higher rate than the data rate (by the over-sampling ratio). This sampling rate (f_{SMP}) is about 16 kSPS when in the 18-bit mode. This is higher than the MCP6031's bandwidth (10 kHz). For this particular circuit, we can use the MCP6031's open-loop output resistance (R_O) to estimate the DC gain accuracy; Z_O is constant at f_{SMP} and above. Because Z_O is constant, there is no need for more sophisticated analyses. Figure 18 shows this model of how the op amp and ADC interact.

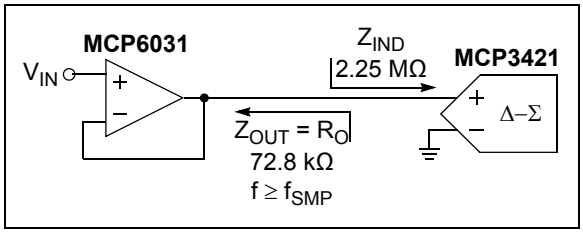

FIGURE 18: *Driving the MCP3421; Improved Model of Interaction.*

Thus, the DC gain error is about -3%. This size of error is unacceptable; it is about 900 times larger than the MCP3421's maximum specified INL. Bench measurements (-5%) are close to this result.

SECOND EXAMPLE – FASTER OP AMP

A faster op amp is better in two ways. The equivalent output inductance is smaller because the open-loop output resistance is smaller and the gain bandwidth product is higher. If it is fast enough to be inductive at the ADC's sampling rate, its contribution to the error budget is greatly reduced.

Note:	A faster op amp can avoid many of the problems listed earlier.

Replacing the op amp with a MCP606 gives (see Figure 19 and Table B-1):

$R_O = 4.20\ k\Omega$
$f_{GBP} = 155\ kHz$
$f_{2P} = 673\ kHz$
$G_N = K = 1\ V/V$
$f_{3dBA} \approx 155\ kHz$
$L_{OUT} \approx 4.31\ mH$
$R_{OUT} \approx 5.46\ k\Omega$

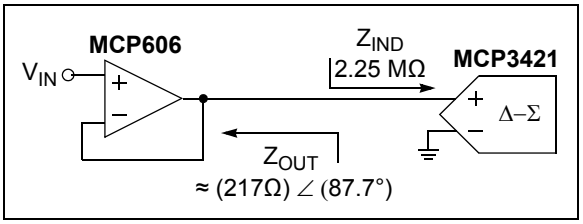

FIGURE 19: *Driving the MCP3421; using a faster op amp.*

An AC analysis of this circuit is quick and easy to do. At the MCP3421 sample rate (f_{SMP}) of 16 kSPS, the MCP606's output impedance is approximately:

EQUATION 13:

$$Z_{OUT} = R_{OUT} \| (j2\pi f_{SMP} L_{OUT})$$
$$Z_{OUT} = 1 \angle \left(\frac{1}{(5.46\ k\Omega)} + \frac{1}{j(217\Omega)} \right)$$
$$Z_{OUT} = (217\Omega) \angle 87.7^\circ$$

The gain error can be roughly approximated by a ratio of complex impedances. The fact that they are almost 90° out of phase greatly reduces the error:

EQUATION 14:

$$\frac{Z_{IND}}{Z_{IND} + Z_{OUT}} = \frac{(2.25\ M\Omega)}{(2.25\ M\Omega) + (8.7\ \Omega) + j(217\ \Omega)}$$
$$\frac{Z_{IND}}{Z_{IND} + Z_{OUT}} = (1 - 3.9\ ppm) \angle -0.0055^\circ$$

Both the DC gain error and the phase shift (time delay) are negligible. The cost for these improvements is using an op amp with a V_{OS} of ±250 µV (was ±150 µV), and an I_Q of 18.7 µA (from 0.9 µA).

Step Response Analysis

A step response analysis of this circuit is more accurate and informative than an AC analysis. To see how this circuit behaves when it switches, place a step function at the input and see how quickly the output settles to the desired accuracy. The settling time must be short enough to allow the ADC to settle accurately.

FIRST EXAMPLE

Figure 20 models this circuit in the time domain for the MCP6031 op amp.

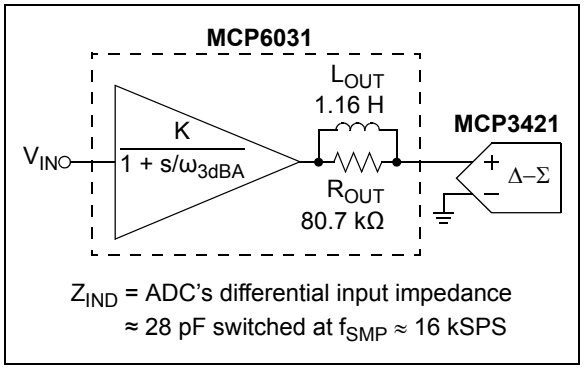

FIGURE 20: *Op Amp and ADC Models for Time Domain Analysis.*

We now estimate the step response settling time using 28 pF as the load capacitance (see Equation 9, Equation A-5, and Equation A-15):

$$C_L \approx 1 / (f_{SMP} Z_{IND}) \approx 28\ pF$$
$$f_P \approx 27.9\ kHz$$
$$Q_P \approx 0.396$$
$$f_{3dB} \approx 13.0\ kHz$$
$$t_{set} \approx 30\ \mu s, \quad x_{set} = 10\%$$
$$t_{set} \approx 56\ \mu s, \quad x_{set} = 1\%$$
$$t_{set} \approx 83\ \mu s, \quad x_{set} = 0.1\%$$
$$t_{set} \approx 110\ \mu s, \quad x_{set} = 0.01\%$$

Since the f_{SMP} is about 16 kSPS, the sample period (T_{SMP}) is about 62.5 µs. Notice that each decade of increase in x_{set} gives an increase of 27 µs in t_{set}, so a 5% error would happen at:

$$t_{set} \approx 38\ \mu s, \quad x_{set} = 5\%$$

This means that about 61% of T_{SMP} may have been used for the ADC's settling when the bench results were measured. The MCP6031 op amp is too slow for this application, unless we compensate it.

SECOND EXAMPLE

Figure 21 models this circuit in the time domain for the MCP606 Op Amp.

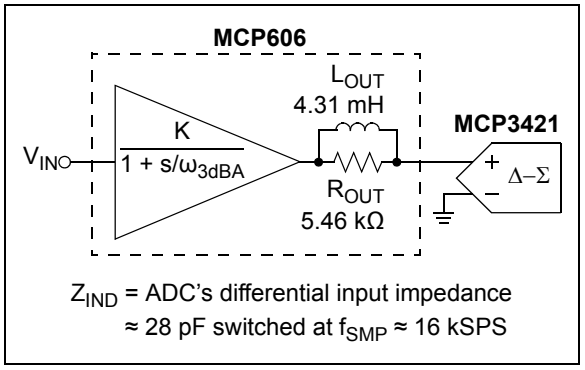

FIGURE 21: *Op Amp and ADC Models for Time Domain Analysis.*

We now estimate the step response settling time using 28 pF as the load capacitance (see Equation 9, Equation A-5, and Equation A-15):

$$C_L \approx 1 / (f_{SMP} Z_{IND}) \approx 28\ pF$$
$$f_P \approx 458\ kHz$$
$$Q_P \approx 0.440$$
$$f_{3dB} \approx 246\ kHz$$
$$t_{set} \approx 3.0\ \mu s, \quad x_{set} = 10\%$$
$$t_{set} \approx 5.5\ \mu s, \quad x_{set} = 1\%$$
$$t_{set} \approx 8.0\ \mu s, \quad x_{set} = 0.1\%$$
$$t_{set} \approx 10.5\ \mu s, \quad x_{set} = 0.01\%$$

From the first example, we know that T_{SMP} is about 38 µs. Each decade of x_{set} gives an increase of 1.5 µs in t_{set}, so x_{set} at 38 µs should be roughly 18.3 decades below 0.01%; the settling error should be negligible. It is also encouraging that the pole quality factor (Q_P) is low; the MCP606 should be a good fit for this application without any compensation.

Improved Design Using R-C Snubber

A R_{SH} and C_{SH} snubber reduces the output impedance of an op amp at higher frequencies, which reduces the resistor gain error at the ADC's sampling rate. The snubber can be designed to maintain feedback stability and greatly reduce output resistance at the ADC's sampling rate (and its harmonics). The cost for this improvement is low. Best of all, we avoided using an op amp with higher supply current.

EXAMPLE

The R_{ISO} and C_L values for the MCP6031, estimated by Equation 8, are shown in Figure 22. It shows normalized load capacitance (C_L/G_N) for convenience.

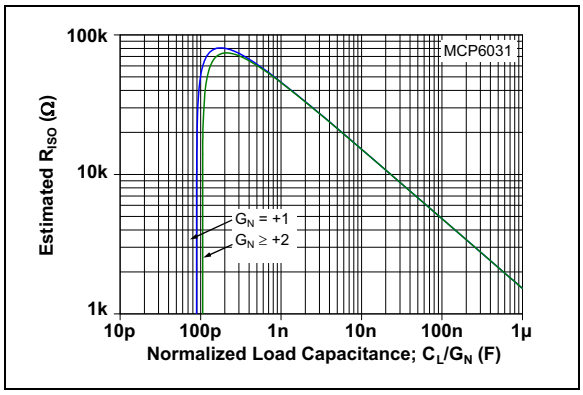

FIGURE 22: *Estimated R_{ISO} for the MCP6031.*

The capacitive load presented by the ADC in Figure 23 is small (28 pF); we don't need to stabilize the op amp for this load. This circuit, however, uses a snubber (R_{SH} and C_{SH}) to reduce the output resistance at the switching frequency, which improves the step response (reduces the Q of the resonant circuit). Figure 22 helps us select R_{SH} and C_{SH} values that will keep the op amp stable (C_{SH} acts as a capacitive load), while selecting a reasonable value of R_{SH}:

- R_{SH} ("R_{ISO}") was selected to be 1 kΩ in order to reduce the resistor gain error to about -0.044%
- C_{SH} ("C_L") was selected as the largest corresponding capacitance (2.2 µF) in Figure 22

The pole set by R_{SH} and C_{SH} (72 Hz) is much smaller than the ADC's sampling rate (16 kSPS). Thus, the ADC's input sees a constant impedance at the sample rate (and its harmonics).

Figure 23 includes a resistor to balance the impedance at the ADC's inputs (R_{BAL}) at the sampling frequency; it may not be needed in all designs.

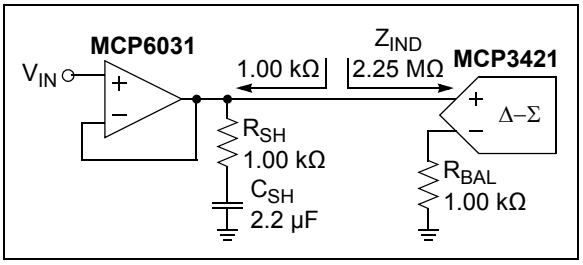

FIGURE 23: *Driving the MCP3421; using an R-C Snubber.*

We now investigate the step response settling time with a load capacitance of 28 pF; C_{SH} is a short circuit (see Equation 9, Equation A-5, and Equation A-16):

$$C_L = 2.2\ \mu F$$
$$f_P \approx 99.6\ Hz$$
$$Q_P \approx 1.36$$
$$f_{3dB} \approx 140\ Hz$$
$$t_{set} \approx 10\ \mu s, \quad x_{set} = 10\%$$
$$t_{set} \approx 20\ \mu s, \quad x_{set} = 1\%$$
$$t_{set} \approx 30\ \mu s, \quad x_{set} = 0.1\%$$
$$t_{set} \approx 40\ \mu s, \quad x_{set} = 0.01\%$$

Since the amplifier is now much slower than the ADC's sampling rate, and the snubber looks like a constant resistance at the sample rate, the amplifier's output impedance dominates the performance. The DC error should be about -0.044% as we expected.

Since we have a double pole, any crosstalk at 16 kHz will be rejected by 88 dB.

C_{SH} will need to be larger when the MCP3421 is run at lower precision (lower sampling rate, but higher data rates). See **Appendix C: "MCP3421 Sampling Rates"** for more information.

NON-LINEAR RESPONSE

Capacitive loads can cause a non-linear response when they demand more current than the op amp's output can produce. This non-linearity imposes a limit on the output voltage slew rate (not the op amp's internal slew rate specified in its data sheet).

Physical Cause Of Slew Rate Limitation

The op amp produces an output current (I_{OUT}) that goes into a capacitive load (C_L); see Figure 24. Since I_{OUT} cannot exceed the op amp's output short circuit current (I_{SC}), and the voltage on C_L (V_{OUT}) changes at a rate proportional to I_{OUT}, V_{OUT} is slew rate limited (SR_{CL}). SR_{CL} is physically independent of the op amp's internally set slew rate (SR); the slower of the two will dominate circuit behavior.

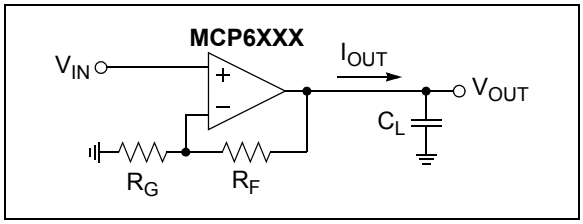

FIGURE 24: *I_{OUT}, C_L, and V_{OUT}.*

We can derive SR_{CL} (units of V/s) as follows:

EQUATION 15:

$$\frac{dV_{OUT}(t)}{dt} = \frac{I_{OUT}(t)}{C_L}$$

$$SR_{CL} = max\left(\frac{dV_{OUT}(t)}{dt}\right) = \frac{I_{SC}}{C_L}$$

Slew Rate and Sine Waves

Sine waves with edge rates faster than SR_{CL} or SR cause signal distortion. The maximum edge rate is:

EQUATION 16:

$$max\left(\frac{dV_{OUT}(t)}{dt}\right) = 2\pi f V_M$$

Where:

$$V_{OUT}(t) = V_M sin(2\pi ft)$$

DESIGN

To avoid slew rate limitations, we need:

EQUATION 17:

$$2\pi f V_M < min(SR_{CL}, SR)$$

One solution is to low-pass filter the signal before it reaches C_L; see Figure 25. The filter (LPF) bandwidth (BW) at the input needs to satisfy:

EQUATION 18:

$$BW < \frac{min(SR_{CL}, SR)}{2\pi V_M}$$

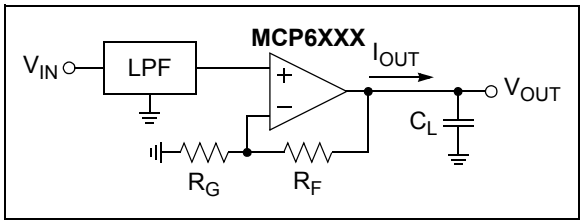

FIGURE 25: *Low-pass Filter that Prevents SR_{CL} Limitations.*

Another solution is to add R_{ISO} as shown in Figure 26. This both limits I_{OUT} and adds an output low-pass filter. The maximum current occurs when $V_{OUT}(t) = 0$; at this point the voltage across R_{ISO} is V_M. Thus, we need:

EQUATION 19:

$$R_{ISO} > V_M / I_{SC}$$

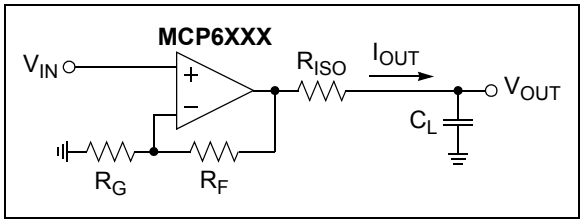

FIGURE 26: *Isolation Resistor (R_{ISO}) that Limits Output Current (I_{OUT}) and Bandwidth (BW).*

This choice will reduce the signal bandwidth at V_{OUT} to:

EQUATION 20:

$$BW = \frac{1}{2\pi R_{ISO} C_L} < \frac{I_{SC}}{2\pi V_M C_L} = \frac{SR_{CL}}{2\pi V_M}$$

This solution gives a result similar to Equation 18, but does not avoid the limitations imposed by the op amp's internal SR. This latter limitation can only be prevented before the op amp, not after.

These design equations, and those in **Appendix A: "2nd Order System Response Model"**, can be used to find the resulting performance as long as the signal's slew rate does not exceed SR or SR_{CL}.

EXAMPLE

Let's look at the MCP6271 with G = +1 V/V and C_L = 1.0 µF. In Table B-1 we find SR = 0.9 V/µs and I_{SC} = 25 mA, giving:

$$SR_{CL} = 0.028 \text{ V/µs}$$

This is much lower than SR. With a maximum peak voltage of $2.5V_{PK}$, we need an input signal with a bandwidth less than 1.8 kHz.

If we use R_{ISO} to limit the output current, then it needs to be > 100 Ω. Setting R_{ISO} = 130 Ω gives:

$$Q_P = 0.046$$
$$f_{3dB} = 1.2 \text{ kHz}$$

If we used the R_{ISO} value for response peaking elimination (7.6 Ω for $Q_P = 1/\sqrt{2}$), we would achieve a wider bandwidth (29 kHz), but would need to keep $V_M < 0.15\ V_{PK}$ to avoid output current limiting and severe signal distortion.

Slew Rate and Square Waves

Square waves with fast edges can also cause problems with capacitive loads. The maximum edge rate of a square wave with a rise time (10% to 90%) of t_r, and a peak-to-peak voltage of V_{PP}, is approximately:

EQUATION 21:

$$max\left(\frac{dV_{OUT}(t)}{dt}\right) \approx \frac{0.8V_{PP}}{t_r}$$

DESIGN

To avoid slew rate limited rise times, we need square waves with lower edge rates (lower V_{PP} and higher t_r):

EQUATION 22:

$$\frac{0.8V_{PP}}{t_r} < min(SR_{CL}, SR)$$

Low-pass filtering the square waves at the input, with a BW = $0.35/t_r$ (see Figure 25), limits the edge rates.

Using slower logic gates also reduces t_r.

The edge rate can be limited at the output by using R_{ISO} (see Figure 26). The maximum I_{OUT} occurs when the ideal output just reaches the new level and $V_{OUT}(t)$ is still slew rate limited. To keep $I_{OUT} < I_{SC}$, we need:

EQUATION 23:

$$R_{ISO} > \frac{V_{PP} - (t_r/0.8)min(SR_{CL}, SR)}{I_{SC}}$$

Using R_{ISO} will both slow the edges down and change the shape of the transitions.

EXAMPLE

Let's use the MCP6271 with G = +1 V/V and C_L = 100 nF. In Table B-1 we find SR = 0.9 V/µs and I_{SC} = 25 mA. We can then calculate:

$$SR_{CL} = 0.25 \text{ V/µs}$$

which is significantly slower than SR. With a maximum voltage swing of $5.0V_{PP}$, we need an input signal with a rise time > 16 µs.

Filtering the input square wave at the input of the op amp would require a bandwidth less than 22 kHz.

If we use R_{ISO} to limit the output current (with a maximum voltage swing of $5.0V_{PP}$ and an input rise time of 10 µs), then we need R_{ISO} > 75Ω. Setting R_{ISO} = 100Ω gives:

$$Q_P = 0.18$$
$$f_{3dB} = 16 \text{ kHz}$$

Note that if we used the R_{ISO} value for response peaking elimination (24.0Ω for $Q_P = 1/\sqrt{2}$), we would achieve a wider small signal bandwidth (92 kHz), but would need to keep $V_{PP} < 3.7V_{PP}$ to avoid output current limiting and reduced rise and fall times.

POWER DISSIPATION

Reactive elements (ideal capacitors and inductors) do not dissipate power. An op amp driving a reactive load, however, does dissipate power; load current in the output stage is rectified by the output transistors.

Figure 27 shows the circuit under discussion. There will be no DC load current because C_L blocks DC. At low frequencies, I_Q (op amp's quiescent current) and C_L will dominate. At high frequencies, R_{ISO} will dominate.

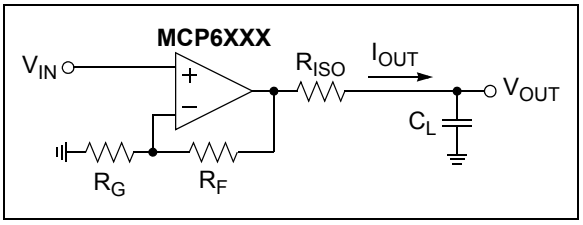

FIGURE 27: *I_{OUT}, C_L, and V_{OUT}.*

At low (sine wave) frequencies, the average op amp power dissipated is:

EQUATION 24:

$$P_{OA} \approx (V_{DD} - V_{SS})(I_Q + 2V_M f C_L)$$

Where:

$$V_{OUT}(t) = V_M sin(2\pi ft)$$
$$f \ll \frac{1}{2\pi R_{ISO} C_L}$$

The power dissipation increases with frequency because C_L dominates the load.

At high frequencies, the average power dissipated by the op amp becomes constant because R_{ISO} dominates:

EQUATION 25:

$$P_{OA} \approx (V_{DD} - V_{SS})\left(I_Q + \frac{V_M}{\pi R_{ISO}}\right) - \frac{V_M^2}{R_{ISO}}$$

Where:

$$f \gg \frac{1}{2\pi R_{ISO} C_L}$$

In the frequency range where neither C_L or R_{ISO} dominates the load ($f \approx 1/(2\pi R_{ISO} C_L)$), estimate P_{OA} as the minimum value from the two formulas above. P_{OA} is actually a little lower than this estimate.

MISCELLANEOUS TOPICS

Simplifications Made in This Application Note

This application note's scope has been limited to keep the results simple to understand and apply. These simplifications include:

- The models (and equations) are simplified
  - Actual circuits have higher order system responses (e.g., 4th-order); possibly including transmission zeros
  - Component variations with process, temperature, operating voltages, and time
- The data in Table B-1 is for guidance only
- Only the most common issues and solutions are included

Driving Multiple Loads

Sometimes op amps are used to drive multiple loads. There can be significant parasitic capacitance at each load, including:

- PCB trace capacitance
- Wiring or coax capacitance
- Capacitors for RFI (EMC) suppression
- Load's input capacitance

These loads can have a significant affect, since there are multiple load points. It may pay to add R_{ISO} on the PCB (at the op amp's output), even when it does not appear to be needed. R_{ISO} can be populated with a very low resistance until the design is tried out in real world conditions.

Driving Large Capacitors Quickly

When capacitive loads are too large to be driven quickly by our op amps, it may pay to look at Microchip's line of Power MOSFET Drivers (www.microchip.com). They have very large bandwidths, rise times, and slew rates; they are designed for capacitive loads.

Design Verification

We recommend that you always verify the performance of your circuit design with SPICE simulations, and by breadboarding it on the bench. Use standard design practices to guard band against unusual events and conditions.

SPICE macro models of Microchip's op amps are available on our web site (www.microchip.com) for your convenience.

SUMMARY

When op amps drive large capacitive loads, they tend to show peaking or oscillation, reduced bandwidth, lower output slew rate, and higher power consumption. Switched capacitors interact with the op amp's output impedance at the switching frequency, causing DC gain errors and other artifacts. These problems exist even in "DC" applications. The output short circuit current causes a limited rate of change in the output voltage.

Adding one resistor (and some times one capacitor) to the circuit can greatly improve the performance. Two different implementations are shown with different trade-offs. Simple formulas are given that allow a circuit designer to quickly evaluate the impact of capacitive loads.

Simulation tools and evaluation on the bench were also covered. Alternate parts for designs with stringent requirements were mentioned.

REFERENCES

Op Amps

[1] Bonnie Baker, *"AN723 - Operational Amplifier AC Specifications and Applications"*, Microchip Technology Inc., DS00723, 2000.

[2] Adel Sedra and Kenneth Smith, *"Microelectronic Circuits"*, 3rd ed., Saunders College Publishing, 1991, Chapter 8.

[3] Paul R. Gray and Robert G. Meyer, *"Analysis and Design of Analog Integrated Circuits",* 2nd ed., John Wiley & Sons, 1984.

Second Order System Response

[4] Charles Phillips and H. Troy Nagle, *"Digital Control System Analysis and Design",* 2nd ed., Prentice Hall, 1990, pp 192-3.

[5] Benjamin Kuo, *"Automatic Control Systems",* 5th ed., Prentice Hall, 1987.

APPENDIX A: 2ND ORDER SYSTEM RESPONSE MODEL

In this application note, we have seen second order transfer functions with no zeros. This type of transfer function models the op amp circuits in this application note reasonably well.

This appendix will show equivalent forms of the transfer function that are useful. It also shows some simple formulas for sine wave and step responses which help evaluate the performance of the circuits in this application note [2, 4, 5]. Suggestions on extracting these parameters from measurements is also given.

A.1 Equivalent Transfer Functions

The form of the transfer function used in the body of this application note is:

EQUATION A-1:

$$\frac{V_{OUT}}{V_{IN}} \approx K \Big/ \left(1 + \frac{s}{\omega_P Q_P} + \frac{s^2}{\omega_P^2}\right)$$

In many engineering fields, including control theory, this transfer function would also be written with the damping coefficient (ζ). This form is useful because ζ divides the response cases into under-damped ($0 < \zeta < 1$), critically damped ($\zeta = 1$), and over-damped ($\zeta > 1$). See reference [5] for more information.

EQUATION A-2:

$$\frac{V_{OUT}}{V_{IN}} \approx K \Big/ \left(1 + 2\zeta \cdot \frac{s}{\omega_P} + \frac{s^2}{\omega_P^2}\right)$$

Where:

$$\zeta = \text{damping coefficient} = \frac{1}{2Q_P}$$

When $Q_P \leq 1/2$, it is useful to factor the denominator into two real poles:

EQUATION A-3:

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{K}{\left(1 + \frac{s}{\omega_{P1}}\right)\left(1 + \frac{s}{\omega_{P2}}\right)}$$

Where:

$$Q_P \leq 1/2$$

$$A = Q_P \cdot \frac{2}{1 + \sqrt{1 - 4Q_P^2}}$$

$$\omega_{P1} = \omega_P A$$

$$\omega_{P2} = \omega_P / A$$

It is sometimes useful to reverse this process:

EQUATION A-4:

$$\omega_P = \sqrt{\omega_{P1}\omega_{P2}}$$

$$Q_P = 1 \Big/ \left(\sqrt{\frac{\omega_{P1}}{\omega_{P2}}} + \sqrt{\frac{\omega_{P2}}{\omega_{P1}}}\right)$$

A.2 Sine Wave Response

Figure A-1 shows a typical frequency (sine wave) response.

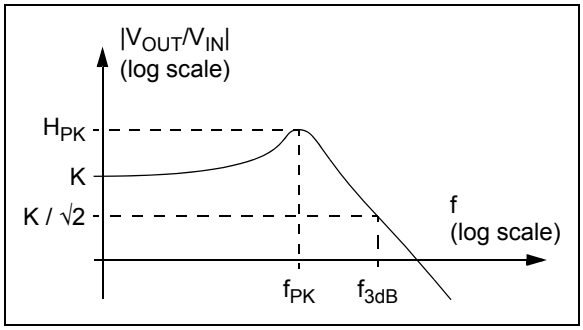

FIGURE A-1: *Frequency Response.*

These exact equations for f_{3dB} are set up to minimize numerical truncation or rounding errors:

EQUATION A-5:

$$f_{3dB} = \frac{f_P Q_P}{\sqrt{\frac{1}{2} - Q_P^2 + \sqrt{\left(\frac{1}{2} - Q_P^2\right)^2 + Q_P^4}}}, \quad Q_P \leq \frac{1}{\sqrt{2}}$$

$$f_{3dB} = f_P \sqrt{1 - \frac{1}{2Q_P^2} + \sqrt{\left(1 - \frac{1}{2Q_P^2}\right)^2 + 1}}, \quad Q_P > \frac{1}{\sqrt{2}}$$

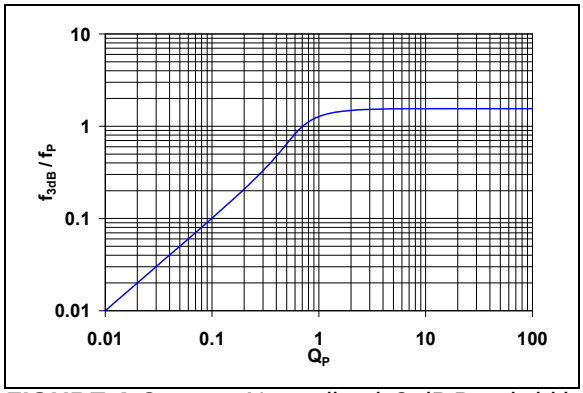

FIGURE A-2: *Normalized -3 dB Bandwidth vs. Q_P*

The peak gain (H_{PK}) occurs at the frequency f_{PK}. Gain peaking (H_{PK}/K) is a normalized parameter:

EQUATION A-6:

$$f_{PK} = 0, \quad Q_P \le 1/\sqrt{2}$$
$$f_{PK} = f_P\sqrt{1-\frac{1}{2Q_P^2}}, \quad Q_P > 1/\sqrt{2}$$

EQUATION A-7:

$$\frac{H_{PK}}{K} = 1, \quad Q_P \le 1/\sqrt{2}$$
$$\frac{H_{PK}}{K} = Q_P/\sqrt{1-\frac{1}{4Q_P^2}}, \quad Q_P > 1/\sqrt{2}$$

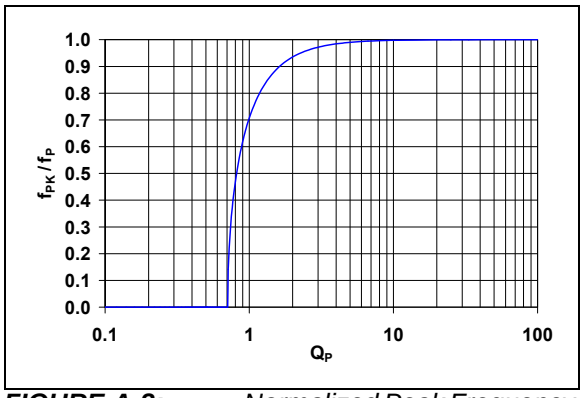

FIGURE A-3: *Normalized Peak Frequency vs. Q_P*

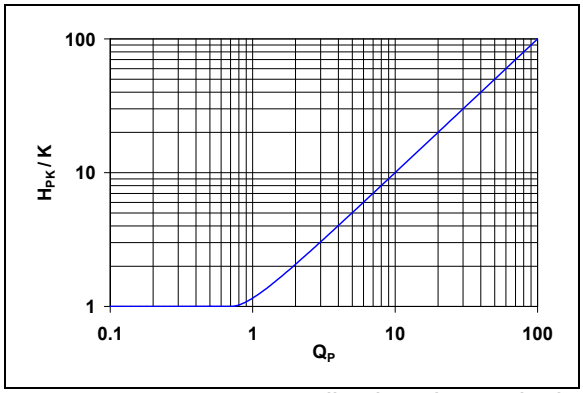

FIGURE A-4: *Normalized Peak Magnitude vs. Q_P*

A.3 Square Wave Response

Figure A-5 shows a typical step (square wave) response; V_{OUT} is normalized by the gain K. The parameters shown are: overshoot (x_{max}), settling accuracy (x_{set}), 10% time (t_{10}), delay (50%) time (t_d), 90% time (t_{90}), time to peak overshoot (t_{max}), and settling time (t_{set}).

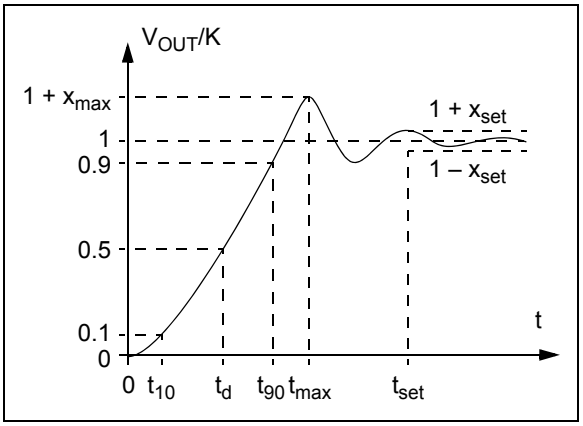

FIGURE A-5: *Step Response.*

The unit step response formulas for under-damped, critically damped, and over-damped responses are:

EQUATION A-8:

$$\frac{V_{OUT}}{K} = [1 - A(t)] \cdot u(t)$$

Where:

$$Q_P < 1/2$$
$$V_{IN}(t) = u(t)$$
$$A(t) = \frac{\omega_{P2}exp(-\omega_{P1}t) - \omega_{P1}exp(-\omega_{P2}t)}{\omega_{P2} - \omega_{P1}}$$

EQUATION A-9:

$$\frac{V_{OUT}}{K} = [1 - B(t)] \cdot u(t)$$

Where:

$$Q_P = 1/2$$
$$V_{IN}(t) = u(t)$$
$$B(t) = (1 + \omega_P t)exp(-\omega_P t)$$

EQUATION A-10:

$$\frac{V_{OUT}}{K} = [1 - C(t)] \cdot u(t)$$

Where:

$$Q_P > \frac{1}{2}$$

$$V_{IN}(t) = u(t)$$

$$A = \sqrt{1 - \frac{1}{4Q_P^2}}$$

$$\phi = acos\left(\frac{1}{2Q_P}\right)$$

$$C(t) = \frac{exp\left(\frac{-\omega_P t}{2Q_P}\right) sin(\omega_P A t + \phi)}{A}$$

The delay time (t_d = 50% time) is roughly:

EQUATION A-11:

$$t_d \approx \frac{0.110 + 0.005Q_P + 0.089Q_P^2 + 0.298Q_P^3}{f_{3dB}}, \quad Q_P \leq \frac{1}{2}$$

$$t_d \approx \frac{\left(0.2587 + \frac{0.0781}{Q_P} - \frac{0.0954}{Q_P^2} + \frac{0.0173}{Q_P^3}\right)}{f_{3dB}}, \quad Q_P > \frac{1}{2}$$

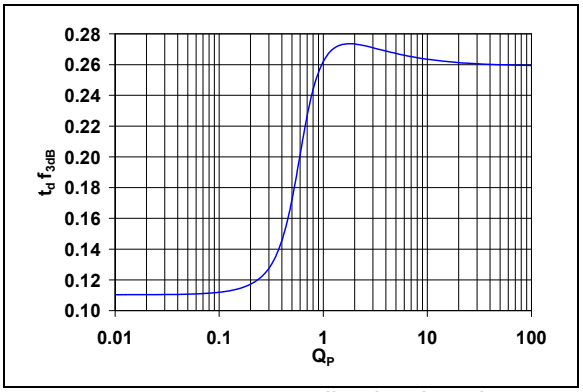

FIGURE A-6: *Normalized Delay Time vs. Q_P*

The 10% to 90% rise time (t_r) is approximately:

EQUATION A-12:

$$t_r = t_{90} - t_{10}$$

$$t_r \approx \frac{0.350 - 0.013Q_P + 0.084Q_P^2 - 0.165Q_P^3}{f_{3dB}}, \quad Q_P \leq \frac{1}{2}$$

$$t_r \approx \frac{\left(0.2503 + \frac{0.1177}{Q_P} - \frac{0.0409}{Q_P^2} + \frac{0.00246}{Q_P^3}\right)}{f_{3dB}}, \quad Q_P > \frac{1}{2}$$

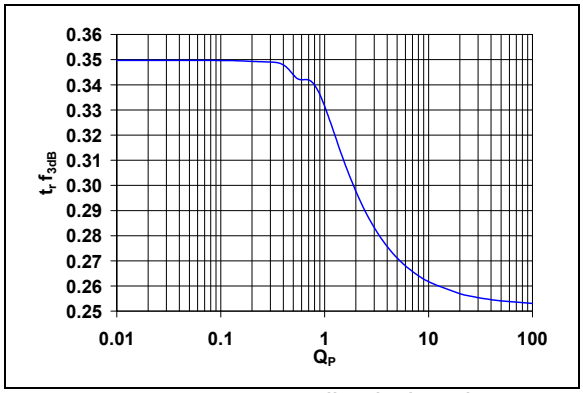

FIGURE A-7: *Normalized Rise Time vs. Q_P*

When Q_P > 1/2, the step response exhibits overshoot (x_{max}). x_{max} and the time to the peak overshoot (t_{max}) are:

EQUATION A-13:

$$x_{max} = 0\%, \quad Q_P \leq 1/2$$

$$x_{max} = (100\%)exp(-\pi/(\sqrt{4Q_P^2 - 1})), \quad Q_P > 1/2$$

EQUATION A-14:

$$t_{max} = 0, \quad Q_P \leq 1/2$$

$$t_{max} = Q_P/(f_P \cdot \sqrt{4Q_P^2 - 1}), \quad Q_P > 1/2$$

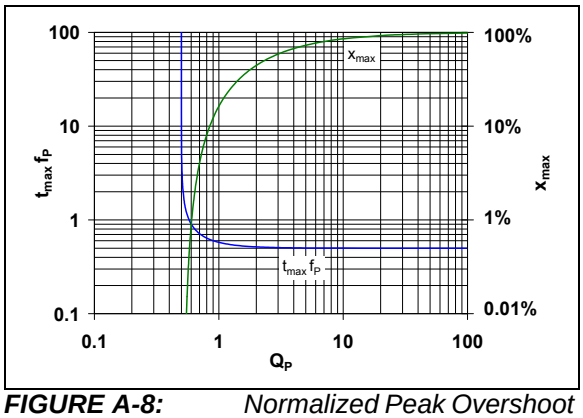

FIGURE A-8: *Normalized Peak Overshoot Time vs. Q_P*

Given a desired settling accuracy (x_{set}), it is possible to estimate the corresponding settling time (t_{set}). When $Q_P \leq 1/2$, the following approximations are useful:

EQUATION A-15:

$$t_{set} \approx \frac{0.367 - 0.013Q_P + 0.270Q_P^2 - 0.232Q_P^3}{f_{3dB}}, \quad x_{set} = 10\%$$

$$t_{set} \approx \frac{0.738 - 0.221Q_P + 1.764Q_P^2 - 3.076Q_P^3}{f_{3dB}}, \quad x_{set} = 1\%$$

$$t_{set} \approx \frac{1.113 - 0.530Q_P + 3.884Q_P^2 - 6.900Q_P^3}{f_{3dB}}, \quad x_{set} = 0.1\%$$

$$t_{set} \approx \frac{1.492 - 0.894Q_P + 6.319Q_P^2 - 11.215Q_P^3}{f_{3dB}}, \quad x_{set} = 0.01\%$$

Where:

$$Q_P \leq \frac{1}{2}$$

When $Q_P > 1/2$, it is hard to calculate the settling time (t_{set}) exactly; the ringing creates discrete jumps in t_{set} as x_{set} is varied. Instead, we estimate the time until the ringing's envelop (t_{env}) reaches the accuracy x_{set}:

EQUATION A-16:

$$t_{env} = -2Q_P \ln\left(x_{set} \cdot \sqrt{1 - \frac{1}{4Q_P^2}}\right) / \omega_P$$

$$t_{set} \leq t_{env}$$

Where:

$$Q_P > \frac{1}{2}$$

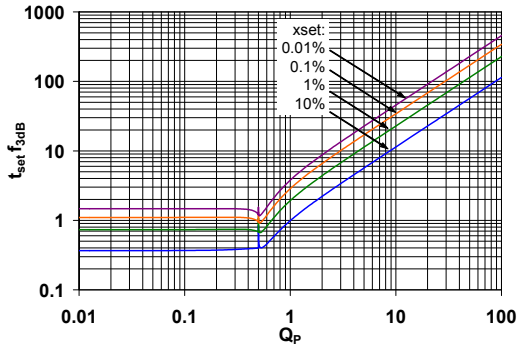

FIGURE A-9: *Normalized Settling Time vs. Q_P*

Note: Figure A-9 shows $t_{set} f_{3dB}$ when $Q_P \leq 1/2$, and shows $t_{env} f_{3dB}$ when $Q_P > 1/2$. t_{set} may actually be smaller than t_{env} in the latter region.

A.4 Extracting a 2nd Order Model From Measurements

When frequency response measurements contain little noise and the response is very close to 2nd order, it is simple to extract K, f_P, and Q_P.

- Extract from $\angle V_{OUT}/V_{IN}$ (in units of °)
  - f_P where the phase is -90°
- Extract from $|V_{OUT}/V_{IN}|$ (in units of V/V)
  - Gain K at low frequencies ($f << f_{3dB}$)
  - Gain KQ_P at the resonant frequency ($f = f_P$)

When there is significant noise, or the response is not approximately quadratic, more sophisticated methods may are needed to fit the data over many frequency points. A least means square fit will be good enough in most cases. Emphasize the fit at frequencies near to the -3 dB bandwidth; this region has the most influence on stability and signal response shape.

APPENDIX B: MICROCHIP OP AMPS

B.1 Estimating f_{2P}

To estimate f_{2P} for the op amp model, find the frequency in the data sheet's Open-Loop Gain plot where the phase is -135° (f_{-135}). Adjust f_{-135} for the typical capacitive load (C_{Ltyp}) used in that plot (usually 60 pF in our data sheets):

EQUATION B-1:

$$\phi_{CLtyp} \approx atan(2\pi f_{-135} R_O C_{Ltyp})$$

$$f_{2P} \approx f_{-135} / tan(45° - min(\phi_{CLtyp}, 40°))$$

B.2 Op Amp Performance

The performance parameters of some Microchip op amps shown in Table B-1 were extracted from the parts' data sheets. These data sheets contain the officially supported specifications, and can be found on our web site (www.microchip.com).

TABLE B-1: ESTIMATES OF TYPICAL MICROCHIP OP AMP PARAMETERS

Part	G_{N_MIN} (V/V) Specified	f_{GBP} (Hz) Typ	SR (V/µs) Typ	f_{-135} (Hz) Typ	I_{SC} at min V_{DD} (mA) Typ	I_{SC} at max V_{DD} (mA) Typ	R_O (Ω) Meas	Φ_{CLtyp} (°) Typ	f_{2P} (Hz) Typ
MCP6041	1	14k	0.003	23k	2	20	101k	41	263k
MCP6141	10	100k	0.024	15k	2	20	108k	31	62.1k
MCP6031	1	10k	0.004	23k	5	23	72.8k	32	102k
TC1034 **(Note 1)**	1	60k	0.035	510k	8	8	15.8k	72	5.83M
MCP606	1	155k	0.080	270k	7	17	4.20k	23	673k
MCP616	1	190k	0.080	300k	7	17	5.05k	30	1.10M
MCP6231	1	300k	0.15	800k	6	23	2.62k	38	6.83M
MCP6241	1	550k	0.30	1.20M	6	23	1.69k	37	8.99M
MCP6001	1	1.00M	0.60	1.00G	6	23	780	90	11.4G
MCP6271	1	2.00M	0.90	5.00M	25	25	368	35	27.6M
MCP601	1	2.80M	2.3	3.10M	22	12	350	22	7.39M
MCP6281	1	5.00M	2.5	11.0M	25	25	173	36	66.9M
MCP6291	1	10.0M	7.0	28.0M	25	25	108	49	320M
MCP6021	1	10.0M	7.0	20.0M	30	22	108	39	195M

Note 1: The TC1034 parameters also apply to the TC1026, TC1029, TC1030, and TC1035.

B.3 MCP6V01/2/3 and MCP6V06/7/8 Op Amps

These auto-zeroed op amps have an output impedance that is more complex than the simple model shown in Figure 5. To stabilize these op amps, see the information in their data sheets.

APPENDIX C: MCP3421 SAMPLING RATES

The current MCP3421 data sheet (as of November 2008) does not directly include information on its sampling rate. The data rate is related to the sampling rate; it includes overhead for communication to the microcontroller.

TABLE C-1: MCP3421 SAMPLING RATES

Precision (bit) Selected	Data Rate (SPS) Typ	Sampling Rate (SPS) Typ (Note 1)
12	240	256
14	60	1024
16	15	4096
18	3.75	16386

Note 1: The data sheet is the official source of specifications; this table is for information only.

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