Low power single/dual frequency synthesizers: UMA1017M/1018M/1019M(AM)/1020M(AM)

AN95102

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UMA1018M and UMA1020M/UMA1020AM low power dual frequency synthesizers

UMA1017M and UMA1019M/UMA1019AM low power single frequency synthesizers

SUMMARY

This application note describes the UMA1018M and UMA1020M/UMA1020AM from Philips Semiconductors. They permit a low-voltage low-power single-chip solution to designing dual PLL frequency synthesizers. They are intended for use in digital or analogue wireless communications equipment. Typical applications include GSM, DECT and DCS1800.

Three low-voltage low-power solutions to single frequency synthesizers are also briefly described. The UMA1017M and UMA1019M/UMA1019AM are derivatives from UMA1018M and UMA1020M, respectively, and are hence closely related.

The overall performance of any PLL frequency synthesizer system is critically determined by the low pass filter used. Described in this report is a basic loop filter design method with worked examples and some measurement results.

1. INTRODUCTION TO UMA1018M DUAL SYNTHESIZER

1.1 General description

The UMA1018M [1] is a low power low voltage single chip solution to a dual frequency synthesizer used in radiocommunications. Designed in a BICMOS process, it operates from 2.7 (3 NiCd cells) to 5.5 V. The UMA1018M contains all the necessary elements with the exception of the VTCXO, VCO and loop filters to build two PLL frequency synthesizers.

It is intended that the principal synthesizer operates in the 50 to 1250 MHz range, and the auxiliary synthesizer will work between 20 and 300 MHz. For each synthesizer, fully programmable main and reference dividers are integrated on chip. The reference input FXTAL can operate from 5 to 40 MHz. Fast programming is possible via the three wire serial bus with clock speeds of up to 10 MHz.

The principal synthesizer phase detector drives a low current charge pump and a high current charge pump simultaneously. Maximum output current is 0.4 mA with the low current charge pump (pin CPP) and 3.2 mA with the other (pin CPPF). The auxiliary phase detector drives only one charge pump. The programmable charge pump currents are fixed by an external resistance R_{ext} at pin I_{SET}. Only passive loop filters are necessary.

To reduce crosstalk between different parts of the synthesizer, separate power supply and ground pins are provided to the analogue and digital sections.

Each synthesizer can be powered down independently to save current via software programming or hardwire pins AON / PON.

An on-chip 7 bit DAC allows adjustment of external functions, such as temperature compensation of the VTCXO, power amplifier control, etc.

1.2 FEATURES

- Dual frequency synthesizers
- Operating voltage range 2.7 to 5.5 V for battery powered operation
- Low current consumption, 10 mA typically at 5.5 V (two PLLs enabled)
- Integrated fully programmable main divider for each synthesizer
  - Principal: 512 to 131,071 up to 1.25 GHz input
  - Auxiliary: 64 to 16,383 up to 300 MHz input
- Independent fully programmable reference divider for each synthesizer
  - Principal: 8 to 2074 up to 2 MHz output
  - Auxiliary: 8 to 2047 up to 1 MHz output
- 3-wire serial bus (Data, Clock, Enable) for fast programming (f_{max} = 10 MHz)
- Independent hardwire and software power down modes for both synthesizers
- Simple passive loop filters
- Charge pump output current under bus control, with reference current I_{SET} set by an external reference resistor R_{ext}
- Programmable out-of-lock detector
- Integrated D-to-A converter
- Small SSOP-20 package

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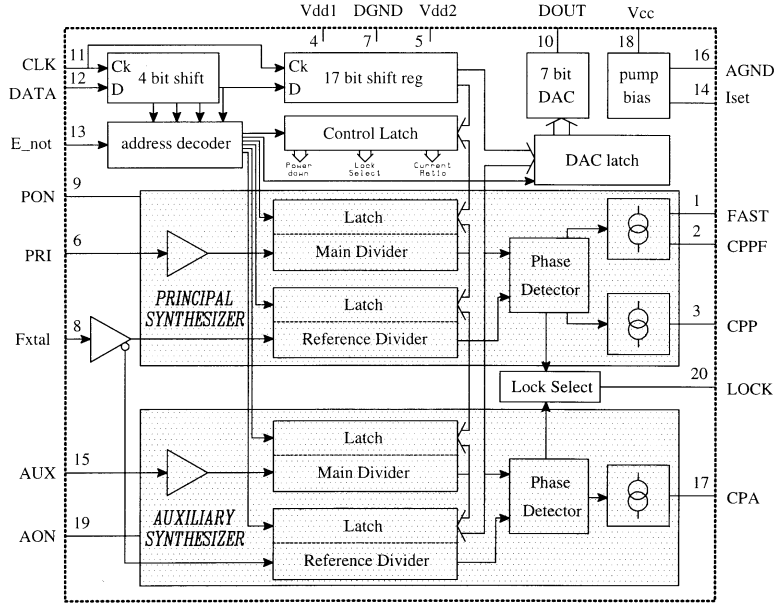

Figure 1–1. UMA1018M Block Diagram

1.3 Typical Application Architecture

UMA1018M integrated circuit is typically used in digital radiotelephone systems like GSM. It is designed to meet the requirements of these systems; low noise (residual and spurious), fast switching and low current consumption (at 5.5 V: 10 mA with both synthesizers ON and 36 μA with both synthesizers OFF).

Figure 1–1 demonstrates a typical application. UMA1018M is integrated on a dual superheterodyne architecture using two local oscillators.

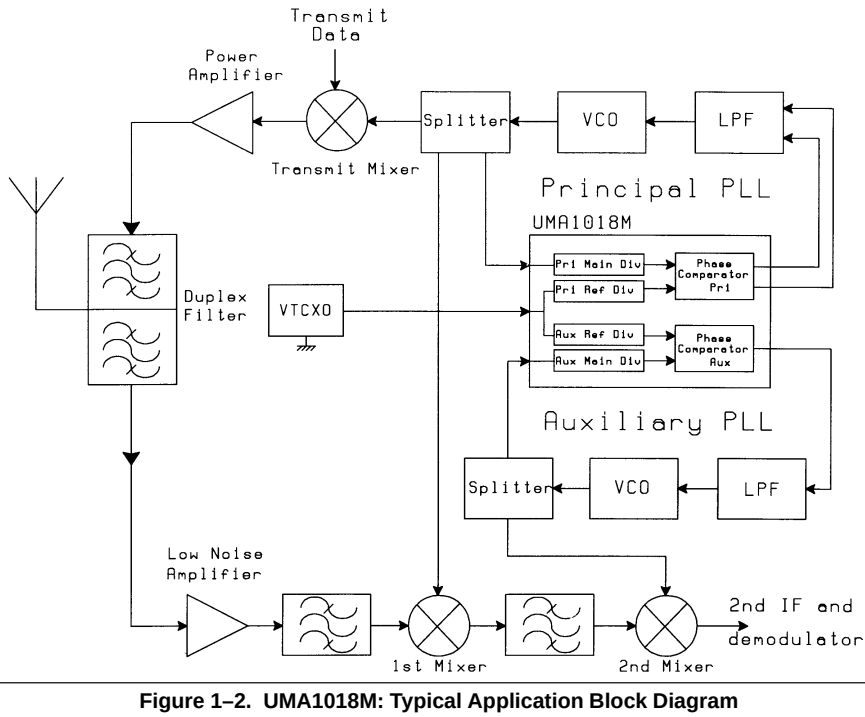

Figure 1–2. UMA1018M: Typical Application Block Diagram

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1.4 UMA1018M Family

To satisfy the need of the emerging digital communication systems, a family of synthesizer controls based around the UMA1018M has been developed.

1.4.1 UMA1020M/UMA1020AM Dual Synthesizers

UMA1020M [2] is used in 2 GHz applications, like PHP, DCS1800 or DECT. Its principal synthesizer operates from 1.7 to 2.4 GHz. It offers the same functions as the UMA1018M dual synthesizer including the 7-bit DAC. The UMA1020AM [3] principal synthesizer works from 1 to 1.7 GHz. It does not include the DAC.

1.4.2 UMA1017M and UMA1019M/UMA1019AM Single Synthesizers

The UMA1017M [4] and UMA1019M/UMA1019AM integrated circuits are derivatives from UMA1018M and UMA1020M, respectively with similar pinning. They contain the principal synthesizer only. UMA1017M operates from 50 to 1250 MHz, UMA1019M [5] from 1.7 to 2.4 GHz and UMA1019AM [6] from 1 to 1.7 GHz. Neither contains the auxiliary synthesizer or the DAC (see Figure 1–3).

In this application note, no extra mention will be made about UMA1020AM and the single synthesizers. All UMA1018M and UMA1020M principal synthesizer descriptions and results are valid for other circuits.

Table, overleaf, summarizes characteristics and typical applications of each synthesizer.

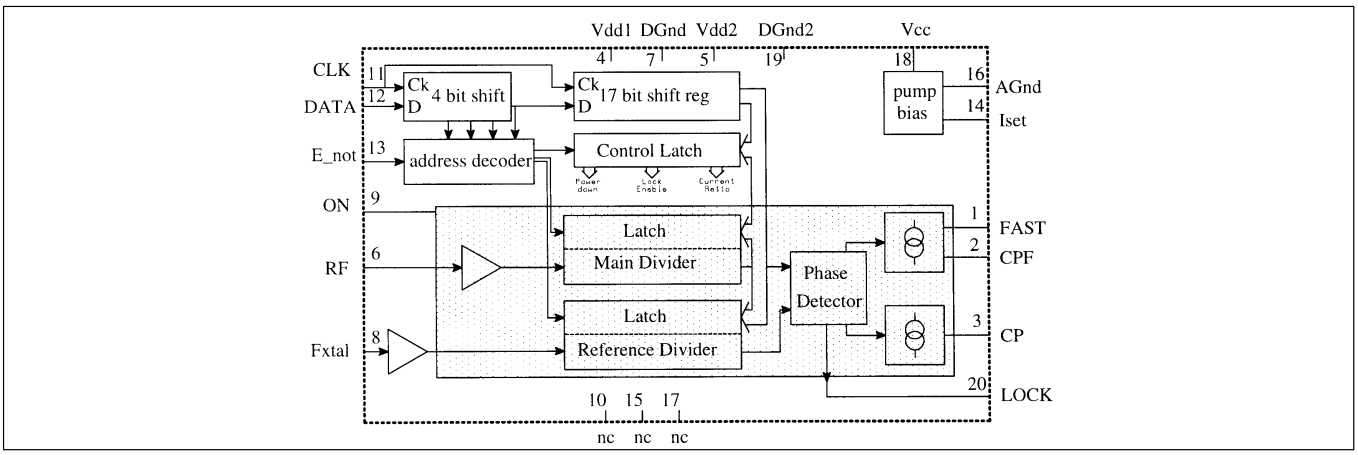

Figure 1–3. UMA1017M and UMA1019M/UMA1019AM Block Diagram

Table 1–1. Frequency Synthesizers Update

Part No.	Supply	Consumption	RF Input Frequency	Main Applications
UMA1017M	2.7 to 5.5 V	7.7 mA (5.5 V) 36 µA (PD)	Single 50 to 1250 MHz	CT2 digital cordless GSM digital cellular General purpose
UMA1018M	2.7 to 5.5 V	10 mA (5.5 V) 36 µA (PD)	Dual 50 to 1250 MHz (main) 20 to 300 MHz (aux)	Cellular systems like GSM Applications with UHF and VHF synthesizers
UMA1019AM	2.7 to 5.5 V	9.4 mA (5.5 V) 36 µA (PD)	Single 1 to 1.7 GHz	General purpose
UMA1019M	2.7 to 5.5 V	9.4 mA (5.5 V) 36 µA (PD)	Single 1.7 to 2.4 GHz	DECT Zero IF Cordless and wireless radios
UMA1020AM	2.7 to 5.5 V	12.1 mA (5.5 V) 36 µA (PD)	Dual 1 to 1.7 GHz (main) 20 to 300 MHz (aux)	General purpose
UMA1020M	2.7 to 5.5 V	12.1 mA (5.5 V) 36 µA (PD)	Dual 1.7 to 2.4 GHz (main) 20 to 300 MHz (aux)	Ideal for DECT superhet Digital cordless and wireless radios

2. FUNCTIONAL DESCRIPTION OF THE UMA1018M AND UMA1020M SYNTHESIZERS

The principle of the Phase Locked Loop (PLL) is illustrated in the PLL application block diagram (Figure 3–1).

A crystal (VTCXO) provides a reference frequency to the PLL. A phase detector drives a charge pump to send correction current pulses to a low pass filter. Current pulses are proportional to the difference in phase between the two phase detector input signals. The filter integrates the pulses giving a voltage which controls a Voltage Controlled Oscillator. VCO frequency and crystal frequency are divided down to a common comparison frequency to control the phase detector. The PLL is locked when the phase difference between input signals is maintained null.

2.1 Phase Detector and Charge Pump

2.1.1 Description

The principal and auxiliary phase detectors in the dual synthesizers are sensitive to both phase and frequency. They react to small phase differences between the main divider and reference divider inputs. The design responds to the full ±2∏ radians range of phase inputs.

The operating principle of the phase detectors is depicted in Figure 2–1. The comparison frequency f_{PC} at the inputs of the phase detector is typically the same as the radio system channel spacing. The phase detection is performed once each period of the comparison frequency.

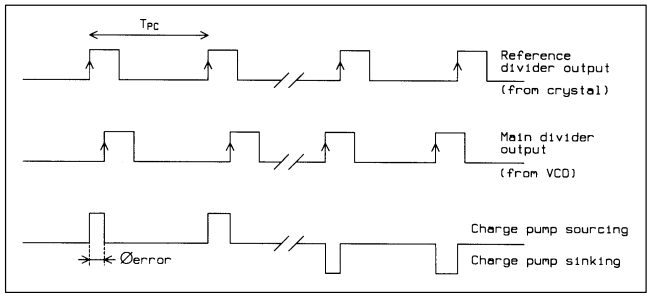

Figure 2–1. Principle of UMA1018M Phase Detectors

The charge pump outputs of the synthesizers are either sourcing, sinking or in high impedance. When the loop is locked, i.e., when the phase error at the input of the phase detector is zero, the charge pump output is in the high impedance state. When the loop is not locked, a phase error between the input signals is seen by the phase detector and the charge pump sends correction current pulses to the loop filter. If the output of the reference divider is leading, then the charge pump sources current pulses to increase the VCO control voltage and frequency. If the output of the reference divider is lagging, then the charge pump sinks current pulses to decrease the VCO control voltage and frequency. The pulse duration is proportional to the phase error. The sinking and sourcing pulses charge or discharge the capacitors in the loop filter, to a voltage required to bring the PLL back into lock.

The principal phase detector drives two charge pumps (pins CPP and CPPF). The charge pump current (the “height” of the positive or negative pulses in Figure 2.1) are switch–selectable by software. I_{CPPF} maximum output current is 3.2 mA, and that for CPP is 0.4 mA. The I_{CPPF}:I_{CPP} current ratio between the two charge pumps varies from 4 to 16. The reference current I_{SET} is set by an external resistance R_{ext} at pin I_{SET}, where a temperature independent voltage of 1.2 volts is generated. R_{ext} should be between 12 kΩ and 60 kΩ to give an I_{SET} between 100 µA and 20 µA. The auxiliary charge pump output current (pin CPA) is always 4 x I_{SET} the charge pump output currents can be programmed as shown below.

Table 2–1. Charge Pumps Current Ratio Relationships

CR1	CR0	I_{CPA}	I_{CPP}	I_{CPPF}	I_{CPPF} : I_{CPP}
0	0	4 x I_{SET}	4 x I_{SET}	16 x I_{SET}	4 : 1
0	1	4 x I_{SET}	4 x I_{SET}	32 x I_{SET}	8 : 1
1	0	4 x I_{SET}	2 x I_{SET}	24 x I_{SET}	12 : 1
1	1	4 x I_{SET}	2 x I_{SET}	32 x I_{SET}	16 : 1

There are three ways to connect the charge pump outputs to the principal loop filter:

- Generally, the two charge pump outputs (CPP and CPPF) are connected together to the loop filter. The loop filter design is given in section 3.1.
- In some applications, the PLL is only closed during frequency switching, and opened during time slots where the transmitter (for open loop modulation) or the receiver must be active. In this case, the pin FAST allows opening the loop by disabling the principal fast charge pump. Only this pump should be connected to the loop filter. The principal charge pump (CPP output) is grounded.
- The third way is to have a dual time constant loop. The loop uses both charge pumps during frequency switching. The phase detector drives just the principal charge pump after the required frequency is obtained. The fast charge pump is disabled by the pin FAST. The loop filter design procedure is shown in section 3.3.

The following curves show measurements of sink and source currents of the auxiliary and principal fast charge pumps, as well as leakage currents (high impedance) of the different charge pumps.

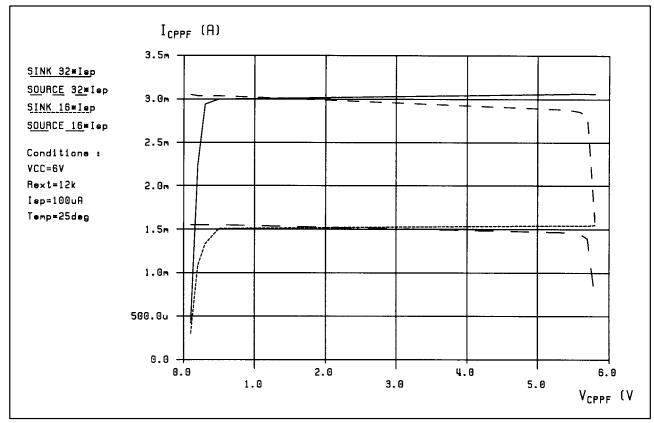

Figure 2–2. Principal Fast Charge Pump (CPPF) Output Current vs Voltage

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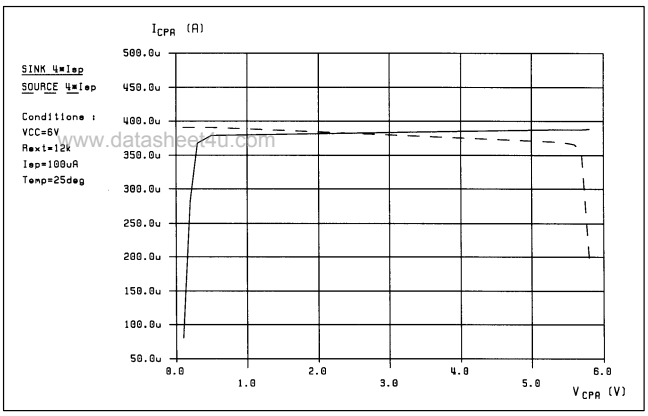


Figure 2–3. Auxiliary Charge Pump (CPA) Output Current vs Voltage

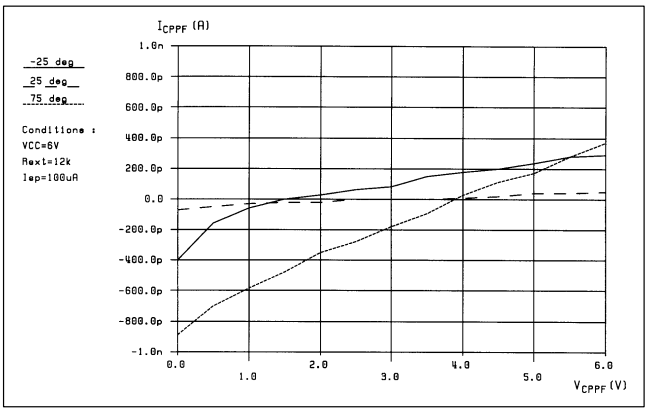


Figure 2–4. Principal Fast Charge Pump Leakage Current vs Voltage and Temperature

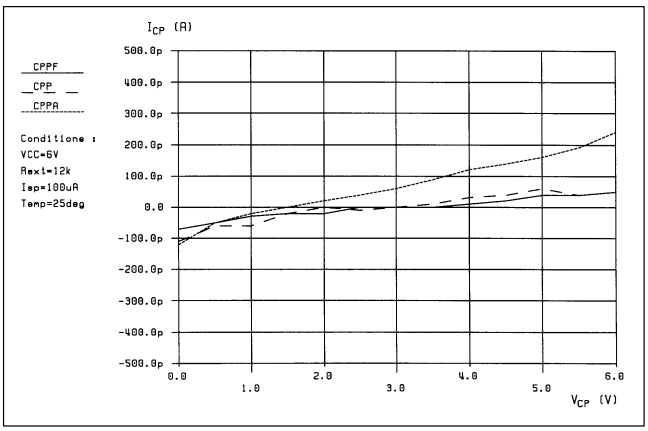


Figure 2–5. Leakage Current of UMA1018M Charge Pumps vs Voltage

2.1.2 Dynamic Characteristics

Two problems occur when the phase detector input signals' edges are very close together, i.e., when the phase error is zero (PLL is locked) or around zero (PLL has nearly settled after switching).

– The first problem is known as the dead–zone. It is due to the finite time the current sources take to switch on. The design of the UMA1018M and UMA1020M takes this into account by introducing a delay in the phase detector reset path. This gives the current sources enough time to respond.

– The second problem is that the charge pump gain is dependent on temperature and VCO control voltage. In this region, the gain varies as a function of the phase error. When the phase error increases outside the defined region, the charge pump gain becomes essentially independent and constant (see curve overleaf). This section is intended to show the linearity of the phase detectors and charge pumps.

Measurement method:

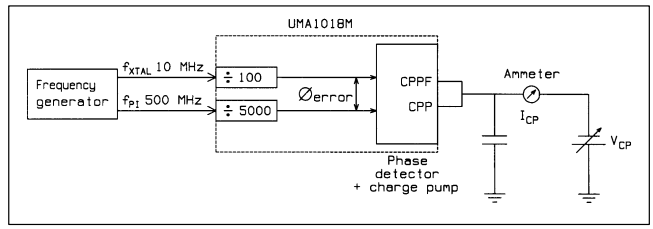
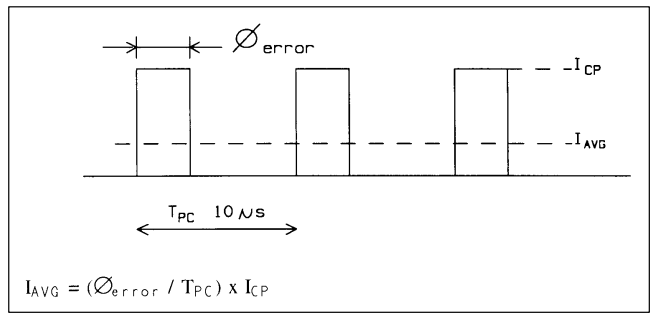
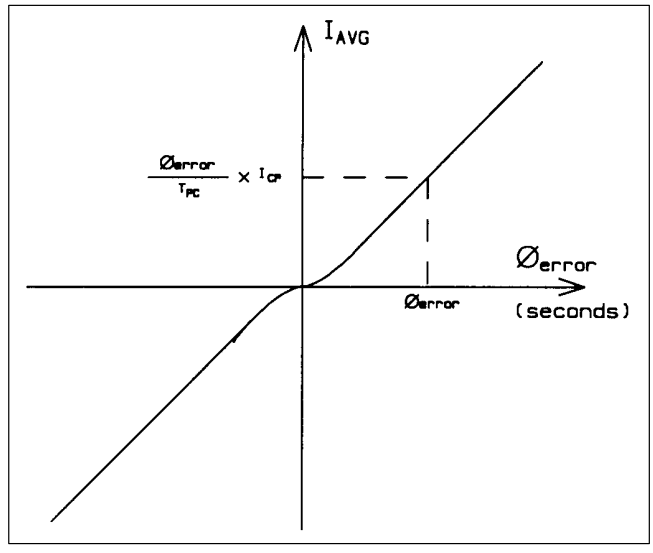


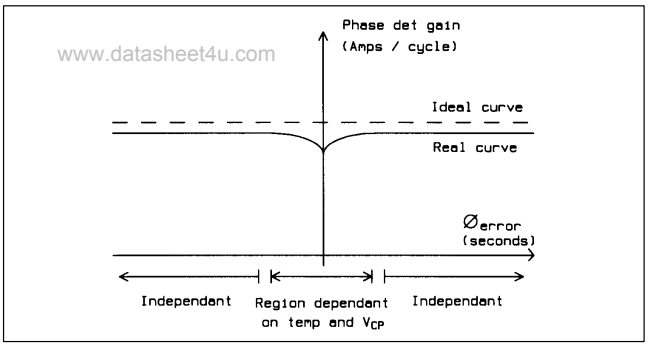
Figure 2–6. UMA1018M Principal Synthesizer Phase Detector Linearity Measurement

A frequency generator supplies the reference frequency f_{XTAL} and the main frequency f_{PI}. These frequencies are divided down to obtain a comparison frequency of 100 kHz. The generator allows controlling the phase of the 500 MHz signal with respect to the 10 MHz reference signal. The I_{AVG} phase detector current is measured as a function of the phase error:





In order to find the real phase detector and charge pump gain for very small phase errors, we transform this curve by the equation: Phase det gain (Amps/cycle) = $I_{AVG} \times (T_{PC}/\Phi error)$



Phase error values are taken in the region of ±10 ns. This is where the phase detector and the charge pump are less linear and where the loop spends most of its time, i.e., when it is locked or nearly locked. The following curves show measurements for source and sink gains around zero, showing the small departure from ideal. The jagged nature of the curves can partly be explained by very small values of I_{AVG}, and phase error giving granularity problems. In any case real charge pump gain for very small phase errors is mostly maintained within 25% of ideal value.

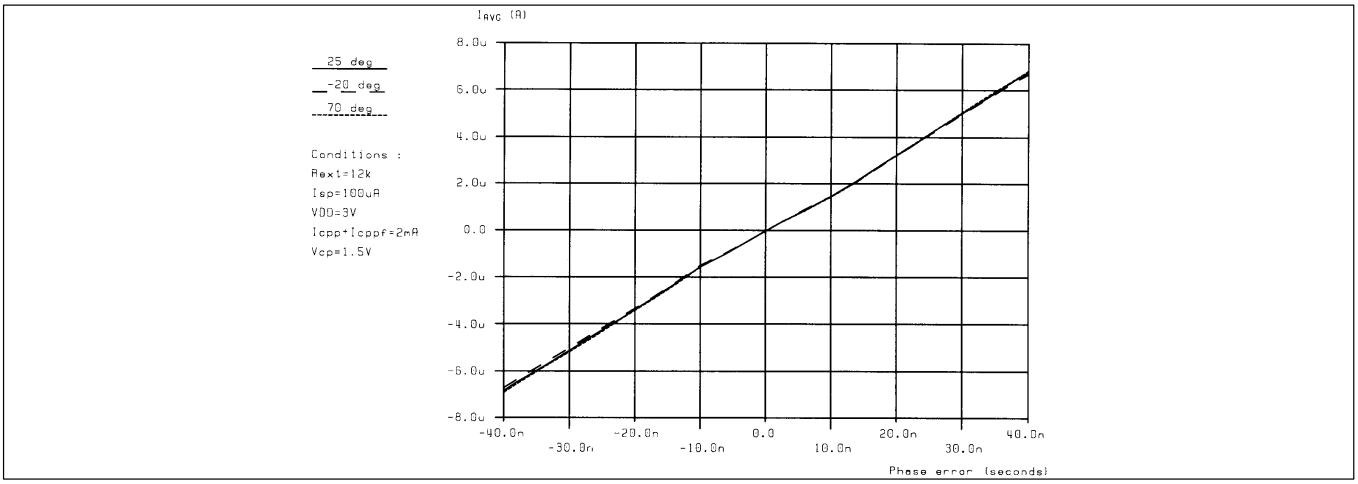


Figure 2–7. Principal Phase Detector and Charge Pump Characteristics vs Temperature

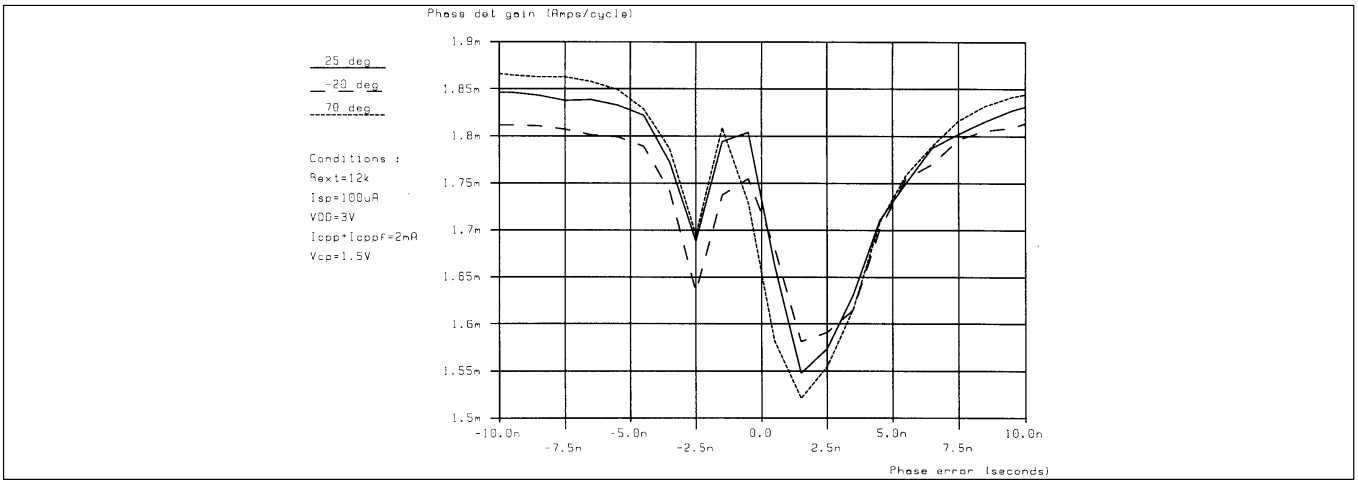


Figure 2–8. Principal Phase Detector and Charge Pump Gain vs Temperature

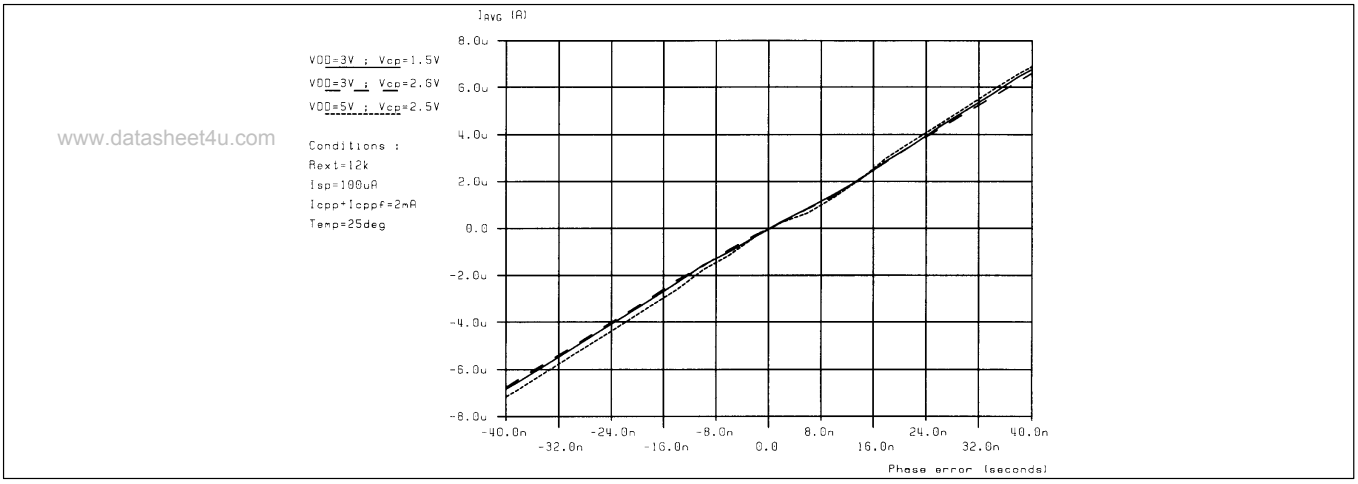


Figure 2–9. Principal Phase Detector and Charge Pump Characteristics vs Temperature

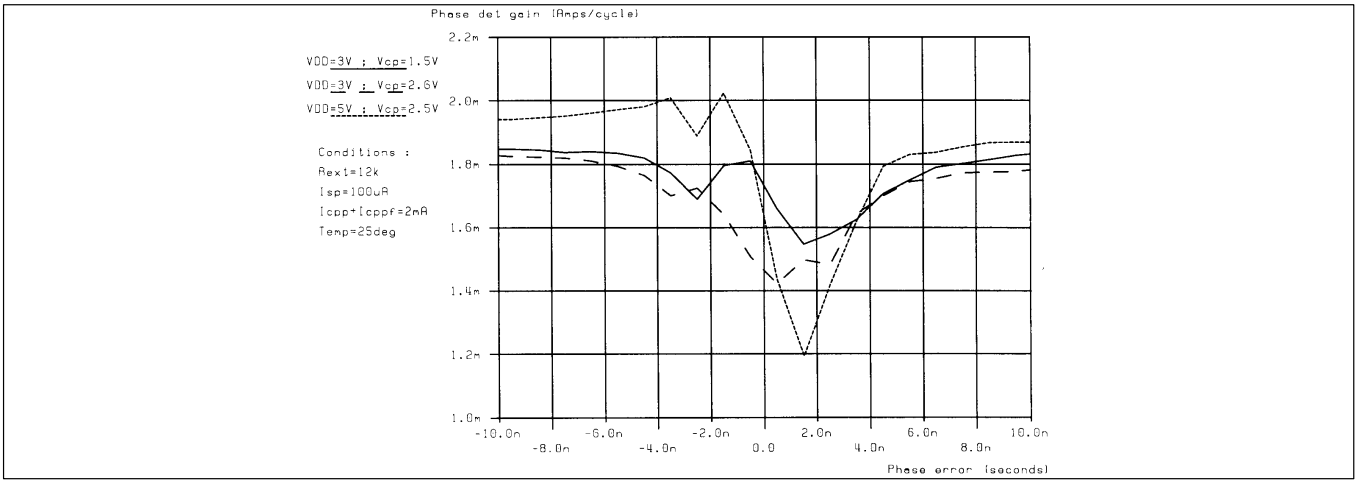


Figure 2–10. Principal Phase Detector and Charge Pump Gain vs V_{DD}

2.2 Programming

A simple 3-wire unidirectional serial bus is used to program the synthesizer. The three lines are DATA, CLK (Clock) and $\overline{E}$ (Enable). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges are ignored until $\overline{E}$ goes active low. The programmed information is loaded into the addressed latch when $\overline{E}$ returns inactive high. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programming data even during power–down of either or both synthesizers.

After software or hardware power down is terminated, it is not necessary to program the device. Previous programming data is preserved during power down.

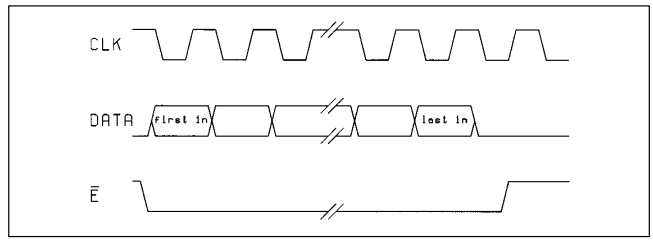


Figure 2–11. Serial Interface Timing Diagram

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are used for the address. The bits are decoded on the rising edge of $\overline{E}$. Two worked examples of programming are shown overleaf.

Special care has to be taken for correct programming when first applying power to the synthesizer. The E signal should be held LOW and only taken HIGH after having programmed an appropriate register on first powering up. If this condition is not achieved, it may result in loading of random data from the serial bus shift register (programming register) into one of the synthesizers data registers including the test register. It should be noted that the test register does not normally need to be programmed. However, if it is programmed, all bits in the data field should be set to 0. In case of random data being loaded into the test register, it is possible to program a frame of zeros, to return to normal operation.

2.2.1 UMA1018M Typical Programming Example

f_{XTAL} input frequency: 13 MHz
Principal synthesizer input frequency: 900 MHz (main divider ratio = PM = 4500)
Principal synthesizer comparison frequency: 200 kHz (main divider ratio = PR = 65)
Auxiliary synthesizer input frequency: 100 MHz (main divider ratio = AM = 1000)
Auxiliary synthesizer comparison frequency: 100 kHz (main divider ratio = AR = 130)
Both synthesizers ON (AON = PON = 1)
Out-of-lock indication from both synthesizer loops (OLP = OLA = 1)
Charge pump currents: I_{CPPF} = 32 x I_{SET}; I_{CPP} = 4 x I_{SET} (CR1 = 0 CR0 = 1)

Table 2–2. UMA1018M Register Data Allocations Expressed in Decimal and Hexidecimal

First In	Register Bit Allocation	Last In
dt16	Data Field dt0	Address
Test register (must be 0 if programmed)		0h
Control reg = 0 0001 101010110 0000b		1h
Principal main = 4500d = 01194h		4h
Principal reference = 65d = 00041h		5h
Auxiliary main = 1000d = 003E8h		6h
Auxiliary reference = 130d = 00082h		7h
DAC setting is 123d = 0007Bh		8h

Table 2–3. UMA1018M Register Data Allocations Expressed in Binary

First In (MSB)							Data Field								(LSB) Last In		Address			
0	0	0	0	1	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	0	1	1	0	0	1	0	1	0	0	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1
0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1	1
0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	1	0	0	0

2.2.2 UMA1020M Typical Programming Example

f_{XTAL} input frequency: 13.824 MHz
Principal synthesizer input frequency: 1890.432 MHz (main divider ratio = PM = 1094)
Principal synthesizer comparison frequency: 1728 kHz (main divider ratio = PR = 8)
Auxiliary synthesizer input frequency: 300.52 MHz (main divider ratio = AM – 3000)
Auxiliary synthesizer comparison frequency: 100.17 kHz (main divider ratio = AR = 138)
Both synthesizers ON (AOFF = POFF = 0)
Out-of-lock indication from both synthesizer loops (OLP = OLA = 1)
Charge pump currents : I_{CPPF} = 32 x I_{SET} ; I_{CPP} = 4 x I_{SET} (CR 1 = 0 CR0 = 1)

Table 2–4. UMA1020M Register Data Allocations Expressed in Decimal and Hexidecimal

First In	Register Bit Allocation	Last In
dt16	Data Field dt0	Address
Test register (must be 0 if programmed)		0h
Control reg = 0 0001 1010 0000 0000b		1h
Principal main = 1094d = 00446h		4h
Principal reference = 8d = 00008h		5h
Auxiliary main = 3000d = 00BB8h		6h
Auxiliary reference = 138d = 00082h		7h
DAC setting is 123d = 0007Bh		8h

Table 2–5. UMA1020M Register Data Allocations Expressed in Binary

First In (MSB)							Data Field								(LSB) Last In		Address			
0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	1	0	0	1	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1
0	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	1	1	1
0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	1	0	0	0

2.2.3 UMA1018M and UMA1020M Preset Values

After the supply voltage is switched on, the preset values are normally:

Principal main divider ratio: 4500
Principal reference divider ratio: 65
Auxiliary main divider ratio: 8000
Auxiliary reference divider ratio: 1040
Control register: all 1 except out-of-lock
DAC register: all 0
Test register: all 0

2.2.4 Enable Pulse Width

With $\overline{E}$, a minimum inactive pulse width (T_W in the specification) is necessary before sending a new data burst. Due to internal synchronization, this minimum width depends on the input frequency to the main dividers and the reference divider. In the specification, this is indicated as 4 µs.

In fact, the minimum pulse width (T_W) can be smaller than 4 µs provided the following conditions are all satisfied:

Principal main divider input frequency > ($256/T_W$)
Auxiliary main divider input frequency > ($32/T_W$)
Reference dividers input frequency > ($3/T_W$)

Example: a pulse width of 500 ns can be used if

f_{PI} > 256 / 500 ns f_{PI} > 512MHz
f_{AI} > 32 / 500 ns f_{AI} > 64MHz
f_{XTAL} > 3 / 500 ns f_{XTAL} > 6MHz

2.3 Reference Divider

The input f_{XTAL} drives a preamplifier to provide the clock input for the reference dividers. The auxiliary reference divider is clocked on the opposite edge to the main reference divider to ensure that active edges arrive at the auxiliary and principal phase detectors at

different times. This minimizes the potential for interference between the charge pumps of each loop. Figure 2–12 shows the typical measured input sensitivity of the reference divider.

Some sensitivity to the reference input signal level on overall loop noise performance has been observed. Better performance is obtained for a higher level of f_{XTAL}.

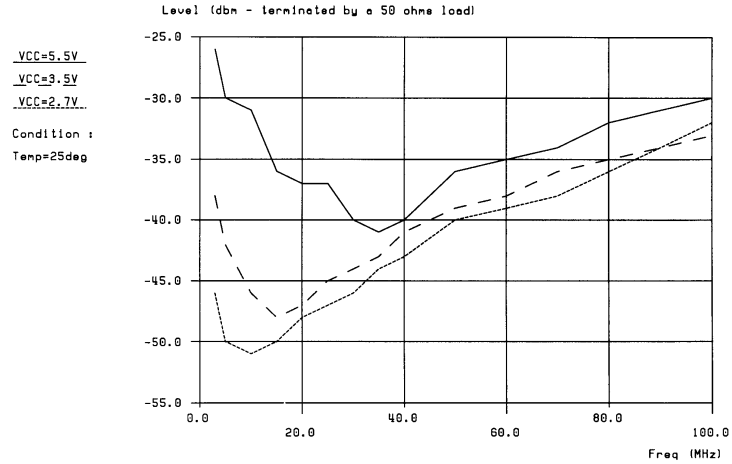


Figure 2–12. Reference Divider Input Sensitivity vs Frequency

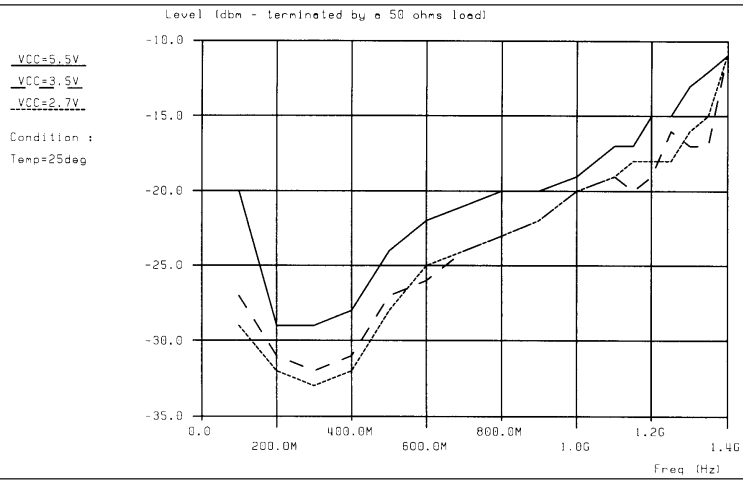


Figure 2–13. UMA1018M Principal Main Divider Input Sensitivity vs Frequency

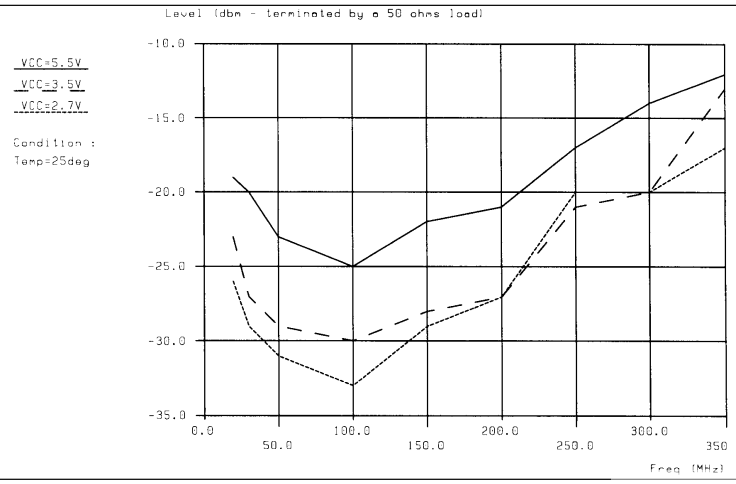


Figure 2–14. Auxiliary Main Divider Input Sensitivity vs Frequency

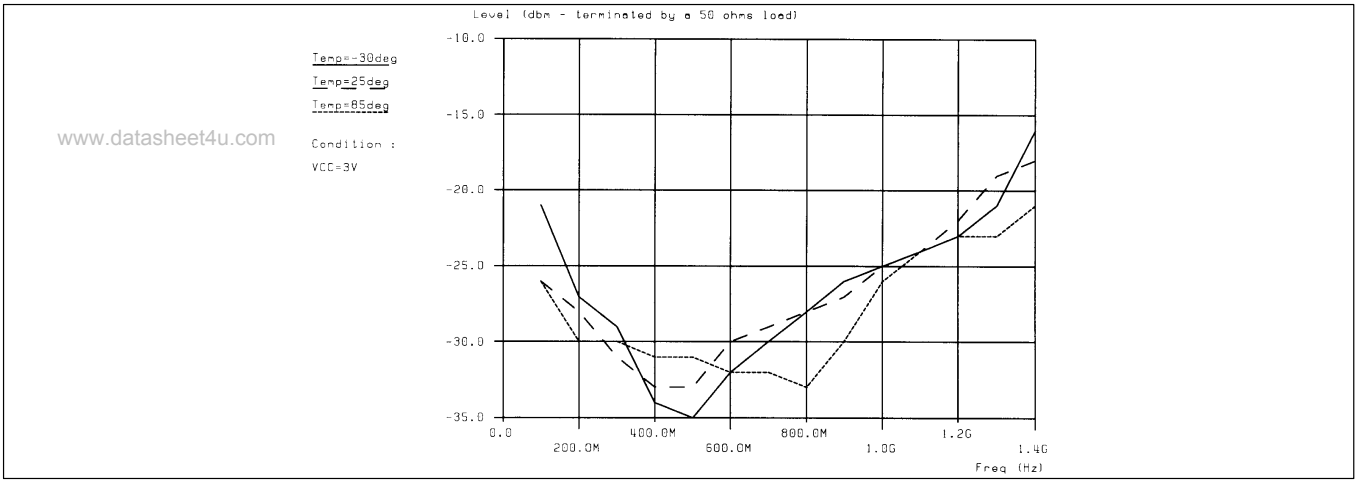


Figure 2–15. UMA1018M Principal Main Divider Input Sensitivity vs Frequency and Temperature

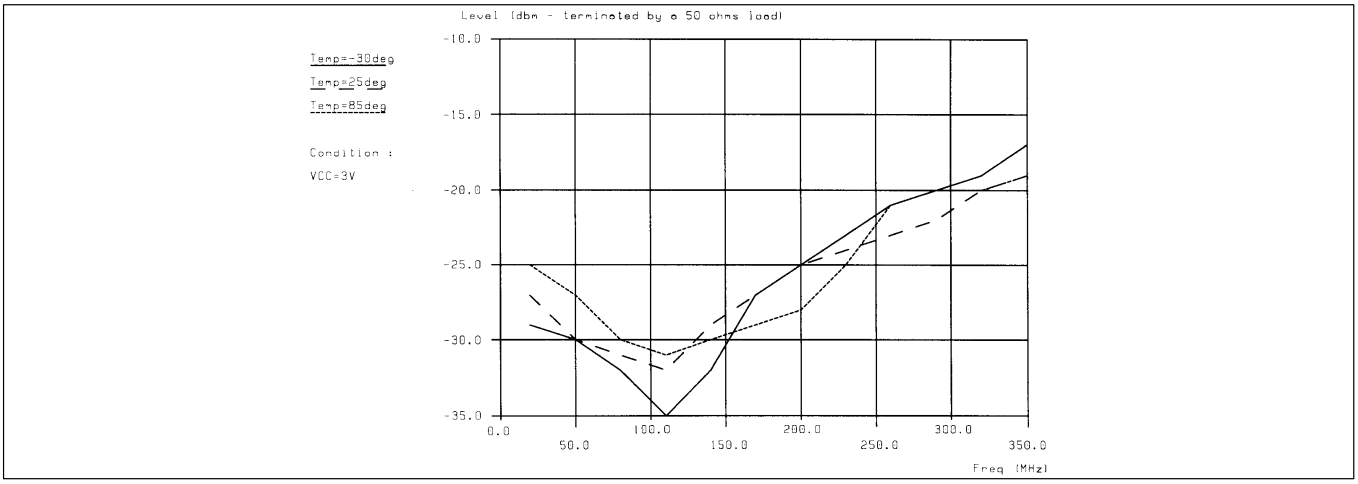


Figure 2–16. Auxiliary Main Divider Input Sensitivity vs Frequency and Temperature

2.4 Main Divider

The RF input drives a preamplifier to provide the clock for the main dividers. The preamplifier has a high input impedance, dominated by pin and pad capacitance. The high frequency sections of the main dividers are implemented using bipolar logic, while the slower sections use lower current CMOS logic. Figures 2–13 to 2–16 show the typical measured input sensitivity of the principal and auxiliary main dividers. Two samples were selected at random, with the device used for frequency versus temperature measurement showing better sensitivity.

2.5 Voltage and Ground Pins

Separate power and ground pins are provided to the analog and digital circuits. To reduce crosstalk between CMOS and bipolar parts, two independent pins supply the digital parts of the integrated circuit (V_{DD1} and V_{DD2}). V_{DD2} pin supplies the principal main divider bipolar section, V_{DD1} pin other digital sections. V_{DD1} and V_{DD2} could be shorted at the pins, however, separate decoupling will be better. The voltages at these pins should be similar.

The ground leads should be externally shorted together otherwise large currents may flow across the die, and damage it.

2.6 In lock Detector

There is a lock detector on-chip for each synthesizer. The lock condition of one, or both loops, can be indicated via an open-drain transistor which drives in-lock detect pin. A pull up resistor must be connected to the output. Whenever a phase difference occurs at the input of a phase detector this produces a pulse that can pass through to the out-of-lock pin (see Figure 2.17).

When integrating the OOL output to convert the pulsed output to a level, a resistor must be added between the OOL pin and the capacitor. This avoids that a current bigger than 400 µA flows through the pin from the capacitor.

The lock output is software selectable as given in Table 2–6 below. Operating principle of out-of-lock is described overleaf.

Table 2–6. Out-Of-Lock Bit Allocations

OLP	OLA	Out-of-Lock Select
0	0	Output disabled
0	1	Auxiliary phase error
1	0	Principal phase error
1	1	Both auxiliary and principal

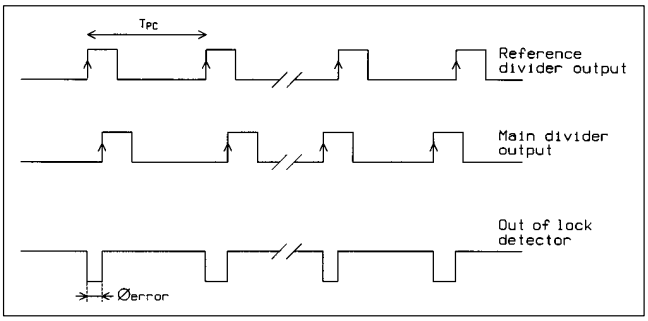


Figure 2–17. Operating Principal of the Out-of-Lock Detector

2.7 Digital-to-Analog Converter

A digital-to-analogue converter is integrated on the UMA1018M and UMA1020M synthesizers.

The DAC output current is scaled by the external resistance R_{ext} at pin I_{SET}, also used by the charge pumps. The nominal full scale current is 2 x I_{SET}. An external user-defined ground referenced resistance connected to the DAC output allows producing a full scale voltage (from 0V to V_{DD1} – 0.4V).

The DAC signal is monotonic across the full range of programmation. A programmed code of 00 corresponds with the minimum DAC leakage current (I_{10min}). It should be less than 5 µA programmed code of 7F corresponds to 2 x I_{SET} x (127 / 128).

The worst monotonic cases occur between 3Fh and 40h, 1Fh and 20h. Here, ΔI measured varies from 0.1 x $\Delta I_{expected}$ to 1.9 x $\Delta I_{expected}$.

Example:

R_{ext} = 12k I_{SET} = 1.2 / 12k = 100 µA
$\Delta I_{expected}$ = I_{SET} x 2 x (3Fh – 40h) / 128 = 1.56 µA
° $\Delta I_{measured}$ can vary between 0.16 µA to 3 µA

The on-board DAC allows adjustment of an external component, such as the central frequency of a VTCXO (Voltage Controlled Temperature Compensated Crystal Oscillator).

3. LOOP FILTER DESIGN

3.1 Basic Loop Filter Design Procedure

This section gives the procedure to ensure a quick and simple loop filter design. The method is based on first order approximations, and provides a working solution without the need for computer simulation. Reading appendices A and B can be useful to clarify some PLL terms and equations of this chapter.

The purpose of a Phase Locked Loop (PLL) in a single loop frequency synthesizer as shown in Figure 3–1 is to transfer the spectral purity and stability of a fixed reference frequency oscillator (TCXO or VTCXO) to that of the Voltage Controlled Oscillator (VCO) output.

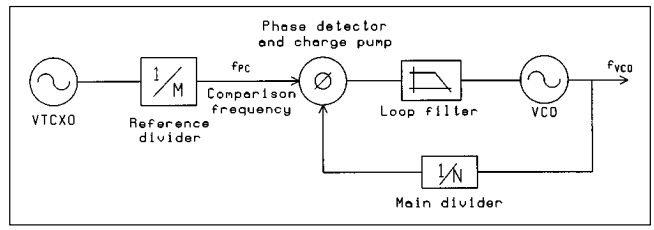


Figure 3–1. Basic Phase Lock Loop Block Diagram

The correct design of the loop filter is of considerable importance to have the optimum performance from the synthesizer. The filter should be designed so as to achieve the required compromise between noise performance and switching time.

Loop filters are usually passive when used with current charge pumps, but can be active if desired. Passive loops have the advantage of reduced noise, fewer parts count and low cost. With UMA1018M or UMA1020M synthesizers, only passive loop filters are necessary. Two common configurations are shown overleaf. The filters in Figure 3–2 are classified in terms of the order of the loop formed.

With the UMA1018M or UMA1020M, the use of the loop filter (a) is often sufficient. For applications requiring further comparison frequency breakthrough rejection, a low pass filter stage (R_3, C_3) can be added. It reduces comparison frequency breakthrough spurs without affecting too much the transient response of the loop when correctly designed.

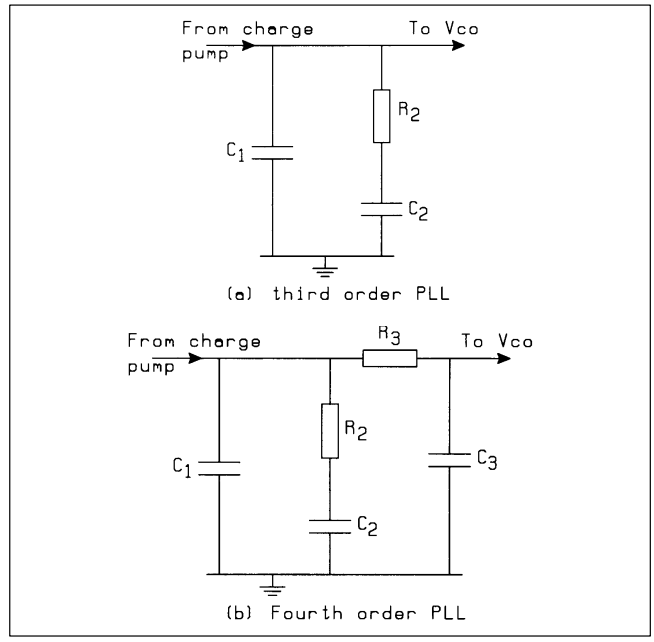


Figure 3–2. Different Types of Passive Loop Filter

Loop parameters are first chosen, they are:

- VCO frequency f_{VCO} (in Hz)
- Phase comparator frequency f_{PC} (in Hz)
- Switching time t_S (in seconds)
- VCO gain K_{VCO} (in Hz/V)

- Phase comparator gain I_{CP} (in amps/cycle)

As the starting point, the equations below are used.

$$W_n = 2 \cdot \Pi \cdot f_n = \left(\frac{K_{VCO} \cdot I_{CP}}{C_2 \cdot N}\right)^{1/2} \quad (1.)$$

$$R_2 = 2 \cdot \rho \left(\frac{N}{(K_{VCO} \cdot I_{CP} \cdot C_2)}\right)^{1/2} \quad (2.)$$

where f_n is the natural frequency (in Hz) and ρ is the damping coefficient.

Calculate the resistor R_{ext} for setting the charge pump output current from

$$R_{ext} = \frac{1.2}{I_{SET}} \quad (3.)$$

I_{CP} is related to I_{SET} according to the relationship given in Table 2–1 and whether the two charge pumps CPP and CPPF are shorted together or not.

Determine the natural frequency f_n

$$f_n = \frac{2.5}{t_S} \quad (4.)$$

It has been found by experience that a good PLL loop filter design takes a switching time (t_S) of less than $2.5/f_n$ to settle to a new frequency. This rule of thumb allows a good compromise between switching time, stability and noise performance when using the UMA1018M and UMA1020M synthesizers. Of course the switching time will also depend on the size of the frequency jump and the definition of when the PLL is settled (i.e., acceptable frequency or phase error with respect to target).

Determine main divider ratio from

$$N = \frac{f_{VCO}}{f_{PC}} \quad (5.)$$

Determine angular velocity W_n (in rad/seconds) from

$$W_n = 2 \cdot \Pi \cdot f_n \quad (6.)$$

Determine C_2 from (1)

$$C_2 = \left(\frac{K_{VCO} \cdot I_{CP}}{W_n^2 \cdot N}\right) \quad (7.)$$

Select damping ratio of approximately 0.9 for a good compromise between switching time and stability.

Determine R_2 from (2)

$$R_2 = 2 \cdot \rho \left(\frac{N}{K_{VCO} \cdot I_{CP} \cdot C_2}\right)^{1/2}$$

Choose C_1 between 1/10 and 1/15 the value of C_2

Determine R_3 from

$$R_3 \geq 2 \cdot R_2 \quad (8.)$$

Determine C3 from

$$C3 < \left(\frac{R_2 \cdot C_2}{20 \cdot R_3}\right) \quad (9.)$$

A program using this cook book method has been written for use on IBM PC (and compatible). It is included with the 3-wire serial bus control software diskette. Values given by the program are approximate and the final values should be optimized. For further optimization, both computer simulation programs, as well as practical experiments, are required.

Capacitors with high leakage currents, such as electrolytic capacitors and capacitors with piezoelectric or delay effects are not preferred because of higher comparison frequency breakthrough and increased switching times. A polyester film capacitor is a good idea for C_2.

3.2 Analysis and Simulation

For analysis, optimization and worst case design of more complex filters, key loops parameters can be entered into a simulation program.

Generally, a stable loop with an acceptable noise performance and a given switching time is needed. Unfortunately, these two requirements are dependent and must be traded off against each other. Stability, being an absolute necessity, gets higher priority. With third order loop filters (see Figure 3–3), the phase margin is the simplest criterion for the stability.

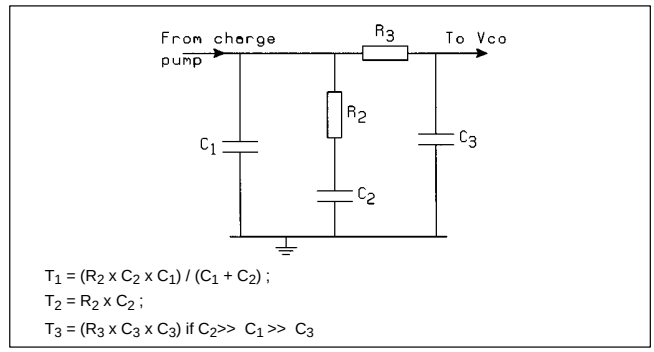


Figure 3–3. Third Order Loop Filter

The phase margin is easily determined from the Bode plot. A Bode plot displays the open loop transfer function magnitude and phase. Figure 3–4 shows Bode plot of a fourth order loop with third order filter (type 3 fourth order system) and a pole in the origin due to the VCO.

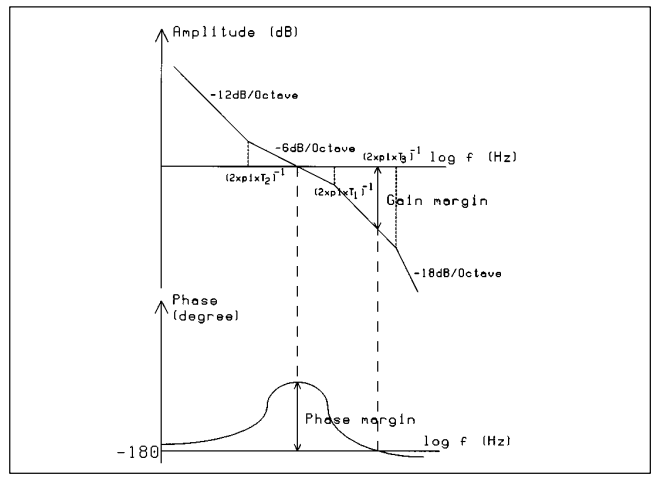


Figure 3–4. Bode Plot 4th Order Open PLL Transfer Function Magnitude and Phase

The phase margin is defined as the difference between 180° and the phase of the open loop transfer function at the frequency where the gain is 1 (gain cross over). The critical point for stability is a phase margin of 0°. The factor by which the system gain would have to be increased for the phase margin to reach the critical value of 0° is called the gain margin.

The time constants in the loop filter are key to controlling the overall loop performance and phase margin. The offset of different time constants can be evaluated from the Bode diagram. The reciprocal of the time constants of the loop filter in Figure 3–3 are the break points in the magnitude plot of Figure 3–4.

When increasing the time constant $T_3 = C_3 \times R_3$, the breakpoint (T_3)–1 will move left and the magnitude curve will start to roll off at a lower frequency. Therefore, the greater the time constant T_3, the better the comparison frequency breakthrough is suppressed. But increasing T_3 will force the point of inflection of the phase margin curve to move to the left as well, this decreasing the phase margin and eventually reducing system stability.

By iteration, inspection of the Bode plot, adjusting the loop filter values and measuring the performance, will yield a compromise between switching time, stability and noise. Simulation programs may give reasonable approximations of PLL behavior, but their accuracy is always limited due to the fact that many practical imperfections and non linearities are not taken into account.

Phase margin between 30° and 70° is required for most applications. The larger the phase margin, the more stable the loop, and the slower the transient response and hence the switching time. A loop with a low phase margin is still stable but may exhibit other problems aside from outright oscillation, low phase margin makes the transient response more oscillatory. A phase margin of 45° is a good compromise between desired stability and the other generally undesired effects.

3.3 Adaptive Loop

Some applications may need to have a dual time constant loop. With two principal charge pumps, UMA1018M and UMA1020M allow this to be implemented. The loop uses both charge pumps for fast frequency switching. Then the phase detector drives just the principal charge pump (CPP) after obtaining the required frequency with a lower bandwidth and hence lower noise. The loop filter used is shown in the Figure 3–5. This filter allows an optimized filter when both charge pumps are ON or when just one charge pump is active.

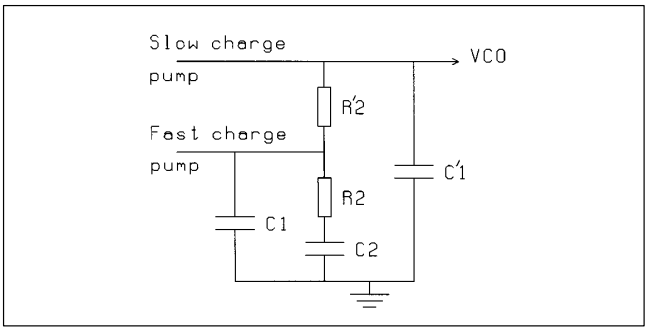


Figure 3–5. Adaptive Loop Filter

The loop filter calculation is given below:

- Use the same design procedure from paragraph 3.2 to calculate the main capacitor C_2, the damping resistor R_2 and the filter capacitor C_1.
- When the fast charge pump CPPF is disabled, loop stability needs to be maintained for the loop which uses only CPP. Recalculate value for the damping resistor with the new value of I_{CP} and ρ = 0.9

$$R'_2 = 2 \cdot \rho \left(\frac{N}{(K_{VCO} \cdot I_{CP} \cdot C_2)} \right)^{1/2} - R_2$$

- Determine C'_1 from

$$C'_1 < \frac{R_2 \cdot C_2}{20 \cdot R'_2}$$

Some precautions must be taken when the principal fast charge pump is switched off. A parasitic capacitor, due to the integrated circuit and the printed circuit board, exists between the FAST and CPPF pins. When the signal is sent to the FAST pin, a coupling through the parasitic capacitance on to the CPPF pin, results in a VCO frequency drift. This problem can he reduced by decreasing the slope of the FAST signal with a RC filter.

3.4 PCB Layout Considerations

With frequency synthesizer layout, good RF design techniques should be employed. To avoid crosstalk between synthesizers (auxiliary and principal), the printed circuit board should have a solid ground plane on the non surface mount side (apart from isolated pads for non-grounded connections to leaded components). On the surface mount side of the board, the ground plane should be designed round each synthesizer, and underneath the Philips integrated circuit so as to provide maximum isolation between two PLLs. A good number of plated-through holes must connect the two layers of the ground plane.

Suitable high frequency capacitors (100 nF) in series with a small value resistor (12Ω) should be used for power supply decoupling. V_{DDI} and V_{DD2} can be shorted at the output of the integrated circuit. However, separate decoupling to Pins 4 and 5 will be better. It is very important to de-couple as close as possible to Pins 4 and 5.

3.5 Worked Example

In this chapter, a design example based on the fourth order PLL for GSM specification is shown. Only the loop filter of the UMA1018M principal synthesizer is calculated.

Experiments show that the use of just one charge pump gives better close in noise (about 3dBc/Hz) than two enabled charge pumps with outputs (CPPF + CPP) connected together. Because slow charge pump is better (about 1 dBc/Hz) than fast charge pump, only the slow charge pump is used in this worked example. The fast charge pump is switched off via pin FAST.

- VCO Frequency f_{VCO} = 902MHz
- Phase comparator frequency f_{CP} = 200kHz
- Switching time t_S = 600µs
- VCO gain K_{VCO} = 11MHz/V
- Phase comparator gain I_{CP} = 0.4mA with CR1 bit set to 0 and CR0 bit set to 0. Pins CPP and CPPF connected together. Fast charge pump is switched off by the pin FAST. Following the basic design procedure from paragraph 3.2 yields:

I_{CP} = 0.4mA = 4 x I_{SET} → I_{SET} = 100µA
R_{ext} = 1.2 / I_{SET} = 1.2 / 100µA = 12kΩ
Natural frequency f_n = 2.5 / t_S = 2.5 / 600µS = 4170Hz
Main divider ratio N = f_{VCO} / f_{CP} = 902MHz / 200kHz = 4510

Low power single/dual frequency synthesizers: UMA1017M/1018M/1019M(AM)/1020M(AM)

AN95102

The main components in the loop filter are:

main capacitor C_2 $= K_{VCO} \times I_{CP} / W_n^2 \times N$
$= 11MHz \times 0.4mA / (2 \times 11 \times 4170)^2 \times 4510$
$= 1.5nF$

damping resistor R_2 $= 2 \times \rho\ (N / K_{VCO} \times I_{CP} \times C_2)^{1/2}$
$= 2 \times 0.9\ (45101 / 11MHz \times 0.4mA \times 1.5nF)_{1l2}$
$= 47k\Omega$

filter capacitor $C_2 / 15 \leq C_1 \leq C_2 / 10$ $C_1 = 100pF$

$R_3 \geq 2 \times R_2$ $R_3 = 100k\Omega$

$C_3 < (R_2 \times C_2 / 20 \times R_3)$ $C_3 = 22pF$

A software simulation program has been used to verify the stability of this loop filter. The phase margin is maximum and equal to 52° at the gain cross-over point. The requirement for basic loop stability is fulfilled (see Figure 3–6).

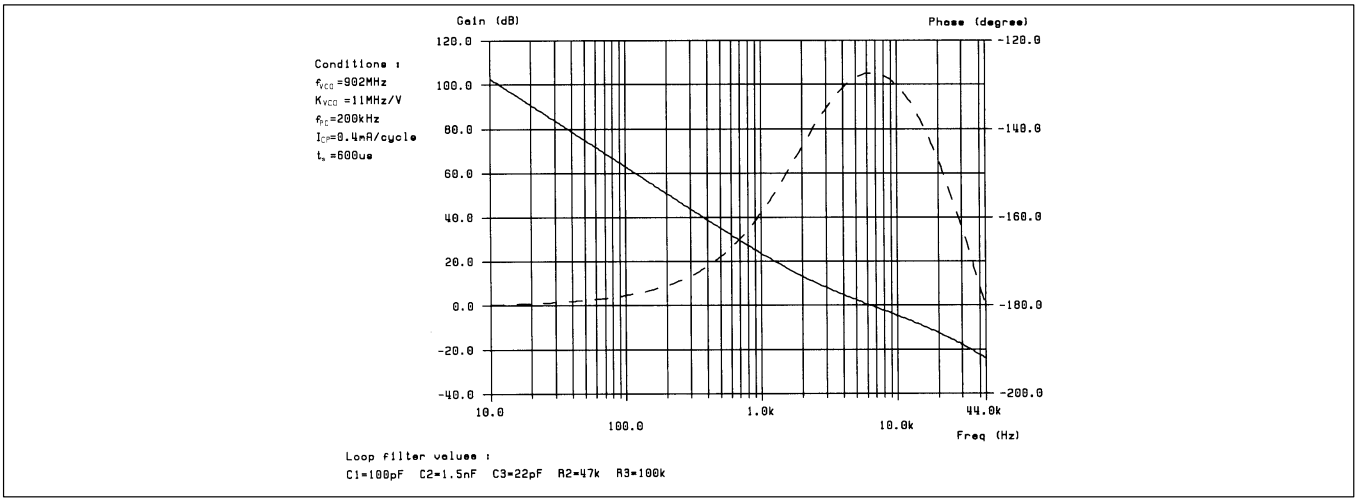


Figure 3–6. Simulated Bode Plot of 4th-Order Open Loop Transfer Function of UMA1018M Principal Synthesizer, Magnitude and Phase vs Frequency

The design procedure is similar with the auxiliary synthesizer and with the UMA1020M for the DCS1800 application. Results are summarized in Table 3–1 and 3–2.

Table 3–1. Design Parameters and Simulation for UMA1018M Dual Synthesizer

Parameter		Principal synthesizer	Auxiliary synthesizer
Loop components (refer to figure 3.3) VCO		C_1 = 100p C_2 = 1.5n C_3 = 22p R_2 = 47k R_3 = 100k	C_1 = 470p C_2 = 10n C_3 = 100p R_2 = 18k R_3 = 39k
VCO gain K_{VCO} VCO frequency f_{VCO}		11MHz/V 902MHz	2.5MHz/V 100MHz
Comparison frequency f_{PC}		200kHz	100kHz
Charge pump	Current gain I_{CP}	0.4mA/cycle	0.4mA/cycle
	R_{ext}	12k	
	Bits CR0, CR1	CR0 = 0, CR1 = 0	
Reference frequency VTCXO		13MHz	
Unity gain phase margin (simulated)		52.6 deg	58.9 deg
Gain margin at 180 deg phase margin (simulated)		24dB	27dB
Unity gain loop bandwidth (simulated)		6.3k	2.8k
Natural frequency (simulated)		4.1k	1.6k
Switching time for a 25MHz step ; freq error < 1kHz (simulated)		540µs	

Table 3–2. Design Parameters and Simulation for UMA1020M Dual Synthesizer

Parameter		Principal synthesizer	Auxiliary synthesizer
Loop components (refer to figure 3.3) VCO		C_1 = 820p C_2 = 13n C_3 = 180p R_2 = 5.6k R_3 = 15k	C_1 = 470p C_2 = 10n C_3 = 100p R_2 = 18k R_3 = 39k
VCO gain K_{VCO} VCO frequency f_{VCO}		20MHz/V 1890MHz	2.5MHz/V 100MHz
Comparison frequency f_{PC}		200kHz	100kHz
Charge pump	Current gain I_{CP}	3.6mA	0.4mA
	R_{ext}	12k	
	Bits CR0, CR1	CR0 = 1, CR1 = 0	
Reference frequency VTCXO		13MHz	
Unity gain phase margin (simulated)		53.2 deg	58.9 deg
Gain margin at 180 deg phase margin (simulated)		25dB	27dB
Unity gain loop bandwidth (simulated)		6.45k	2.8k
Natural frequency (simulated)		3.8k	1.6k
Switching time for a 25MHz step ; freq error < 1kHz (simulated)		550µs	

4. MEASUREMENTS AND TYPICAL RESULTS

This section describes the performance of the UMA1018M and UMA1020M demoboards with the loop filters indicated in Table 3–1 and 3–2.

The relevant performance criteria for a synthesizer are usually:

- Close in phase noise
- Comparison frequency breakthrough
- Switching time
- Integrated phase jitter

Close in noise was measured using a direct reading from the spectrum analyzer and referred to 1Hz bandwidth. This is normally done at a given offset from the carrier while still inside the loop bandwidth.

Integrated phase jitter was measured on a Rohde and Schwartz Modulation Analyzer in a 10Hz to 200kHz audio bandwidth.

Tables 4–1 to 4–3 summarize the measurement results. Figures 4–1 to 4–8 show some of the actual measurements. During the measurements both synthesizers were enabled and locked.

Table 4–1. Demoboard Measurement Results on UMA1018M Principal Synthesizer

VCO supply voltage : 5 volts Both synthesizers enabled UMA1018M supply voltage : 5 volts Temperature=25°C		Principal synthesizer
VCO frequency range		890MHz - 915MHz
Comparison frequency breakthrough	at 200kHz	- 81dBc
	at 400kHz	- 82dBc
	at 600kHz	< -82dBc
Switching time for frequency jump around centre frequency to within 1kHz of the target frequency	200kHz (1 channel)	450µs
	10MHz	500µs
	25MHz (max jump)	580µs
Close in noise (at 1kHz distance from carrier)		-78dBc/Hz
Integrated phase jitter		18 mrad rms

Table 4–2. Demoboard Measurement Results on UMA1020M Principal Synthesizer

VCO supply voltage : 3 volts Both synthesizers enabled UMA1020M supply voltage : 3 volts Temperature=25°C		Principal synthesizer
VCO frequency range		1878MHz - 1903MHz
Comparison frequency breakthrough	at 200kHz	- 77dBc
	at 400kHz	- 81dBc
	at 600kHz	< -82dBc
Switching time for frequency jump around centre frequency to within 2kHz of the target frequency	200kHz (1 channel)	370µs
	10MHz	430µs
	25MHz (max jump)	540µs
Close in noise (at 1kHz distance from carrier)		-70dBc/Hz
Integrated phase jitter (Obtained by integration of close in noise)		53 mrad rms

Table 4–3. Demoboard Measurement Results on Auxiliary Synthesizer

VCO supply voltage : 5 volts Both synthesizers enabled UMA1018M supply voltage : 5 volts Temperature=25°C		Auxiliary synthesizer
VCO frequency		97MHz - 104MHz
Comparison frequency breakthrough	at 100kHz	- 77dBc
	at 200kHz	- 80dBc
	at 400kHz	< -82dBc
Close in noise (at 2kHz from carrier)		-83dBc/Hz
Integrated phase jitter		6 mrad rms

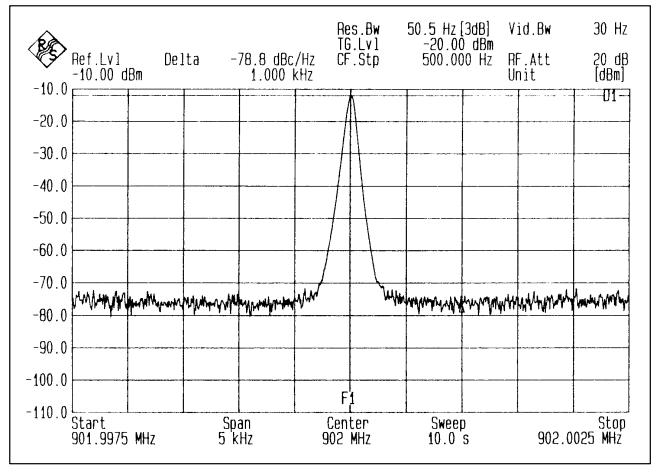


Figure 4–1. UMA1018M Principal Synthesizer Output Spectrum – Close in Noise

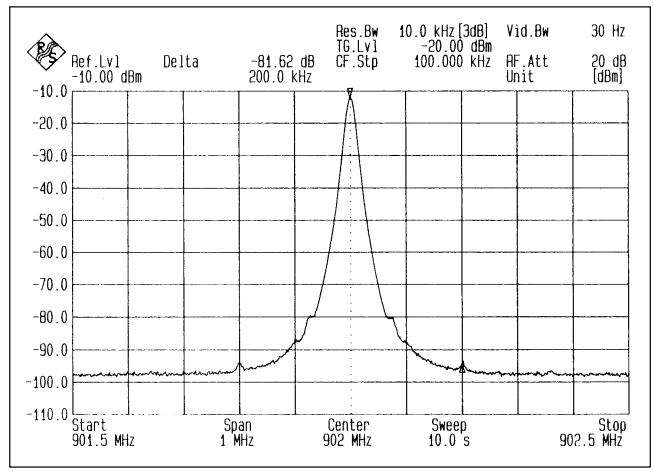


Figure 4–2. UMA1018M Principal Synthesizer – Comparison Frequency Breakthrough

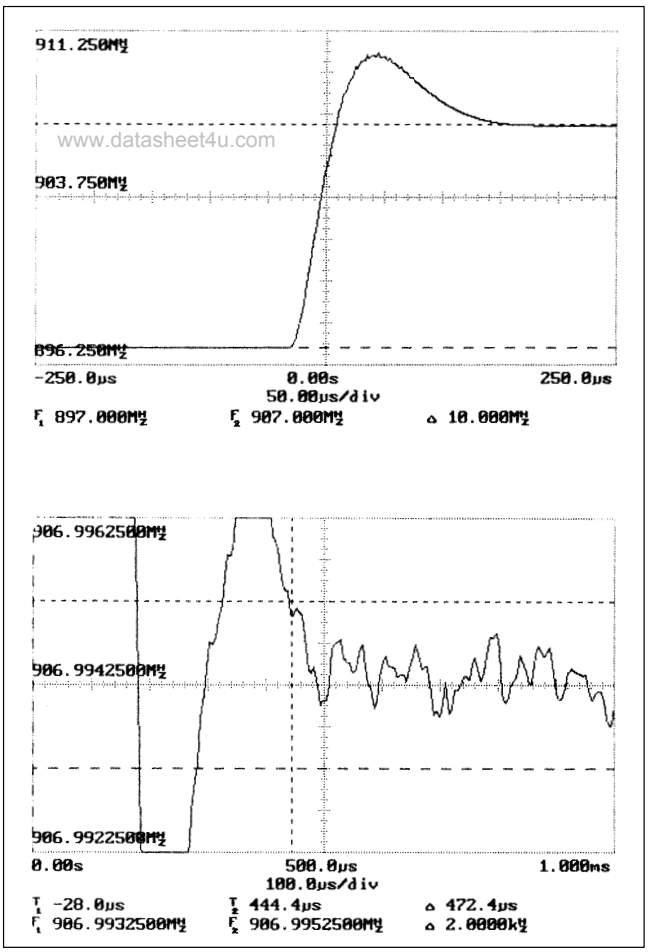


Figure 4–3. UMA1018M Principal Synthesizer – Settling Time for a 10MHz Step

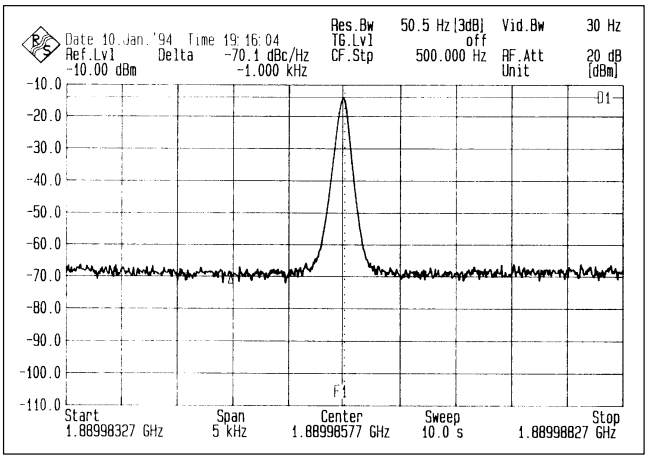


Figure 4–4. UMA1020M Principal Synthesizer Output Spectrum – Close in Noise

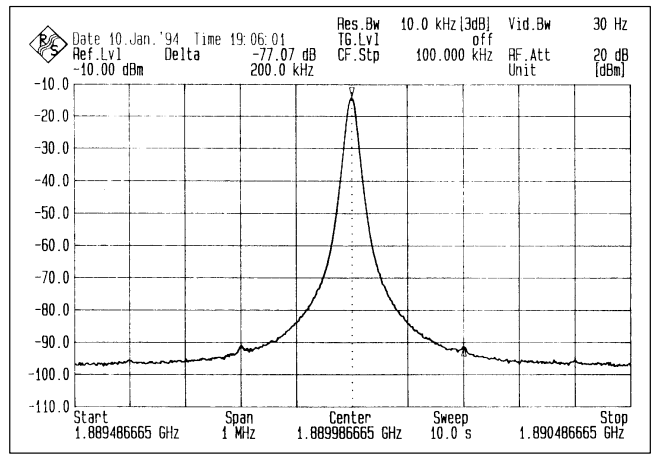


Figure 4–5. UMA1020M Principal Synthesizer – Comparison Frequency Breakthrough

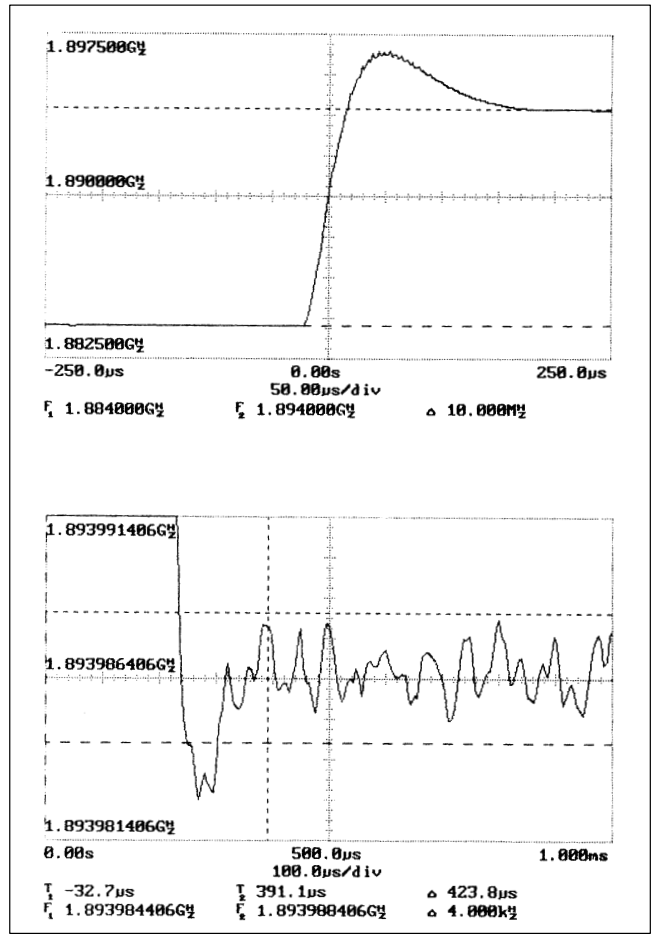


Figure 4–6. UMA1020M Principal Synthesizer – Settling Time for a 10MHz Step

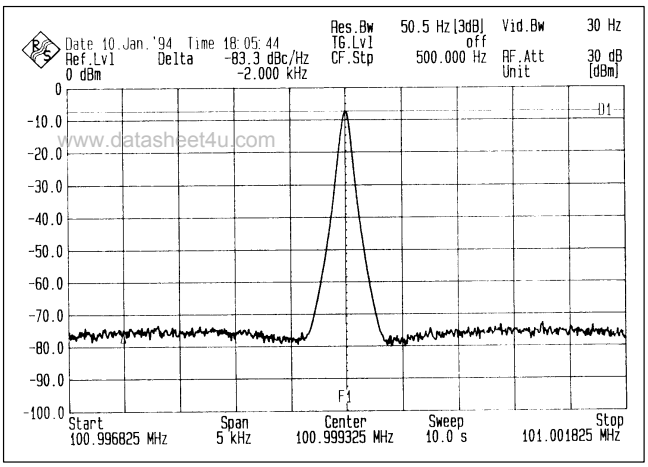


Figure 4–7. UMA1020M Auxiliary Synthesizer Output Spectrum – Close in Noise

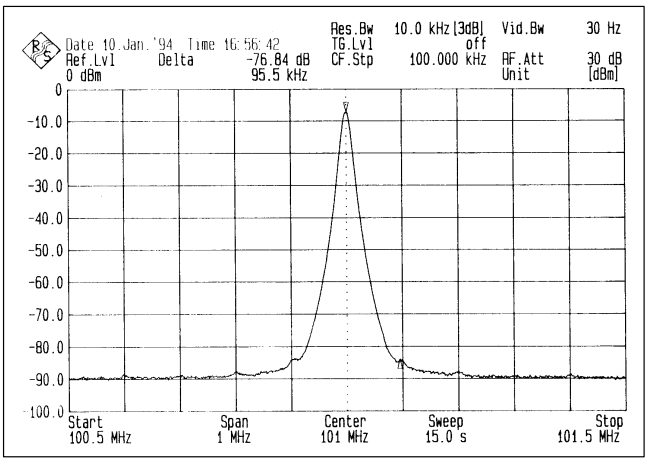


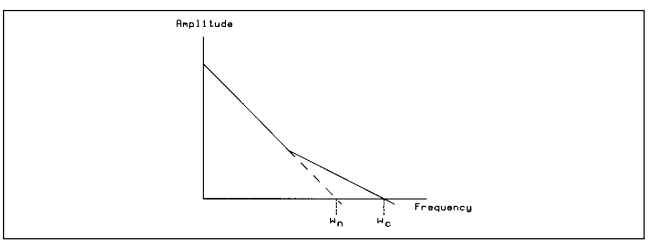
Figure 4–8. UMA1018M Auxiliary Synthesizer – Comparison Frequency Breakthrough

5. APPENDICES

5.1 Appendix A: PLL Terms

The following is a brief glossary of frequently encountered terms in PLL literature.

- **Natural frequency w_n**: the natural frequency of the loop. This is the frequency at which the loop would theoretically oscillate if the damping factor were zero.
- **Open loop cross-over frequency w_C**: this is the frequency at which the open loop gain is unity. It is useful in determining the phase margin and hence the stability.



- **Damping coefficient**: ρ can be used as a measure of the stability in second order systems. It is seldom used as a direct measure of stability in higher order designs.
- **Order of loop**: the order of the loop is the highest power of s (s=jw) in the denominator of the open loop transfer function. The example below shows a second order loop.

  $G(s) \times H(s) = (K_{VCO} \times I_{CP}) \times (s \times T_2 + 1) / (N \times C \times s^2)$
- **Type of loop**: the type of control system formed is defined by the number of perfect integrators in the loop. In the example, above, the loop is a type two system.
- **Phase margin Φm**: The phase margin, in degrees, is expressed as $\Phi m = \Phi(w_C) + 180$ where $\Phi(w_C)$ is the open loop phase shift at the frequency w_C
- **SSB phase noise or close in noise**: It is the noise level within the loop bandwidth relative to carrier at a given frequency offset. It is referred to a 1Hz bandwidth. It is expressed in dBc/Hz.
- **Integrated phase jitter or residual FM**: this is another measure of the noise performance of a signal source. This measure of integrated noise is usually specified over a particular audio bandwidth, e.g., 10 Hz to 200 kHz. It is expressed in degrees rms. An ideal synthesizer would have zero integrated phase jitter.
- **Spurious**: this defines the spectral purity of the oscillator. Common sources of spurious are the comparison frequency and harmonies. Comparison frequency breakthrough is generated by leakage in the loop filter components or the charge pump.
- **Settling time or switching time**: this indicates the time for a given frequency jump to be within a specified distance (frequency or phase) from target value.

5.2 Appendix B: Basic PLL Transfer Function

Figure 5–1 shows the block diagram of a basic control loop.

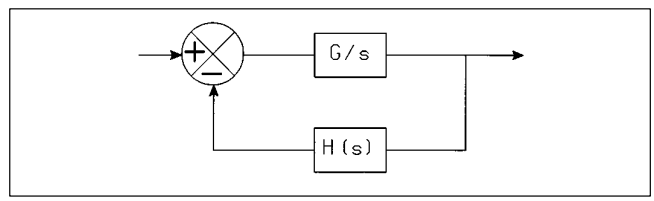


Figure 5–1. Block Diagram of a Loop

In open loop, the transfer function is

$$H(s) \cdot G(s) \quad \text{(a)}$$

In closed loop, the transfer function is

$$\frac{G(s)}{1 + G(s) \cdot H(s)} \quad \text{(b)}$$

If we apply these transfer functions to the Phase Locked Loop in Figure 5–2 with equations expressed in Laplace notation

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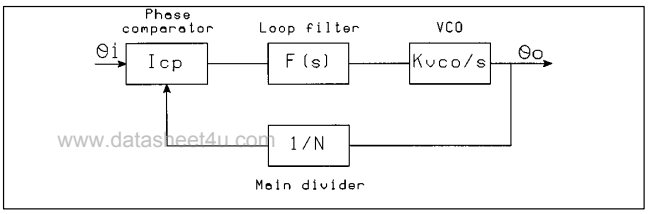

Figure 5–2. Block Diagram of a Phase Locked Loop

$$G(s) = \frac{I_{CP} \cdot K_{VCO} \cdot F(s)}{s} \quad (c)$$

$$H(s) = \frac{1}{N} \quad (d)$$

The PLL open loop transfer function is

$$\frac{I^{CP} \cdot K_{VCO} \cdot F(s)}{s \cdot N} \quad (e)$$

The PLL closed loop transfer function is

$$\frac{\Phi o(s)}{\Phi(s)} \frac{K_{VCO} \cdot I_{CP} \cdot F(s)/s}{1 + (K_{VCO} \cdot I_{CP} \cdot F(s)/s \cdot N)}$$

$$= \frac{N \cdot K_{VCO} \cdot I_{CP} \cdot F(s)}{(s \cdot N) + (K_{VCO} \cdot I_{CP} \cdot F(s)} \quad (f)$$

Basic performance of PLL is determined by R_2 and C_2 (see Figure 3–2) in the loop filter.

Note: when introducing more components in the loop filter, the expression for the transfer function becomes a lot more complicated. Anyway, this design can serve as a starting point for even more complicated filters.

The transfer function of this simple loop filter is

$$F(s) = R_2 + \left(\frac{1}{s \cdot C_2}\right) = \left(\frac{(s \cdot R_2 \cdot C_2) + 1}{(s \cdot C_2)}\right) \quad (g)$$

Then, the closed loop transfer function is

$$\frac{\Phi o(s)}{\Phi i(s)} = \frac{N \cdot K_{VCO} \cdot I_{CP} \cdot F(s)}{s \cdot N + K_{VCO} \cdot I_{CP} \cdot F(s)} =$$

$$\frac{N \cdot K_{VCO} \cdot I_{CP}(s \cdot R_2 \cdot C_2 + 1)/s \cdot C_2}{s \cdot N + K_{VCO} \cdot I_{CP}(s \cdot R_2 \cdot C_2 + 1)/s \cdot C_2} =$$

$$\frac{N(s \cdot R_2 \cdot C_2 + 1)}{\frac{s^2 (C_2 \cdot N)}{(K_{VCO} \cdot I_{CP})} + (s \cdot R_2 \cdot C_2 + 1} \quad (h)$$

If we compare the denominator of (h) with

$$\frac{s^2}{w_n^2} + \frac{2 \cdot \rho \cdot s}{W_n} + 1$$

we find the equations shown below:

$$w_n = \left(\frac{K_{VCO} \cdot I_{CP}}{C_2 \cdot N}\right)^{1/2} \quad (i) \rightarrow (1)$$

$$\rho = \frac{w_n (R_2 \cdot C_2)}{2} \quad (j)$$

$$R_2 = 2 \cdot \rho \left(\frac{N}{K_{VCO} \cdot I_{CP} \cdot C_2}\right)^{1/2} \quad (k) \rightarrow (2)$$

5.3 APPENDIX C: DEMONSTRATION BOARD DOCUMENTATION

Table 5–1 Parts List for UMA1018M/UMA1020M Demonstration Board (GSM/DCS1800)

Reference	Value / Type	Size	Reference	Value / Type	Size
R1	560kΩ	0805 SMD	C1	33pF	0805 SMD
R2	560kΩ	0805 SMD	C2	33pF	0805 SMD
R3	560kΩ	0805 SMD	C3	33pF	0805 SMD
R4	12kΩ	0805 SMD	C4	56pF	0805 SMD
R5	56Ω	0805 SMD	C5	56pF	0805 SMD
R6	18Ω	0805 SMD	C6	560pF	0805 SMD
R7	18Ω	0805 SMD	C7	100pF	1206 SMD
R8	12Ω	0805 SMD	C8	47µ / 25V	Alu 5x11
R9	12Ω	0805 SMD	C9	470pF	0805 SMD
R10	18kΩ	0805 SMD	C10	10nF	0805 SMD
R11	39kΩ	0805 SMD	C11	100pF	0805 SMD
R12	12Ω	0805 SMD	C12	100nF	1206 SMD
R13	100kΩ	0805 SMD	C13	–	
R14	3k9	0805 SMD	C14	100pF (820pF)	0805 SMD
R15	100kΩ	0805 SMD	C15	–	0805 SMD
R16	–		C16	1.5nF (12n//1n)	0805 SMD
R17	–(12)	0805 SMD	C17	22pF (180pF)	0805 SMD
R18	0	0805 SMD	C18	100nF	1206 SMD
R19	47kΩ (5k6)	0805 SMD	C19	100nF	1206 SMD
R20	100kΩ (15kΩ)	0805 SMD	C20	56pF	0805 SMD
R21	12kΩ	0805 SMD	C21	56pF	0805 SMD
R22	12kΩ	0805 SMD	C22	100nF (–)	1206 SMD
R23	56Ω	0805 SMD	C23	47µ / 25V	Alu 5x11
R24	18Ω	0805 SMD	C24	1nF	0805 SMD
R25	18Ω	0805 SMD	C25	10nF	0805 SMD
R26	18Ω	0805 SMD	C26	22nF	0805 SMD
R27	12 (–)	0805 SMD	C27	100nF	1206 SMD
R28	100kΩ	0805 SMD	C28	100nF	1206 SMD
R29	22kΩ	0805 SMD	C29	100nF	1206 SMD
R30	1k8	0805 SMD	C30	1µ / 63V	Alu 5x11
R31	1k2	0805 SMD	C31	–(100nF)	1206 SMD
R32	–	0805 SMD	D1	LED	
R33	12	0805 SMD	L1	4.77nF	1008CT
R34	–(12)	0805 SMD	78L05		T092
VCO1	MQC505-902	MURATA	LM317LZ		T092
VCO2	(URAE8x542A)	ALPS	FXTLIN	PN-Minicoax-Bus SMB	
VCO3	Aux. VCO		RF_PRI	PN-Minicoax-Bus SMA	
VTCX01	13MHz	B8 Philips	RF_AUX	PN-Minicoax-Bus SMB	
VCTX02	13MHz	B9 Philips			

NOTE: All values in between brackets ( ) are related to 1800MHz application.

J1 Controls power down auxiliary synthesizer
J2 Activates the FAST charge pump
J3 Controls power down principal synthesizer
J4 Enables DAC output
J5 Selects VTCXO or external reference frequency
J6 Selects 3V, 5V or external variable voltage
J7 Disconnects the auxiliary VCO
X1 3-Wire bus control
X2, X4 Supply
X3 Modulation

Table 5–2 Parts List for Interface Card and Auxiliary VCO

Reference	Value / Type	Size	Reference	Value / Type	Size
Components for the Auxiliary VCO 100 MHz					
Rf1	27Ω	0805 SMD	Cf1	1pF	0805 SMD
Rf2	150Ω	0805 SMD	Cf2	27pF	0805 SMD
Rf3	1kΩ	0805 SMD	Cf3	68pF	0805 SMD
Rf4	820Ω	0805 SMD	Cf4	–	0805 SMD
Rf5	1kΩ	0805 SMD	Cf5	22pF	0805 SMD
Rf6	1kΩ	0805 SMD	Cf6	33nF//22pF	0805 SMD
Rf7	10kΩ	0805 SMD	Cf7	3p3	0805 SMD
Rf8	100Ω	0805 SMD	Cf8	3p9	0805 SMD
Rf9	270Ω	0805 SMD	Cf9	10pF	0805 SMD
Rf10	82Ω	0805 SMD	Cf10	15pF	0805 SMD
Lf1	120nF	0805 SMD	Cf11	1pF	0805 SMD
Lf2	180nF	0805 SMD	Cf12	8n2	0805 SMD
CVf1	BBY31	SOT-23	Tf1	BFT92	SOT-23
			Tf2	BFR92	SOT-23
Components for PC Interface Card					
R1	10kΩ	0805 SMD	C1	100nF	1206 SMD
R2	10kΩ	0805 SMD	IC1	74HC04	
R3	10kΩ	0805 SMD	J1	Sub D 25 pins	
R4	330Ω	0805 SMD	X1	6 pins	
R5	330Ω	0805 SMD			
R6	330Ω	0805 SMD			

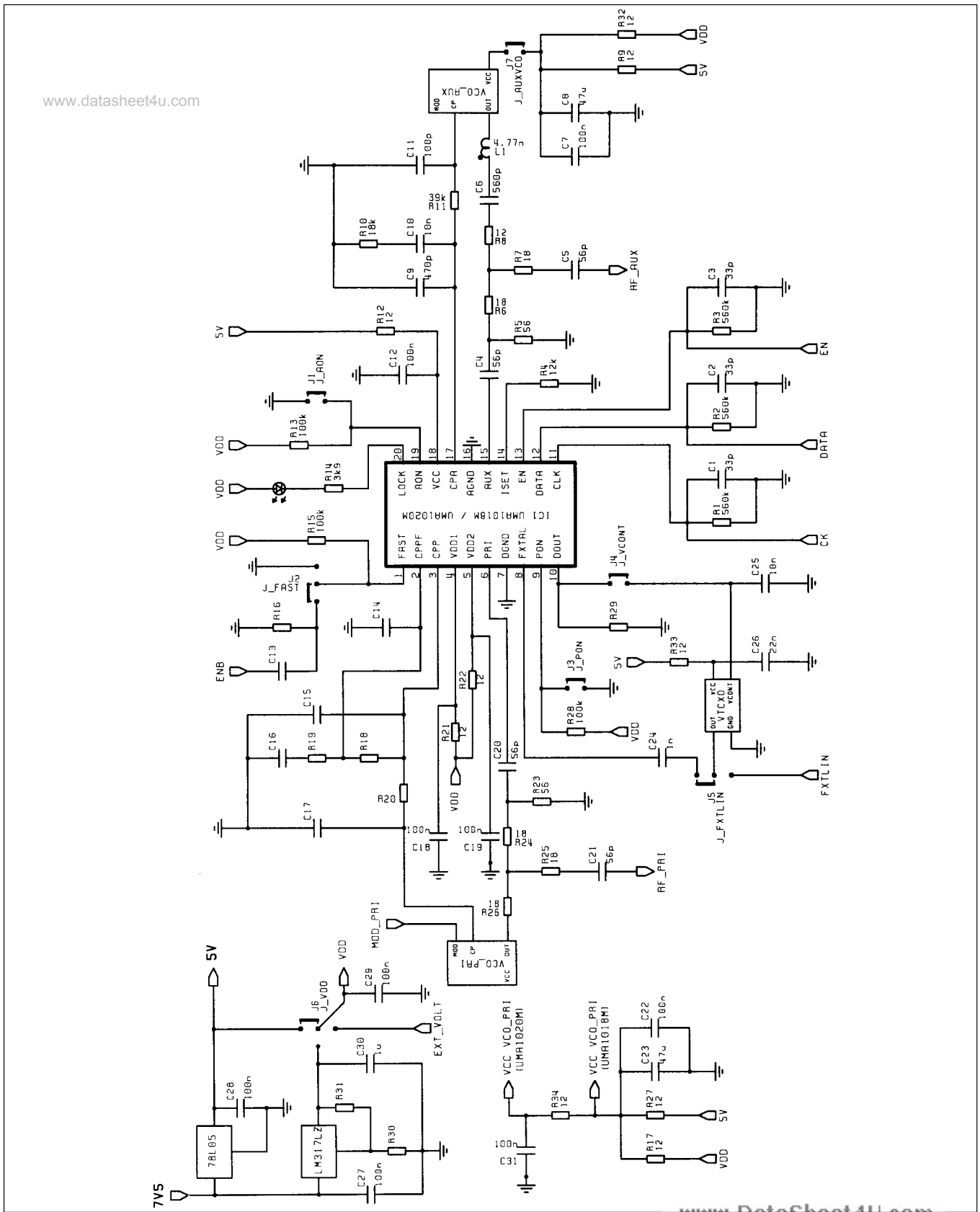

Figure 5–3. Demonstration Board Circuit Diagram

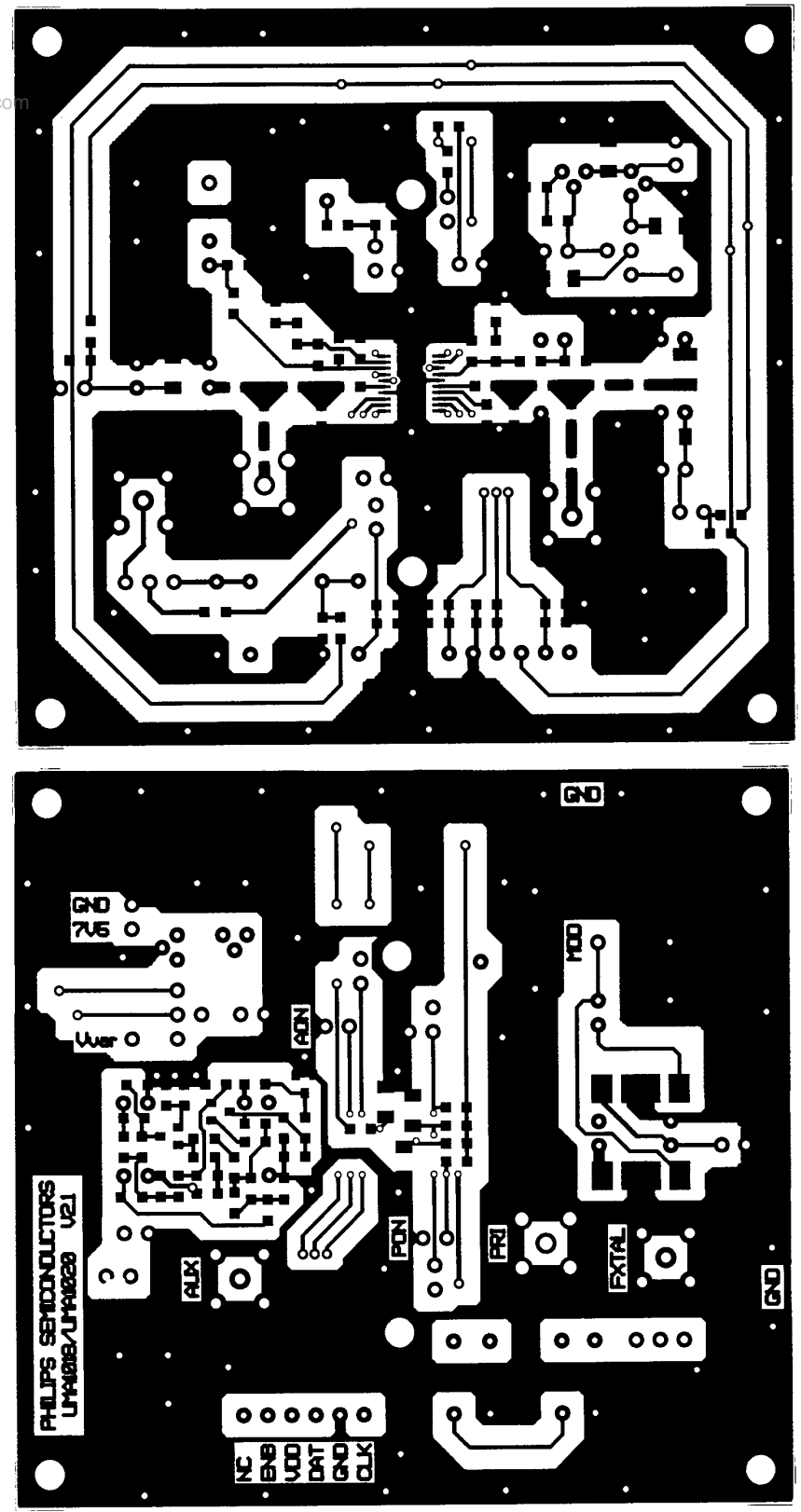

Figure 5–4. Demonstration Board PCB Layout

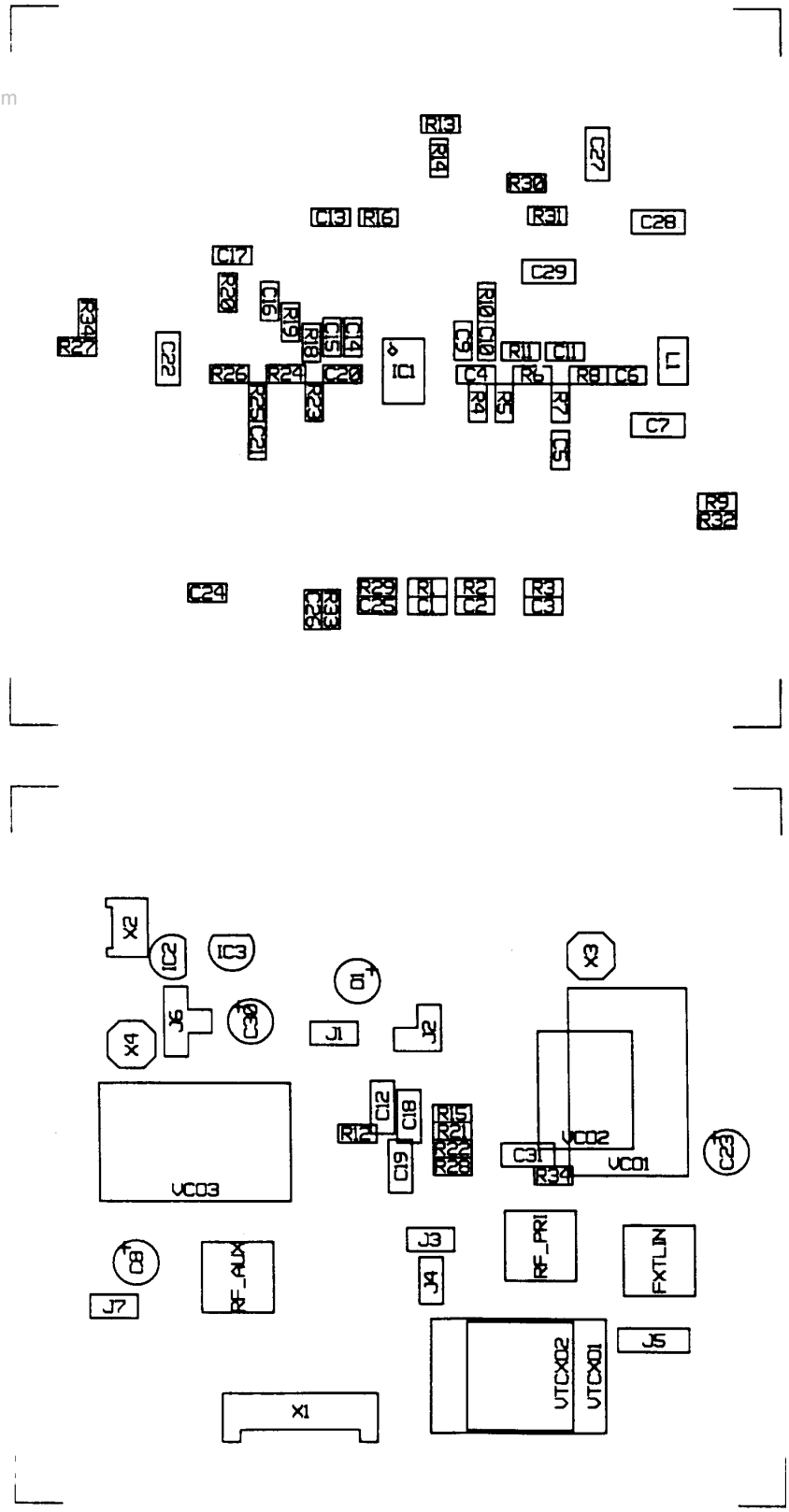

Figure 5–5. Demonstration Board Placement of Components

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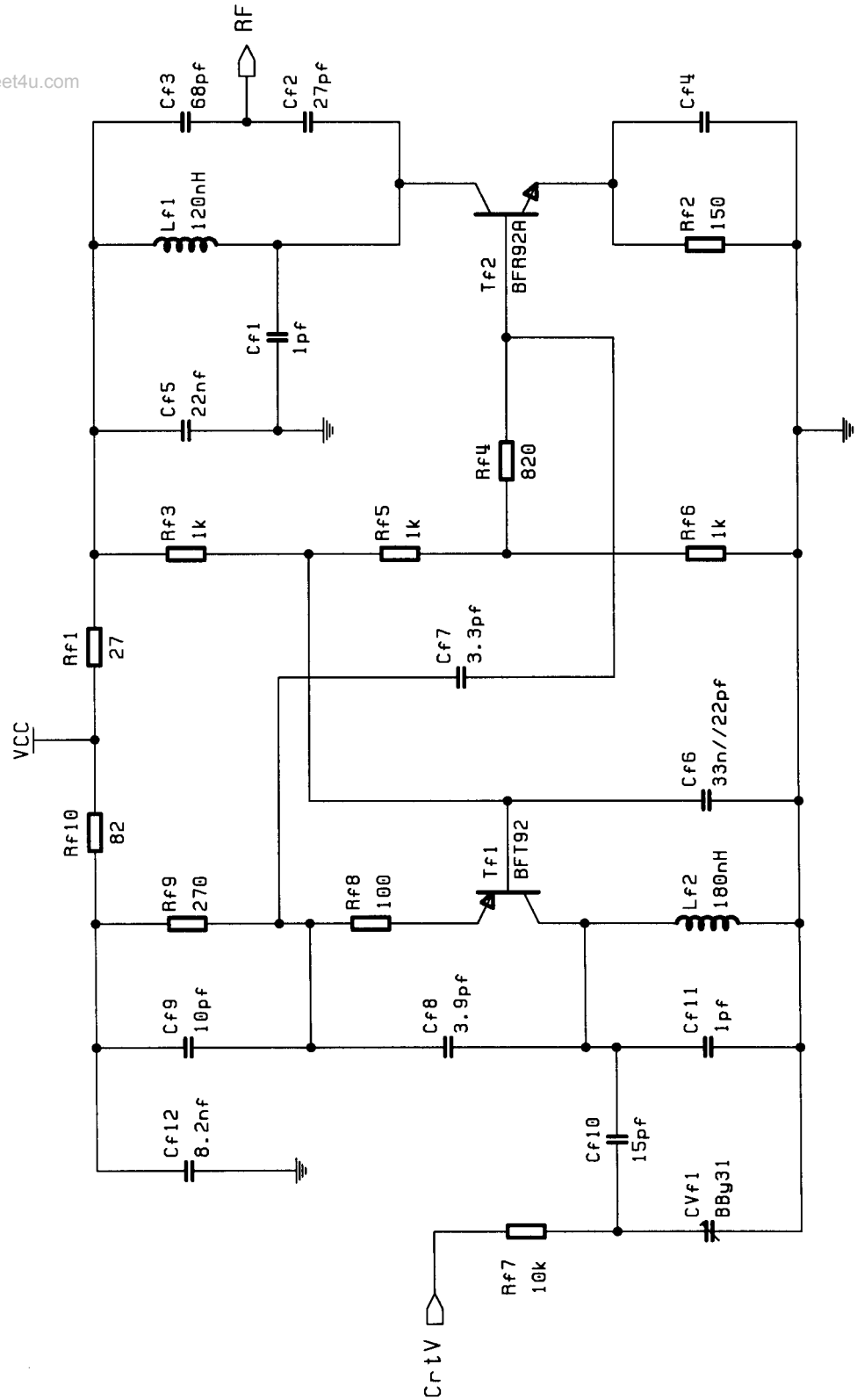
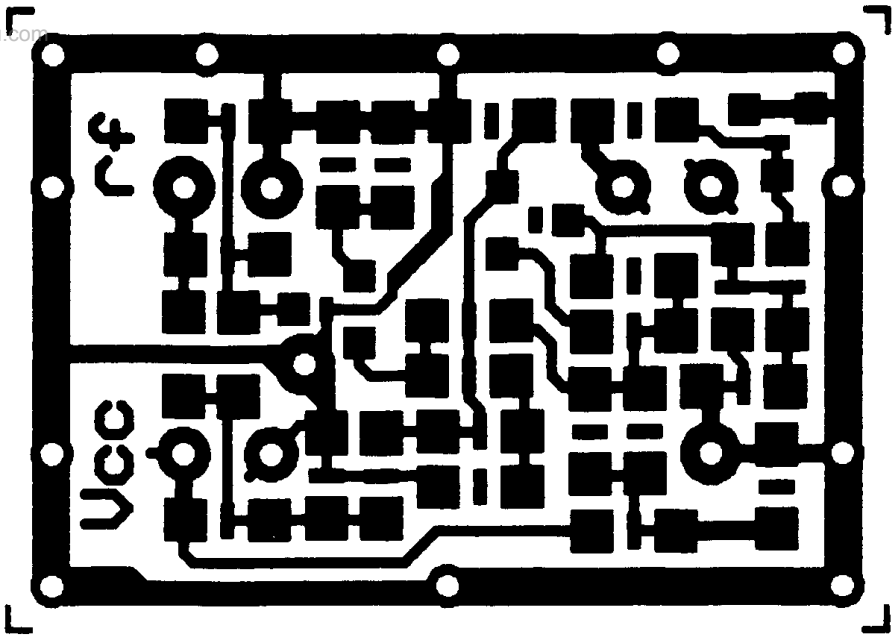


Figure 5–6. Auxiliary 100MHz VCO Circuit Diagram



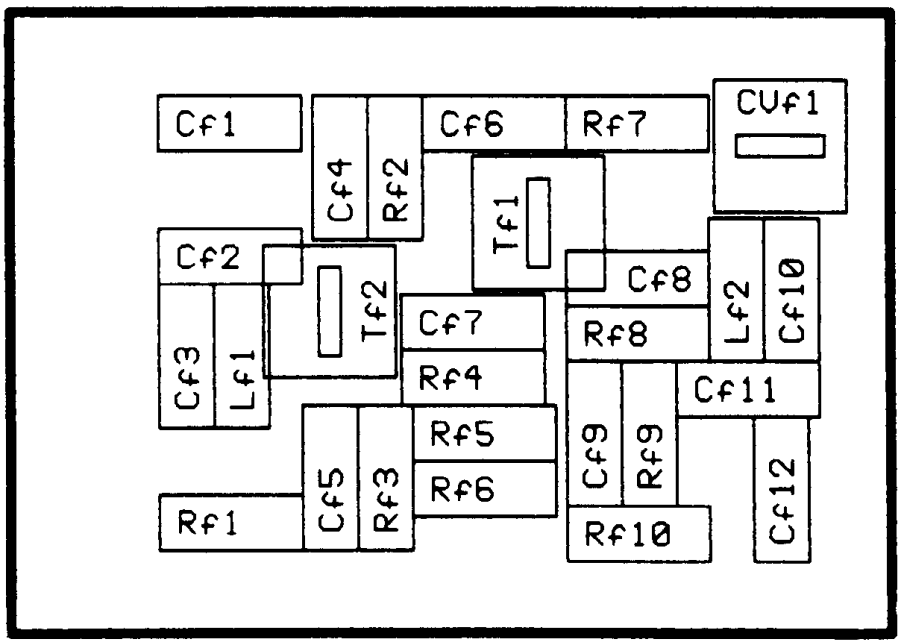
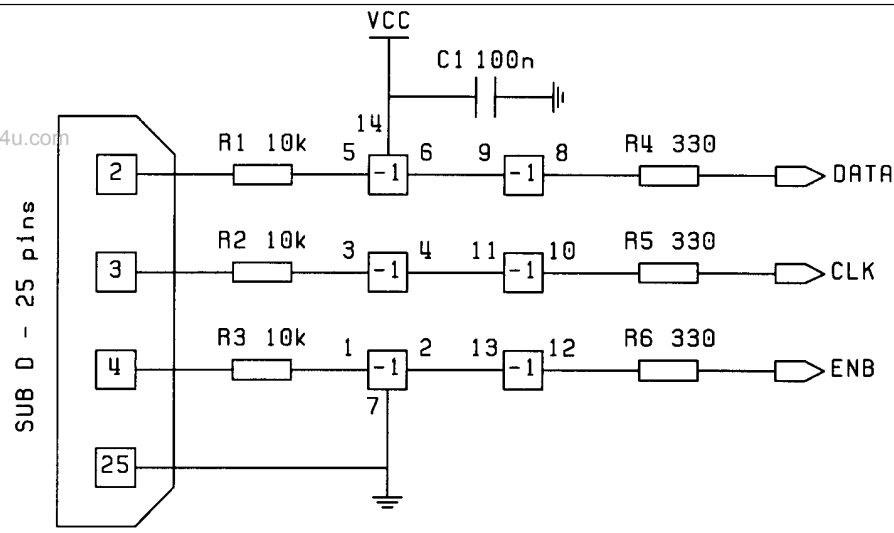
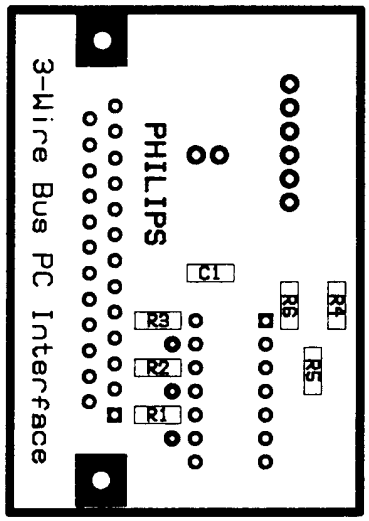
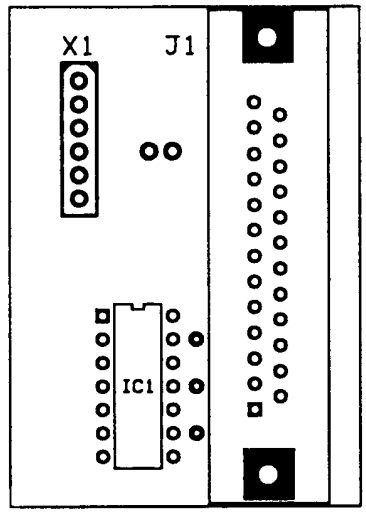


Figure 5–7. Auxiliary 100MHz VCO PCB Layout and Placement of Components







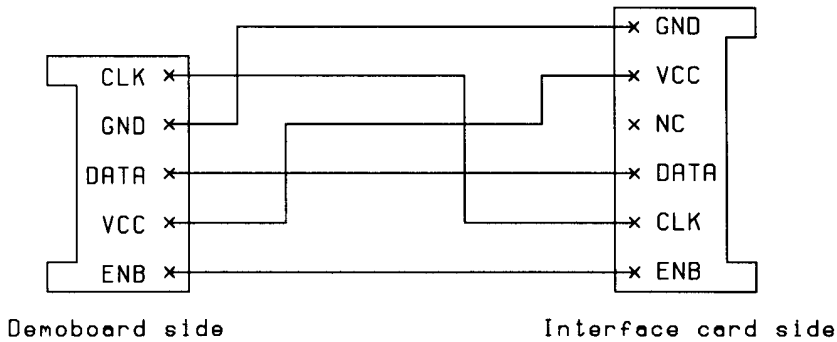


Figure 5–8. Interface Card PCB Layout and Cable Connection

6. FREQUENTLY ASKED QUESTIONS

Q. How can the noise be improved?

A. Five things can be done to improve the noise:

1. Increase the f_{XTAL} level (within specification limits).
2. Use a higher crystal frequency. Doubling the reference frequency improves the close in noise by 3dBc/Hz.
3. Use only one charge pump (CPP or CPPF). The dynamic gain is more constant with supply voltage, frequency and temperature.
4. Use a narrower loop filter. But this increases the switching time.
5. Ensure that supply is well decoupled.

Number 4 does not improve the close in noise, just the phase noise. Other points can improve the close in noise and so, the total phase noise of the PLL.

Q. What is the phase detector gain? Is it charge pump output current divided by 2π or just the charge pump output current, itself?

A. The phase detector gain is equal to the charge pump output current I_{CP} divided by 2π since the phase detector covers 2π range. However, when using the design formulas, the phase detector gain can be replaced directly by I_{CP} because the 2π factor will be cancelled out by the 2π also in the VCO gain.

Q. What kind of main capacitor should be used in the loop filter?

A. Higher leakage current raises comparison frequency breakthrough and the 'memory effect' of higher dielectric capacitor degrades the settling time, Z5U, X7R series and electrolytic capacitors are not used. A polyester film capacitor is generally used with main capacitor of the loop filter.

Q. How to use the synthesizer with V_{DD} < 4.5 V whereas DATA, CLK and $\overline{E}$ arc at 5 V logic?

A. Because of protection against electrostatic discharges, the input voltage for these logic pins can not be greater than V_{DD} + 0.3 V. An interface between the microcontroller and the synthesizer is then needed to reduce voltage at serial bus pins. A voltage divider using two resistors is a simple and cheap solution to implement. The design of this interface involves performance compromise between the current consumption and the programming speed, which depend on the resistor values in the voltage divider and the parasitic capacitance from the demonstration board. A Technical Marketing Report (TMT94008) describes some measurement results. For different values of V_{DD} < 4.5 V, the current consumption and the programming speed are given.

Q. Open loop modulation?

A. Two methods of open loop modulation are briefly described. A complete report "UMA1020M Modulation Capability for DECT" (TMT250894) is available.

Method 1: only the principal fast charge pump is used, and it is enabled/disabled using the pin FAST. The principal charge pump (pin CPP) is grounded. An internal circuit synchronizes the FAST signal with the fast charge pump correction current pulses. This avoids opening the loop when the fast charge pump is still active, which would cause a frequency drift. After the loop is opened, the UMA1020M (or UMA1018M) principal synthesizer can then be powered down to reduce consumption. Some precautions must be taken when the principal fast charge pump is switched off.

Method 2: the loop is opened by powering down (PON pin) the principal synthesizer directly. The signal sent to the PON is externally synchronized with the charge pumps to avoid powering down the synthesizer while they are still active.

Two problems can occur when a synthesizer is powered down:

The first is known as "load pulling". When the synthesizer is switched off, its RF input impedance may change and then an unintended jump in frequency is possible if the VCO is susceptible to load changes. This problem is negligible with the UMA10XX synthesizers, a frequency drift of less than 2kHz has been observed with the UMA1020M in a typical DECT application.

The second problem is called "pushing". The frequency of the VCO moves with changes in its supply voltage. When the principal synthesizer is powered down, it may temporally affect the supply voltage. Two separate voltage supplies (one for the synthesizer, the other for the VCO) will eliminate frequency shift due to "pushing". Alternatively, if using only one voltage supply, proper supply decoupling will attenuate.

7. REFERENCES

1. Product specification UMA1018M, Philips Semiconductors, 27 June 1995.
2. Product specification UMA1020M, Philips Semiconductors, 15 June 1995.
3. Product specification UMA1020AM, Philips Semiconductors, 06 July 1995.
4. Product specification UMA1017M, Philips Semiconductors, 10 July 1995.
5. Product specification UMA1019M, Philips Semiconductors, 07 July 1995.
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8. Rohde, Ulrich L., Digital PLL Frequency Synthesizers, Theory and Design, Prentice–HaII, Englewood Cliffs, New Jersey 1983.