AN98580

Migration from Macronix® MX25L to Cypress S25FL1-K SPI Flash Family

AN98580 provides migration guidelines for migrating from Macronix MX25L to Cypress S25FL1-K SPI Flash Families. The discussions will focus on same density migrations, specifically the cases when migrating from the MX25L16 to S25FL116K, from the MX25L32 to S25FL132K, and when migrating from the MX25L64 to the S25FL164K. Concerns regarding migration to and from other densities can be extrapolated from the provided discussions.

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1 Introduction

This application note provides migration guidelines for migrating from Macronix MX25L to Cypress S25FL1-K SPI Flash Families.

The discussions will focus on same density migrations, specifically the cases when migrating from the MX25L16 to S25FL116K, from the MX25L32 to S25FL132K, and when migrating from the MX25L64 to the S25FL164K. Concerns regarding migration to and from other densities can be extrapolated from the provided discussions.

The application note is based on information available to date from data sheets and other application notes publicly available from Cypress and Macronix. Please also refer to the latest relevant specifications.

2 Feature Comparison

MX25L products are well suited for migrations to S25FL1-K products. Some of the reasons are compatible pinouts, packages, command set, and 4/64 kB block/sector structure. Both product families support Dual I/O and Quad I/O modes.

The major difference is the different OTP handling, which requires some SW changes when this feature is in use. Please refer to the upcoming sections for more details regarding the other minor differences.

Table 1. Feature Comparison between Cypress S25FL1-K and Macronix MX25L (Sheet 1 of 2)

	MX25L16 (2) **MX25L32** (2) **MX25L64** (2)	**S25FL116K** **S25FL132K** **S25FL164K**
Standard Pinout	√	√
Standard Packages	√	√
Standard Command Set	√	√
4/64-kB Block/Sector	√ (3)	√ (4)
Multi I/O	√ (5)	√ (6)
Block Protection	√	√
OTP	√ (7)	√ (8)

Table 1. Feature Comparison between Cypress S25FL1-K and Macronix MX25L (Sheet 2 of 2)

	MX25L16 (2) **MX25L32** (2) **MX25L64** (2)	**S25FL116K** **S25FL132K** **S25FL164K**
SFDP	√ (9)	√
Program/Erase Suspend	√ (10)	√
Configuration Register	√ (11)	√
Security Register	√	—

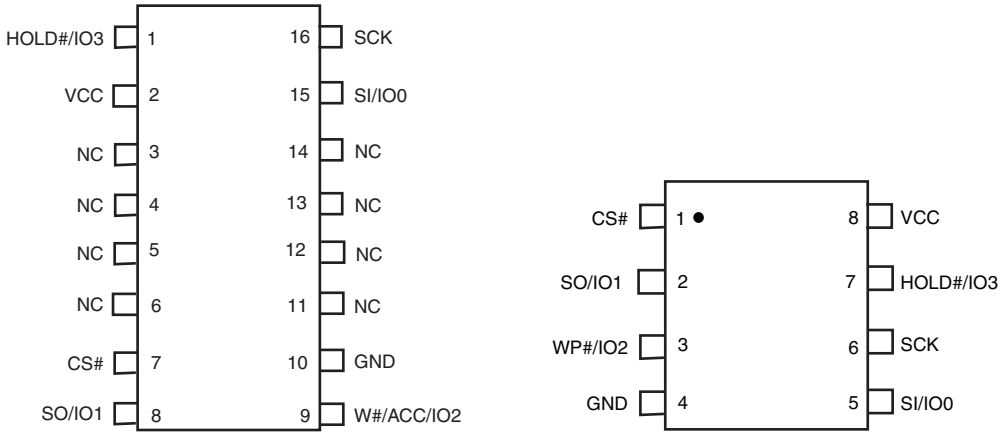
Notes:

1. *√: Feature is supported; —: Feature is not supported.*
2. *The following Macronix parts were considered in this Application Note: 16 Mbit: MX25L1606E, MX25L1633E, MX25L1635E, MX25L1636D, MX25L1636E, MX25L1673E, and MX25L1675E; 32 Mbit: MX25L3206E, MX25L3225D, MX25L3235D, MX25L3235E, MX25L3236D, MX25L3237D, MX25L3239E, MX25L3273E, and MX25L3275E; 64 Mbit: MX25L6406E, MX25L6435E, MX25L6436E, MX25L6439E, MX25L6445E, MX25L6465E, MX25L6473E, and MX25L6475E.*
3. *Supporting both uniform 64-kB sectors and uniform 4-kB sectors. The following family members additionally support uniform 32-kB sectors: MX25L3235E, MX25L3273E, MX25L3275E, MX25L6435E, MX25L6436E, MX25L6439E, MX25L6445E, MX25L6465E, MX25L6473E, and MX25L6475E.*
4. *Supporting both uniform 64-kB sectors and uniform 4-kB sectors.*
5. *Supporting Single, Dual and Quad I/O with some exceptions: MX25L1606E, MX25L3206E, and MX25L6406E support only Single and Dual I/O. MX25L3239E and MX25L6439E support only Single and Quad I/O.*
6. *All family members support Single, Dual and Quad I/O.*
7. *Offering either 64-byte or 512-byte OTP region depending on device type.*
8. *3 x 256-byte security registers.*
9. *MX25L1606E, MX25L1673E, MX25L1675E, MX25L3206E, MX25L3235E, MX25L3239E, MX25L3273E, MX25L3275E, and all 64-Mbit family members support SFDP mode.*
10. *Only MX25L3239E and MX25L6439E support Program/Erase Suspend/Resume feature.*
11. *MX25L3235E, MX25L3239E, MX25L3273E, MX25L3275E, MX25L6435E, MX25L6439E, MX25L6473E, and MX25L6475E support Configuration Register.*

2.1 Packaging — All Densities

The most common packages for MX25L and S25FL1-K are the SOIC packages. The pinout is identical, thus, this will allow a direct replacement without PCB redesign. Figure 1 shows those SOIC packages and pinouts. Please refer to the data sheets for detailed package information.

Figure 1. SOIC 150/208/300 mil Package and Pinout (16-pin and 8-pin Versions)



The package options offered by Macronix devices are wide and may differ within devices having the same density. Table 2 summarizes the full set of available packages for MX25L and S25FL1-K. Please refer to the notes at the bottom of the table which will clarify within a specific density which exact list of devices support the concerned package option.

Table 2. MX25L and S25FL1-K Available Packages

	Macronix MX25L			Cypress S25FL1-K		
	MX25L16	**MX25L32**	**MX25L64**	**S25FL116K**	**S25FL132K**	**S25FL164K**
SOIC8 150 mil	√ (2)			√	√	
SOIC8 208 mil	√	√ (3)	√	√	√	√
SOIC16 300 mil	√ (4)	√ (5)	√ (6)			√
USON 5x6				√	√	√
USON 4x4	√ (7)	√ (8)				
WSON 6x5	√ (9)	√ (10)	√ (11)			
WSON 8x6		√ (12)	√ (13)			
24-Ball BGA	√ (14)	√ (15)	√ (16)	√	√	√
8-Pin PDIP 300 mil	√ (17)	√ (18)				

Notes:

1. *√: Package is available.*
2. *Only MX25L1606E supports this package option.*
3. *All available 32-Mbit devices support this package option except MX25L3237D.*
4. *Only MX25L1606E and MX25L1636D support this package option.*
5. *All available 32-Mbit devices support this package option except MX25L3225D, MX25L3236D, and MX25L3239E.*
6. *All available 64-Mbit devices support this package option except MX25L6439E.*
7. *Only MX25L1606E and MX25L1633E support this package option.*
8. *Only MX25L3206E supports this package option.*
9. *Package option supported by MX25L1606E, MX25L1633E, MX25L1673E, and MX25L1675E.*
10. *All available 32-Mbit devices support this package option except MX25L3225D and MX25L3236D.*
11. *Package option supported by MX25L6435E, MX25L6473E, and MX25L6475E.*
12. *Only MX25L3235D supports this package option.*
13. *Package option supported by MX25L6406E, MX25L6436E, MX25L6445E, and MX25L6465E.*
14. *Only MX25L1606E supports this package option.*
15. *Only MX25L3206E supports this package option.*
16. *Only MX25L6406E and MX25L6435E support this package option.*
17. *Only MX25L1606E supports this package option.*
18. *Only MX25L3206E supports this package option.*

2.2 Sector Architecture

The sector architecture of MX25L and S25FL1-K is fully compatible. These families offer both 4-kB and 64-kB uniform sector architecture. In addition to that and on some specific devices, Macronix offers 32-kB uniform sector architecture as well.

To summarize, both device families support similar flexible erase architecture of 4-kB, 64-kB, and chip erase operations (see Table 13, . *Command Set of MX25L and S25FL1-K* on page 8). Page programming size of 256 byte is also identical. Table 3 shows a summary of the erase and programming granularity.

When migrating from MX25L to S25FL1-K, if the 32-kB erase command has not been used which is very likely to be the case, then no software adaptation is required with regards to accommodating sector layouts.

Table 3. Erase and Programming Granularity

	Macronix MX25L	**Cypress S29FL1-K**
Sector Size	4 kB, 32 kB (1), 64 kB	4 kB, 64 kB
Erase Size	4-kB, 32-kB (1), 64-kB, chip erase	4-kB, 64-kB, chip erase
Page Program Size	256 bytes	256 bytes

Note:

1. *Only MX25L3235E, MX25L3273E, MX25L3275E, and all 64 MB devices except MX25L6406E offer this sector architecture.*

2.3 Sector Protection

Both MX25L and S25FL1-K offer the same Sector Protection based on Block Protect Bits. MX25L uses four bits (BP3, BP2, BP1, BP0) whereas S25FL1-K uses only 3 bits (BP2, BP1, BP0). However, the fourth bit, BP3, can be ignored since the same protection can be achieved using the first three bits and the protection will have exactly the same layout on both device families when leaving BP3 at its default value 0. Therefore, if BP3 has not been used so far, there is no software change required when migrating to the S25FL1-K.

Using BP bits, all, none, or a portion of the memory array can be protected from Program and Erase instructions. By default, the BP Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register SR (SR[4], SR[3], SR[2]) that provide Write Protection control and status (Status Register is also referred to as SR1 in the S25FL1-K case). The factory default setting for the Block Protect Bits is 0 (none of the array is protected). BP bits can be set using the Write Status Register Instruction.

The TB (Top/Bottom selector) bit on the MX25L is located at bit 3 of the Configuration Register (CR[3]) while this bit on S25FL1-K is located at bit 5 of the Status Register 1 (SR1[5]). It is also important to note that not all MX25L devices offer TB bit. The non-volatile TB bit controls if the BP bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array. The non-volatile Sector/Block Protect bit (SEC) on S25FL1-K devices controls if the Block Protect bits (BP2, BP1, BP0) protect either 4-kB Sectors (SEC=1) or 64-kB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array. The Complement Protect bit (CMP) on S25FL1-K is a non-volatile read/write bit in the status register SR2 (SR2[6]). It is used in conjunction with SEC, TB, BP2, BP1, and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1, and BP0 will be reversed.

The SEC and CMP bits functionality is not available on MX25L. Therefore, when migrating to the S25FL1-K, no software adaptation is required in this area.

Some MX25L devices offer an individual block lock mechanism that is not supported by the S25FL1-K so this might require a software change.

Table 4, Table 5, and Table 6 respectively show the MX25L32 (TB = 0), MX25L32 (TB = 1). and S25FL132K sector protection.

Table 4. MX25L32 Status Register Memory Protection (TB = 0)

Status Register				Protect Level
BP3	**BP2**	**BP1**	**BP0**	**32 Mb**
0	0	0	0	0 (None)
0	0	0	1	1 (1 block, block 63)
0	0	1	0	2 (2 blocks, blocks 62-63)
0	0	1	1	3 (4 blocks, blocks 60-63)
0	1	0	0	4 (8 blocks, blocks 56-63)
0	1	0	1	5 (16 blocks, blocks 48-63)
0	1	1	0	6 (32 blocks, blocks 32-63)
0	1	1	1	7 (64 blocks, protect all)
1	0	0	0	8 (64 blocks, protect all)
1	0	0	1	9 (64 blocks, protect all)
1	0	1	0	10 (64 blocks, protect all)
1	0	1	1	11 (64 blocks, protect all)
1	1	0	0	12 (64 blocks, protect all)
1	1	0	1	13 (64 blocks, protect all)
1	1	1	0	14 (64 blocks, protect all)
1	1	1	1	15 (64 blocks, protect all)

Table 5. MX25L32 Status Register Memory Protection (TB = 1)

Status Register				Protect Level
BP3	BP2	BP1	BP0	32 Mb
0	0	0	0	0 (None)
0	0	0	1	1 (1 block, block 0)
0	0	1	0	2 (2 blocks, blocks 0-1)
0	0	1	1	3 (4 blocks, blocks 0-3)
0	1	0	0	4 (8 blocks, blocks 0-7)
0	1	0	1	5 (16 blocks, blocks 0-15)
0	1	1	0	6 (32 blocks, blocks 0-31)
0	1	1	1	7 (64 blocks, protect all)
1	0	0	0	8 (64 blocks, protect all)
1	0	0	1	9 (64 blocks, protect all)
1	0	1	0	10 (64 blocks, protect all)
1	0	1	1	11 (64 blocks, protect all)
1	1	0	0	12 (64 blocks, protect all)
1	1	0	1	13 (64 blocks, protect all)
1	1	1	0	14 (64 blocks, protect all)
1	1	1	1	15 (64 blocks, protect all)

Table 6. S25FL132K Status Register Memory Protection (CMP = 0)

Status Register (1)					S25FL1-K Family (32-Mbit) Block Protection (CMP=0) (3)			
SEC	TB	BP2	BP1	BP0	Protected Block(s)	Protected Addresses	Protected Density	Protected Portion (2)
X	X	0	0	0	None	None	None	None
0	0	0	0	1	63	3F0000h – 3FFFFFh	64 kB	Upper 1/64
0	0	0	1	0	62 and 63	3E0000h – 3FFFFFh	128 kB	Upper 1/32
0	0	0	1	1	60 thru 63	3C0000h – 3FFFFFh	256 kB	Upper 1/16
0	0	1	0	0	56 thru 63	380000h – 3FFFFFh	512 kB	Upper 1/8
0	0	1	0	1	48 thru 63	300000h – 3FFFFFh	1 MB	Upper 1/4
0	0	1	1	0	32 thru 63	200000h – 3FFFFFh	2 MB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64 kB	Lower 1/64
0	1	0	1	0	0 and 1	000000h – 01FFFFh	128 kB	Lower 1/32
0	1	0	1	1	0 thru 3	000000h – 03FFFFh	256 kB	Lower 1/16
0	1	1	0	0	0 thru 7	000000h – 07FFFFh	512 kB	Lower 1/8
0	1	1	0	1	0 thru 15	000000h – 0FFFFFh	1 MB	Lower 1/4
0	1	1	1	0	0 thru 31	000000h – 1FFFFFh	2 MB	Lower 1/2
X	X	1	1	1	0 thru 63	000000h – 3FFFFFh	4 MB	All
1	0	0	0	1	63	3FF000h – 3FFFFFh	4 kB	Upper 1/1024
1	0	0	1	0	63	3FE000h – 3FFFFFh	8 kB	Upper 1/512
1	0	0	1	1	63	3FC000h – 3FFFFFh	16 kB	Upper 1/256
1	0	1	0	X	63	3F8000h – 3FFFFFh	32 kB	Upper 1/128
1	1	0	0	1	0	000000h – 000FFFh	4 kB	Lower 1/1024
1	1	0	1	0	0	000000h – 001FFFh	8 kB	Lower 1/512
1	1	0	1	1	0	000000h – 003FFFh	16 kB	Lower 1/256
1	1	1	0	X	0	000000h – 007FFFh	32 kB	Lower 1/128

Notes:

1. *X = don't care.*
2. *Lower or Upper portion of the array.*
3. *If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.*
4. *The Complement Protect bit (CMP SR2[6]) is a non-volatile read/write bit in the status register (SR2[6]). It is used in conjunction with SEC, TB, BP2, BP1, and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1, and BP0 will be reversed. For instance, when CMP=0, a top 4-kB sector can be protected while the rest of the array is not; when CMP=1, the top 4-kB sector will become unprotected while the rest of the array become read-only.*

2.4 Status and Configuration Registers

The Status Register can be read to determine the device's ready/busy status as well as the status of many other functions, such as Hardware Locking and Software Protection. The Status Register is referred to as SR on MX25L and SR1 on S25FL1-K. We will use the term SR from here on to refer to the Status Register.

The Configuration Register is used to change some device settings and configurations. The Configuration Register is referred to as CR on MX25L and SR2 on S25FL1-K. We will use the term CR from here on to refer to the Configuration Register.

All SR bits except SR[5] and SR[6] provide the same information on MX25L and S25FL1-K. SR[5] and SR[6] are used as BP3 and QE (Quad Enable) respectively on MX25L, while they contain TB (Top / Bottom selector) and SEC (for setting of Sector protection granularity) on S25FL1-K respectively. The TB bit is located at bit 3 of the CR on MX25L. That being said, a software change might be needed here to stop using SR[5] and SR[6] bits as BP3 and QE and make a correct use of them if needed.

The configuration register layout is completely different on MX25L and S25FL1-K. The CR read command that is used is also different. Please refer to Table 9 and Table 10 for more details about this register layout. A software change might also be needed here to make correct use of CR bits.

Cypress S25FL1-K devices have one additional Status Register (SR3) that can be used to configure the burst wrap feature. The Write Status Register instruction allows up to three Status Registers (SR/SR1, CR/SR2 and SR3) to be written in one command sequence. The read-only Status Register bit locations will not be affected by the Write Status Register instruction.

On the other hand, Macronix MX25L devices have one additional Security Register that can be used to lock down the secured OTP, enable the continuously program mode, select the write protection mode (BP bits or single block locking), and retrieve embedded operations error status (P_FAIL and E_FAIL).

Table 7, Table 9, and Table 11 show the MX25L Status Register (SR), Configuration Register (CR), and Security Register respectively, while Table 8, Table 10, and Table 12 show the S25FL1-K Status Register 1 (SR1), Status Register 2 (SR2), and Status Register 3 (SR3) respectively.

Table 7. MX25L Status Register (SR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRWD (Status Register Write Protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (Write Enable Latch)	WIP (Write in Progress bit)
1 = Status Register Write disable	1 = Quad Enable 0 = Not Quad Enable	—	—	—	—	1 = Write Enable 0 = Not Write Enable	1 = Write Operation 0 = Not in Write Operation
Non-Volatile Bit	Non-Volatile Bit	Non-Volatile Bit	Non-Volatile Bit	Non-Volatile Bit	Non-Volatile Bit	Volatile Bit	Volatile Bit

Table 8. Cypress S25FL1-K Status Register 1 (SR1)

Bits	Field Name	Function	Type	Default State	Description
7	SRP0	Status Register Protect 0	Non-volatile and volatile versions	0	0 = WP# input has no effect or Power Supply Lock Down mode 1 = WP# input can protect the Status Register or OTP Lock Down
6	SEC	Sector / Block Protect		0	0 = BP2-BP0 protect 64-kB blocks 1 = BP2-BP0 protect 4-kB sectors
5	TB	Top / Bottom Protect		0	0 = BP2-BP0 protect from the Top down 1 = BP2-BP0 protect from the Bottom up
4	BP2	Block Protect Bits		0	000b = No protection
3	BP1			0	
2	BP0			0	
1	WEL	Write Enable Latch	Volatile, Read only	0	0 = Not Write Enabled, no embedded operation can start 1 = Write Enabled, embedded operation can start
0	BUSY	Embedded Operation Status	Volatile, Read only	0	0 = Not Busy, no embedded operation in progress 1 = Busy, embedded operation in progress

Table 9. MX25L Configuration Register (CR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DC (Dummy Cycle)	Reserved	Reserved	Reserved	TB (top/ bottom selected)	Reserved	Reserved	Reserved
—	√	√	√	0 = Top area protect 1 = Bottom area protect (default = 0)	√	√	√
Volatile Bit	√	√	√	OTP	√	√	√

Table 10. Cypress S25FL1-K Status Register 2 (SR2)

Bits	Field Name	Function	Type	Default State	Description
7	SUS	Suspend Status	Volatile, Read Only	0	0 = Erase / Program not suspended 1 = Erase / Program suspended
6	CMP	Complement Protect	Non-volatile and volatile versions	0	0 = Normal Protection Map 1 = Inverted Protection Map
5	LB3	Security Register Lock Bits	OTP	0	OTP Lock Bits 3:0 for Security Registers 3:0 0 = Security Register not protected 1 = Security Register protected Security register 0 contains the Serial Flash Discoverable Parameters and is always programmed and locked by Cypress.
4	LB2			0	
3	LB1			0	
2	LB0			1	
1	QE	Quad Enable	Non-volatile and volatile versions	0	0 = Quad Mode Not Enabled, the WP# pin and HOLD# are enabled 1 = Quad Mode Enabled, the IO2 and IO3 pins are enabled, and WP# and HOLD# functions are disabled
0	SRP1	Status Register Protect 1		0	0 = SRP0 selects whether WP# input has effect on protection of the status register 1 = SRP0 selects Power Supply Lock Down or OTP Lock Down mode.

Table 11. MX25L Security Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPSEL	E_FAIL	P_FAIL	Continuously Program Mode (CP mode)	Reserved	Reserved	LDSO (lock-down 4k-bit secured OTP)	4k-bit secured OTP
0 = Normal WP Mode 1 = Individual WP Mode (default)	0 = Normal Erase succeed 1 = Indicate Erase failed (default = 0)	0 = Normal Program succeed 1 = Indicate Program failed (default = 0)	0 = Normal Program Mode 1 = CP Mode (default = 0)	—	—	0 = Not Lock-down 1 = Lock-down (cannot program/ erase OTP)	0 = Non-factory lock 1 = Factory lock
Non-Volatile Bit	Volatile Bit	Volatile Bit	Volatile Bit	Volatile Bit	Volatile Bit	Non-Volatile Bit	Non-Volatile Bit
OTP	Read Only	Read Only	Read Only	Read Only	Read Only	OTP	Read Only

Table 12. Cypress S25FL1-K Status Register 3 (SR3)

Bits	Field Name	Function	Type	Default State	Description
7	RFU	Reserved		0	Reserved for Future Use
6	W6	Burst Wrap Length	Volatile	1	00 = 8-byte wrap. Data read starts at the initial address and wraps within an aligned 8-byte boundary 01 = 16-byte wrap. Data read starts at the initial address and wraps within an aligned 16-byte boundary. 10 = 32-byte wrap. Data read starts at the initial address and wraps within an aligned 32-byte boundary. 11 = 64-byte wrap. Data read starts at the initial address and wraps within an aligned 64-byte boundary.
5	W5			1	
4	W4	Burst Wrap Enable		1	0 = Wrap Enabled 1 = Wrap Disabled
3	Latency Control (LC)	Variable Read Latency Control		0	Defines the number of read latency cycles in Fast Read, Dual Out, Quad Out, Dual IO, and Quad IO commands. Binary values for 1 to 15 latency cycles. A value of zero disables the variable latency mode.
2				0	
1				0	
0				0	

3 Software Considerations

3.1 MX25L versus S25FL1-K Command Set Comparison

MX25L and S25FL1-K have a wide range of common instructions (op-codes) in their command-set.

While Cypress S25FL1-K devices have some additional commands that are related to reading SR-3 and Burst Read mode, MX25L devices have additional commands for 32-kB sector erase (P32E), quad page programming (4PP), and single block locking.

Table 13 shows a comparison summary of the command set of MX25L and S25FL1-K device families.

Table 13. Command Set of MX25L and S25FL1-K (Sheet 1 of 3) (Sheet 1 of 3)

Name	Description	MX25L16 MX25L32 MX25L64	S25FL116K S25FL132K S25FL164K
READ	Read Data (Single output)	03H	03H
FAST_READ	Fast Read (Single output)	0BH	0BH
DOR	Dual Output Fast Read	3BH	3BH

Table 13. Command Set of MX25L and S25FL1-K (Sheet 2 of 3) (Sheet 2 of 3)

Name	Description	MX25L16 MX25L32 MX25L64	S25FL116K S25FL132K S25FL164K
QOR	Quad Output Fast Read	6BH	6BH
DIOR	Dual I/O Fast read	BBH	BBH
QIOR	Quad I/O Fast read	EBH	EBH
	Quad I/O Fast read with 4 dummy cycles	E7H	—
RDID	Read Identification (JEDEC)	9FH	9FH
READ_ID	Read Mfg. ID and device ID	90H	90H
REMS	Read Electronic Man and Dev ID	EFH, DFH	—
	Set Burst with Wrap	—	77H
	Continuous Read Mode Reset	FFH	FFH
WREN	Write Enable	06H	06H
WRDI	Write Disable	04H	04H
	Write Enable for volatile status Register	—	50H
P4E	4-kB Sector Erase	20H	20H
P32E	32-kB Sector Erase	52H (1)	—
SE	64-kB Block Erase	D8H	D8H
BE	Bulk Erase	C7H, 60H	C7H, 60H
	Erase/Program Suspend	75H (1)	75H
	Erase/Program Resume	7AH (1)	7AH
PP	Page Program	02H	02H
4PP	Quad Page Program	38H (1)	—
	Continuous Program	ADH (1)	—
DP	Deep-Power Down	B9H	B9H
RES	Release from Deep-Power Down	ABH	ABH
RES	Release from Deep-Power Down / Read Electronic Signature	ABH	ABH
RDSR	Read Status Register / Status Register 1	05H	05H
RCR	Read Configuration Register / Status Register 2	15H (1)	35H
	Read Status Register 3	—	33H
WRR	Write Status Register	01H	01H
	Read SFDP Register	5AH (1)	5AH
	Read Security Registers (OTP)	—	48H
	Erase Security Registers (OTP)	—	44H
	Program Security Registers (OTP)	—	42H
	Read Security Register	2BH	—
	Write Security Register	2FH	—
ENSO	Enter Secured OTP	B1H	—
EXSO	Exit Secured OTP	C1H	—
SBLK	Single Block Lock	36H (1)	—
SBULK	Single Block Unlock	39H (1)	—
RDBLOCK	Block Protect Read	3CH (1)	—
GBLK	Gang Block Lock	7EH (1)	—
GBULK	Gang Block Unlock	98H (1)	—
RSTEN	Reset Enable	66H (1)	—
RST	Reset Memory	99H (1)	—
WPSEL	Write Protect Selection	68H (1)	—

Table 13. Command Set of MX25L and S25FL1-K (Sheet 3 of 3) (Sheet 3 of 3)

Name	Description	MX25L16 MX25L32 MX25L64	S25FL116K S25FL132K S25FL164K
ESRY	Enable SO to output RY/BY#	70H (1)	—
DSRY	Disable SO to output RY/BY#	80H (1)	—

Note:

1. *Feature is not supported by all the available devices.*

3.2 OTP Related Commands

The OTP (One Time Programmable) area is a special region that can be used to store a serial number or a security-oriented key. The MX25L has a 64-byte or a 512-byte OTP area depending on the device type. This region is for customer usage and can be locked by the end user or locked at the factory.

On the other hand, the S25FL1-K family provides three 256-byte Security Registers that can be used to store information that can be permanently protected by programming One Time Programmable (OTP) lock bits in Status Register 2 (LB3, LB2, and LB1). The S25FL1-K offers another 256-byte Security Register that is used by Cypress to store and protect the Serial Flash Discoverable Parameters (SFDP) information that is also accessed by the Read SFDP command.

The three additional Security Registers can be erased, programmed, and protected individually. These registers may be used by system manufacturers to store and permanently protect security or other important information separate from the main memory array.

Since the MX25L and S25FL1-K present different OTP layouts and commands to access the OTP area, software changes are needed to correctly use the OTP feature.

Table 14 lists the OTP commands of both the MX25L and S25FL1-K devices.

Table 14. OTP Commands

Name	Description	MX25L16 MX25L32 MX25L64	S25FL116K S25FL132K S25FL164K
	Read Security Registers	—	48H
	Erase Security Registers	—	44H
	Program Security Registers	—	42H
ENSO	Entered Secured OTP (1)	B1H	—
EXSO	Exit Secured OTP (1)	C1H	—

Note:

1. *Normal program command should be used to program the OTP area after sending the secured OTP enter command.*

4 Timing Considerations

4.1 Power-Up Timing

One of the most sensitive electrical specifications is the power-up timing needed to correctly initialize the device. Figure 2 and Table 15 show the power-up characteristics of both MX25L and S25FL1-K devices.

Figure 2. Power-Up Timing Diagram

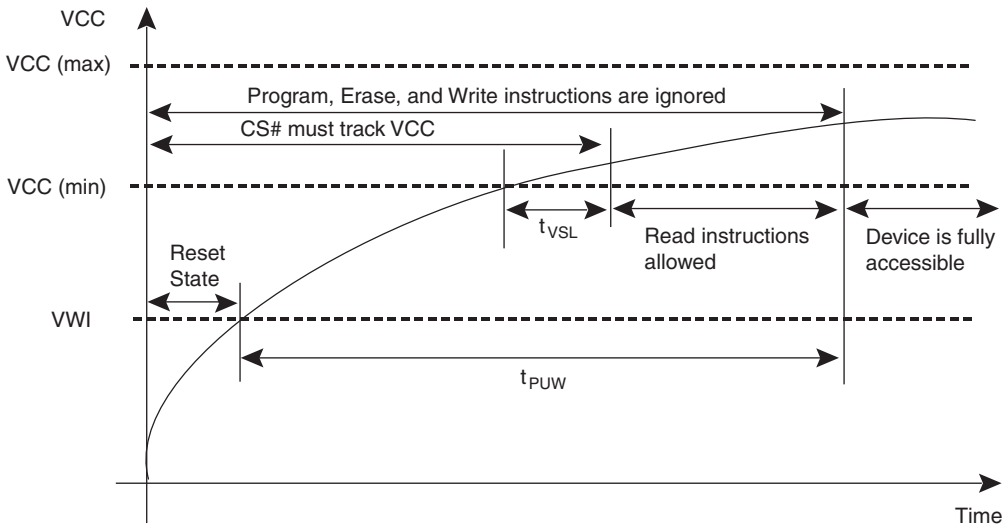


Table 15. MX25L and S25FL1-K Power-Up Timing Requirements

Parameter	Symbol	MX25L		S25FL1-K		Units
		Min	Max	Min	Max	
V_{CC} (min) to CS# Low	t_{VSL}	200 (1)	— (2)	10	—	µs
Delay before Program or Erase	t_{PU}/t_{PUW}	— (2)	— (2)	1	10	ms
Write Inhibit Threshold Voltage	t_{WI}	2.1	2.5	1.0	2.0	V

Notes:

1. *On some Macronix devices, it is even specified as 300 µs.*
2. *Those parameters are not described in the corresponding data sheets.*

It is important to note that the power-up parameters of the MX25L family members are more restrictive. In particular, the delay before the system issues the first Program/Erase operation (t_{VSL}) needs to up to 20 times longer. On the other hand, writes are inhibited already at 2.5V for the MX25L, while S25FL1-K allows writing down to 2.0V.

4.2 Data in Setup/Hold Time

Two AC timing parameters that are critical in SPI designs are Data In Setup Time and Data In Hold Time. They specify how long data needs to be valid before and after the rising edge of the clock signal, respectively. Table 16 shows the Data in Setup/Hold timing characteristics for both MX25L and S25FL1-K devices.

The MX25L and S25FL1-K Devices have very similar timing. The minor difference should not impact design but may need to be verified.

Table 16. Data in Setup/Hold Timing Characteristics

Parameter	Symbol	MX25L16 MX25L32 MX25L64	S25FL116K S25FL132K S25FL164K	Units
Data In Setup Time (Min)	t_{DVCH}/t_{SU}	2	2	ns
Data In Hold Time (Min)	t_{CHDX}/t_{HD}	3	5	ns

4.3 Further Timing Comparison

In general, the timing characteristics of both MX25L and S25FL1-K are almost identical. For example, the CS# deselect time is approximately the same for both device families. Table 4.3 shows a comparison between MX25L and S25FL1-K with regards to the various CS# deselect times.

Since the timing requirement is less restrictive for FL1-K devices, there is no need to apply any changes here.

Table 17. CS# Deselect Time Characteristics

Parameter	Symbol	MX25L	S25FL1-K	Units
CS# deselect time between Reads (Min)	t_{SHSL1}/T_{CS1}	15	7	ns
CS# deselect time for Read after Writes (Min)	t_{SHSL2}/T_{CS2}	50	40	ns

5 Conclusion

Similar pinout, packages, command set and sector architecture make migrating from MX25L to the S25FL1-K straightforward, although it can require some accommodation with regard to the system software. However, no accommodation is required from a hardware perspective.

Software changes should be considered when using the following features:

- 32-kB Sub-sectors erase command (52H)
- OTP feature
- TB (Top/Bottom selector) and QE (Quad Enable) Bits
- Configuration Register
- Single Block Lock feature

Once accommodations are made, Cypress S25FL1-K flash will enable access to a superior read throughput up to 54 Mbytes/s using Quad bit data path which cannot be achieved by any of the available Macronix parts as of today.

Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	-	03/20/2013	Initial version
*A	4929320	MSWI	09/22/2015	Updated in Cypress template
*B	5844281	AESATMP8	08/04/2017	Updated logo and Copyright.

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