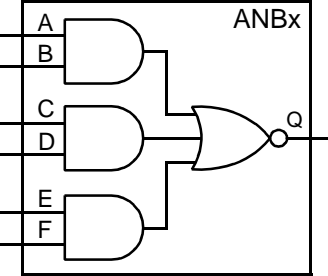


AMI5HG 0.5 micron CMOS Gate Array

Description

ANBx is a family of AND-NOR circuits consisting of three 2-input AND gates into a 3-input NOR gate.

Logic Symbol	Truth Table																																			
	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>C</th> <th>D</th> <th>E</th> <th>F</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>L</td> </tr> <tr> <td>X</td> <td>X</td> <td>H</td> <td>H</td> <td>X</td> <td>X</td> <td>L</td> </tr> <tr> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>H</td> <td>H</td> <td>L</td> </tr> <tr> <td colspan="6">All other combinations</td> <td>H</td> </tr> </tbody> </table>	A	B	C	D	E	F	Q	H	H	X	X	X	X	L	X	X	H	H	X	X	L	X	X	X	X	H	H	L	All other combinations						H
A	B	C	D	E	F	Q																														
H	H	X	X	X	X	L																														
X	X	H	H	X	X	L																														
X	X	X	X	H	H	L																														
All other combinations						H																														

Core Logic

HDL Syntax

Verilog ANBx *inst_name* (Q, A, B, C, D, E, F);

VHDL *inst_name*: ANBx port map (Q, A, B, C, D, E, F);

Pin Loading

Pin Name	Equivalent Loads		
	ANB2	ANB4	ANB6
A	1.0	1.0	2.1
B	1.0	1.0	2.1
C	1.0	1.0	2.1
D	1.0	1.0	2.1
E	1.0	1.0	2.1
F	1.0	1.0	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics ^a	
		Static I _{DD} (T _J = 85°C) (nA)	EQL _{pd} (Eq-load)
ANB2	5.0	TBD	10.3
ANB4	6.0	TBD	10.3
ANB6	12.0	TBD	20.9

a. See page 2-15 for power equation.

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Propagation Delays (ns)

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 5.0\text{V}$, Typical Process

ANB2	Number of Equivalent Loads		1	4	8	13	17 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.46 0.42	0.57 0.54	0.69 0.67	0.84 0.82	0.96 0.93
ANB4	Number of Equivalent Loads		1	8	15	22	30 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.47 0.40	0.61 0.54	0.72 0.65	0.82 0.75	0.93 0.87
ANB6	Number of Equivalent Loads		1	14	28	42	56 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.46 0.40	0.61 0.51	0.72 0.62	0.82 0.72	0.91 0.84

Delay will vary with input conditions. See page 2-17 for interconnect estimates.