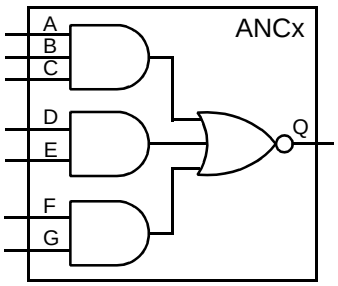
Description

ANCx is a family of AND-NOR circuits consisting of one 3-input AND gate and two 2-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
H	H	H	X	X	X	X	L
X	X	X	H	H	X	X	L
X	X	X	X	X	H	H	L
All other combinations							H

HDL Syntax

Verilog ..... ANCx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ANCx port map (Q, A, B, C, D, E, F, G);

Pin Loading

Pin Name	Equivalent Loads		
	ANC2	ANC4	ANC6
A	1.0	1.0	2.1
B	1.0	1.0	2.1
C	1.0	1.0	2.1
D	1.0	1.0	2.1
E	1.0	1.0	2.1
F	1.0	1.0	2.1
G	1.0	1.0	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Size And Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANC2	6.0	TBD	11.4
ANC4	7.0	TBD	12.5
ANC6	12.0	TBD	21.1

a. See page 2-15 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ANC2	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.49 0.51	0.60 0.63	0.73 0.76	0.87 0.91	0.97 1.02
ANC4	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.50 0.51	0.63 0.65	0.73 0.76	0.83 0.86	0.93 0.97
ANC6	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.46 0.45	0.59 0.60	0.69 0.71	0.79 0.81	0.90 0.93

Delay will vary with input conditions. See page 2-17 for interconnect estimates.