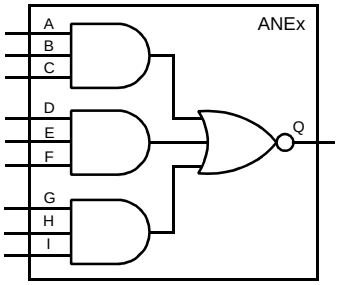
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

ANEx is a family of AND-NOR circuits consisting of three 3-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Q
H	H	H	X	X	X	X	X	X	L
X	X	X	H	H	H	X	X	X	L
X	X	X	X	X	X	H	H	H	L
All other combinations									H

HDL Syntax

Verilog ..... ANEx *inst_name* (Q, A, B, C, D, E, F, G, H, I);

VHDL..... *inst_name*: ANEx port map (Q, A, B, C, D, E, F, G, H, I);

Pin Loading

Pin Name	Equivalent Loads		
	ANE2	ANE4	ANE6
A	1.0	1.0	2.1
B	1.0	1.0	2.1
C	1.0	1.0	2.1
D	1.0	1.0	2.1
E	1.0	1.0	2.1
F	1.0	1.0	2.1
G	1.0	1.0	2.1
H	1.0	1.0	2.1
I	1.0	1.0	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ANE2	7.0	TBD	12.7
ANE4	8.0	TBD	13.8
ANE6	14.0	TBD	23.2

a. See page 2-15 for power equation.

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Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ANE2	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.49 0.51	0.59 0.61	0.71 0.75	0.86 0.91	0.97 1.03
ANE4	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.53 0.51	0.67 0.65	0.79 0.76	0.90 0.86	1.02 0.97
ANE6	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.46 0.48	0.57 0.59	0.69 0.69	0.79 0.79	0.88 0.89

Delay will vary with input conditions. See page 2-17 for interconnect estimates.