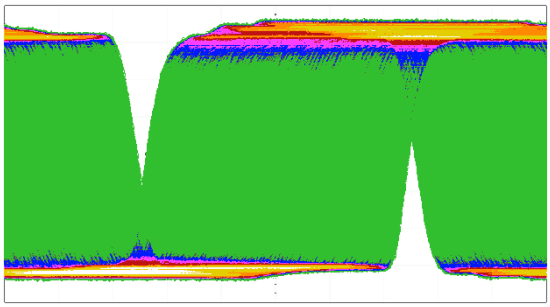
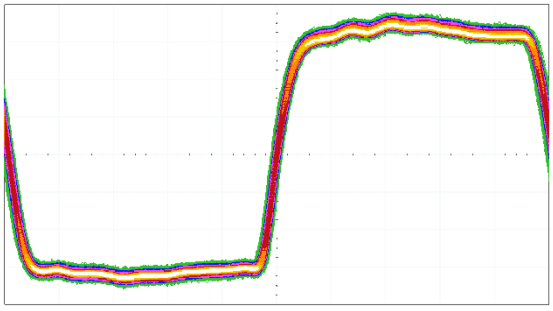
Introduction

The JitterBlocker takes very noisy and jittery clocks and cleans out all the deterministic and excessive jitter. It can handle thousands of picoseconds of period jitter at its input and reduces that to below 100ps on the output.

Eye-Opening Performance

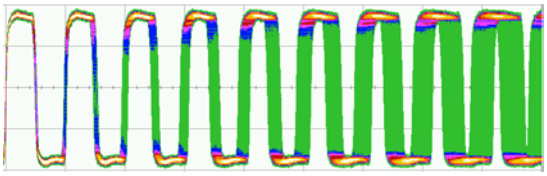


When Eyes Close

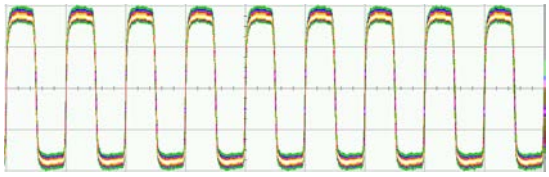


JitterBlocker Output

Block Jitter Accumulation

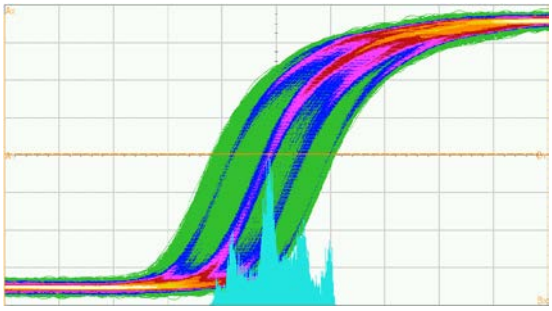


When Jitter Accumulates

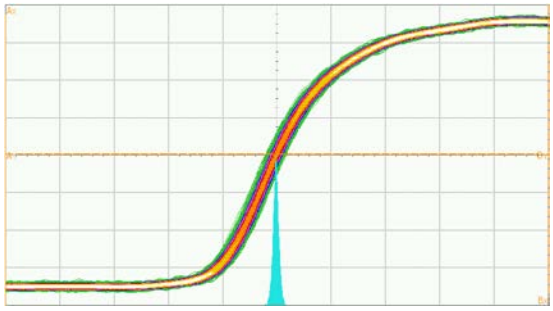


JitterBlocker Output

Block Deterministic Jitter



When Deterministic Jitter Dominates



JitterBlocker Output

Multi-purpose ICs, like FPGAs or multiple-output clock generators, can make a reference clock for your system, but generally this clock is very noisy. These ICs internally deal with a multitude of signals and cross-talk often creates significant deterministic jitter in the generated clock. The period jitter can be as bad as 300ps peak-to-peak or greater.

There are also systems, like IEEE1588, that can create a clock with very high frequency accuracy, but the clock is assembled from time slices and this causes very bad period jitter on the order of thousands of picoseconds.

There are many applications that cannot handle this kind of period jitter and jitter attenuation is required to use that reference clock. However, when looking for jitter attenuating devices today, users often find only high-end devices with high-end price tags. There was nothing available to take that clock with 300ps or more (peak-to-peak) of period jitter and clean it up by 50ps to 100ps, making it useful for many more applications and without the high-end price tag.

Micrel's JitterBlocker was designed to fill that void, to be better suited for a wide variety of applications at a much more reasonable cost and with a very small form factor. The PL902 JitterBlocker is able to take extremely jittery clocks, with up to thousands of picoseconds (peak-to-peak) of period jitter and clean it up to below $100ps_{PP}$ in most cases. The PL903 and PL904 JitterBlockers focus on cleaning up phase noise, attenuating spurs in the phase noise, and lowering the phase noise floor.

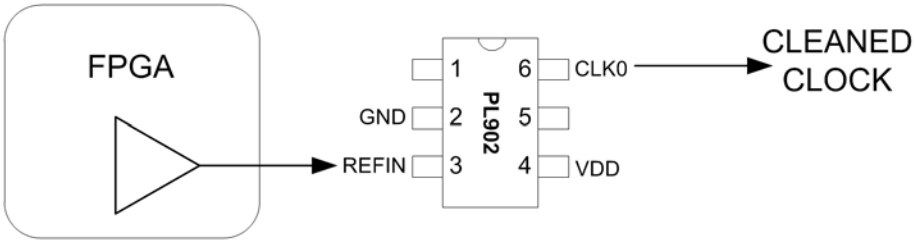
How JitterBlocker Works

The JitterBlocker has a synthesizer that will lock onto the incoming (dirty) clock and reproduce this clock on its output. The synthesizer is deliberately designed to be slow (low-loop bandwidth). This means that it cannot keep up with most of the noisy phase and frequency movements in the incoming clock and will run at the average frequency of the incoming clock. In other words, the JitterBlocker filters out (or blocks) much of the jitter in the input clock and produces a cleaned up clock on its output. The threshold for the noise frequencies that JitterBlocker filters is the synthesizer loop bandwidth. Phase-/frequency-modulated noise below the loop bandwidth passes through and phase-/frequency-modulated noise above the loop bandwidth is blocked. The loop bandwidth of the PL902 series can be as low as 4kHz. Tests show that the PL902 JitterBlocker effectively removes almost any type or amount of jitter fed into it. There are multiple examples of jitter blocking performance in the Performance section of this application note.

The PL903 and PL904 series are somewhat different animals. The PL902 works with single-ended LVCMOS clocks where period jitter is important and the PL903 and PL904 work with differential clocks where phase noise is more important. The loop bandwidth of the PL903 and PL904 JitterBlockers is about 500kHz.

How to Use JitterBlocker

The PL902 JitterBlocker can simply be inserted into the clock that needs cleaning.



The PCB can be designed with the JitterBlocker footprint and a jumper to bypass the JitterBlocker. When the reference clock is clean enough, assemble the jumper. When the reference clock is too noisy, assemble the JitterBlocker. In the block diagram above, the source for the noisy reference clock is an FPGA, but the JitterBlocker can work with any noisy source.

The JitterBlocker is a programmable synthesizer and should be configured for the frequency where it will be used. Alternatively, the synthesizer can be configured for a frequency range of, at most, one octave wide. The X's in the PL902xxx part number are a 3-digit code for the custom configuration. The same is true for the PL903xxx and PL904xxx part numbers.

Additional Features

- The output frequency does not need to be the same as the input frequency; frequency translation is possible.
- The PL902 can have up to three outputs, so there is fanout capability. The PL903 has one differential output and the PL904 can have up to three differential outputs.
- There is a configuration select pin on the PL902 that allows for switching between two different configurations. The parameters that are switched can be anything. For example, you can switch between the operating frequency (range) and the frequency translation.
- Outputs can be disabled to a high impedance (tri-state) or the whole part can be powered down to less than 10µA of supply current.

Applications

Many reasons can prompt the need for the JitterBlocker when designing an application.

- JitterBlocker to the rescue. When first testing an application, a certain clock turns out to be too noisy and the JitterBlocker can be used as a patch to fix the problem.
- The JitterBlocker can also be used as a deliberate, fundamental part of an application from the initial design plans. The JitterBlocker can be a less expensive and more compact solution than a clock oscillator module for creating clean clocks. The JitterBlocker can use available clocks in the system that were previously not suited for anything because of their jitter.
- Insurance. A designer wants to use a certain clock during the design phase, but isn't sure if it will be clean enough. Previously, designers couldn't take the risk and had to design expensive solutions. The JitterBlocker can serve as insurance and allow designers to use the clocks they want. Simply add a JitterBlocker footprint and only use it if the clock turns out to be too noisy.

Here are some example applications that would work fine with a JitterBlocker output clock, but cannot handle hundreds or thousands of pico seconds peak-to-peak of period jitter.

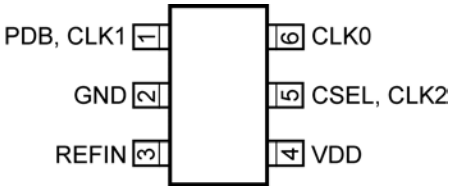
- USB clock
- Bluetooth clock
- 10/100Mbps Ethernet clock
- Microprocessor or microcontroller clock
- SAS or SATA clock
- Optical transceivers (SONET/SDH)
- PCI Express clock
- Audio/Video compression clock

There are some applications that make dirty clocks and possibly need jitter blocking:

- FPGAs can make reference clocks, but because FPGAs usually deal with multiple signals at the same time, cross-talk between signals can make the reference clocks very noisy.
- Certain systems create clocks from time slices—for example, the IEEE1588 time synchronization system. The reference clock from this system has a very accurate frequency, but unfortunately also has a lot of jitter.
- To lower electromagnetic interference (EMI), clocks can have spread spectrum modulation. Specifically, the PL902 is well suited for removing the modulation in case an application using the clock cannot handle the jitter caused by the modulation.
- In general, clocks that travel a relatively long distance across a system can pick up noise along the way.
- Clocks that need to pass an isolation boundary easily pick up noise from other signals passing the same boundary.

Pin Functions

The PL902xxx JitterBlocker is available in an SOT23-6L package.



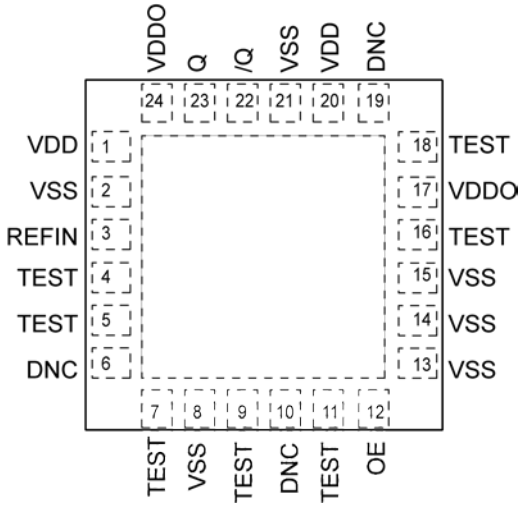
SOT23-6L
(3.0mm × 3.0mm × 1.35mm)

Pin 1 and **Pin 5** can be configured to be either a control input or a clock output. Pin 1 can be the control input for the output enable function and pin 5 can be the control input for the configuration select function.

CLK1 and **CLK2** are secondary clocks to the main CLK0 clock.

Pin 3 = REFIN. Pin 3 is the reference clock input. This input can work with signal amplitudes from 100mV_{PP} up to a rail-to-rail signal swing. This means that it can work with signals from almost any logic type.

The PL903xxx JitterBlocker is available in a QFN-24L package.



QFN-24L
(4.0mm × 4.0mm × 0.85mm)

Pin 22 and **Pin 23** is the differential output pair. The logic type can be set through programming to be LVCMOS, LVPECL, LVDS, or HCSL. In the case of LVCMOS, the phase of the output pins can be selected to make either a differential LVCMOS output or two in-phase single-ended outputs.

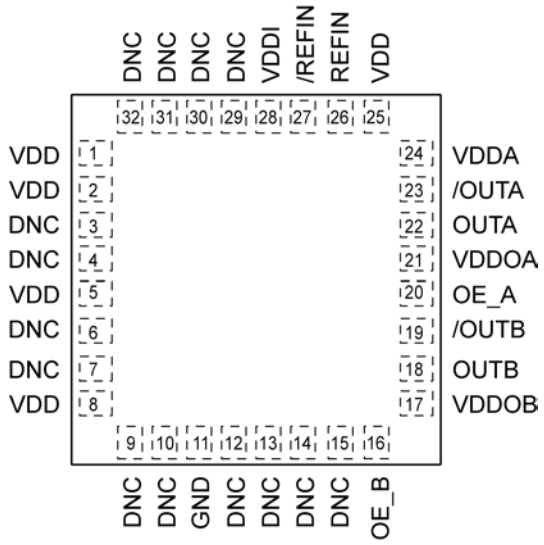
Pin 3 = REFIN. The PL903 reference clock input is single-ended and has the same properties as the PL902 with the capability to work with signal amplitudes between $100mV_{PP}$ and rail-to-rail.

Pin 17 and **Pin 24** are VDD connections for the output buffer and can be connected directly to the VDD power plane.

Pin 1 and Pin 20 are VDD connections for the analog circuits and power supply filtering is recommended. Please see the datasheet for power supply filter schematics.

Pin 12 is the output enable for the differential output on pins 22 and 23.

The PL904xxx JitterBlocker is available in a QFN-32L package.



QFN-32L
(5.0mm × 5.0mm × 0.85mm)

Pins 22-23 and **Pins 18-19** are two differential output pairs. The logic type can be set through programming to be LVCMOS, LVPECL, LVDS, or HCSL.

Pins 26-27 = REFIN. The PL904 reference clock input is differential and compatible with most differential logic types. One can also drive pin 26 only with a single-ended signal.

Pin 17 and Pin 21 are VDD connections for the output buffer and can be connected directly to the VDD power plane.

Pins 1, 2, 5, 8, and 25 are VDD connections for internal logic circuits and can also be connected directly to the VDD power plane.

Pin 24 and Pin 28 are VDD connections for analog circuits and power supply filtering is recommended. Please see the datasheet for power supply filter schematics.

Pin 20 is the output enable for the differential output on pins 22 and 23.

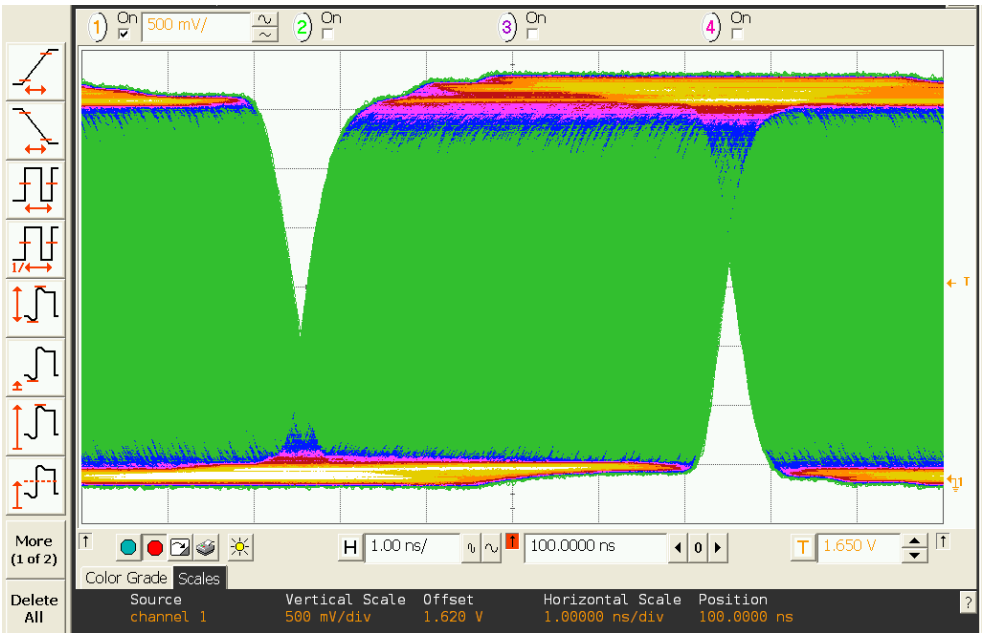
Pin 16 is the output enable for the differential output on pins 18 and 19.

Choosing Between the PL902, PL903, and PL904

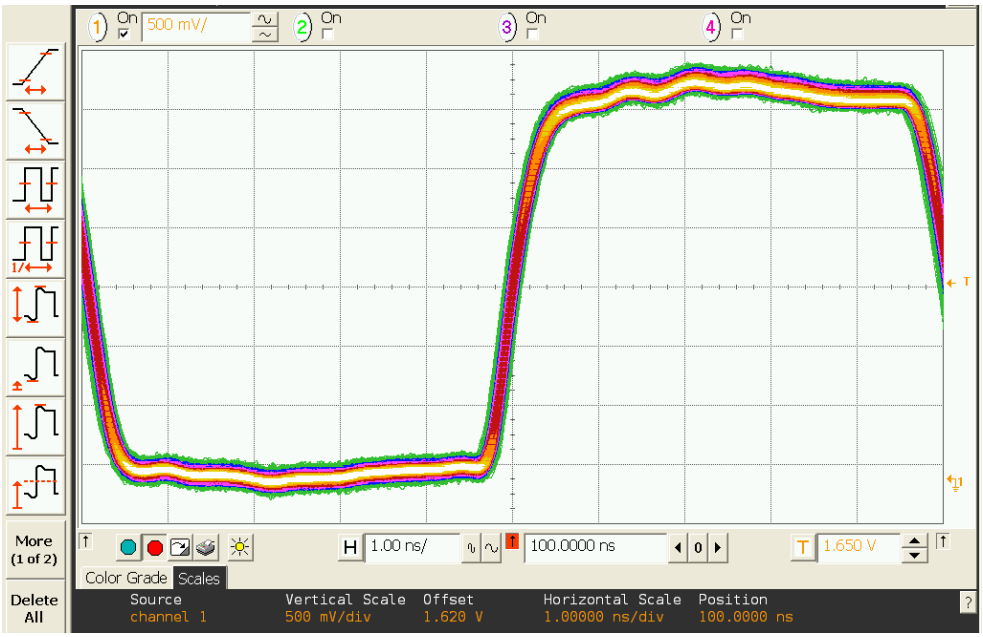
- The PL902 works with single ended clock signals only. If the dirty clock in need of cleaning is differential, the PL902 cannot be used and the choice is limited to the PL903 or PL904. If the dirty clock is single-ended, all three parts can be used and the choice will not be determined by the logic type.
- When the dirty clock in need of cleaning has hundreds or thousands of picoseconds of period jitter and the application would be happy with a reduction to about $100ps_{PP}$, then the PL902 is the ideal choice.
- When phase noise or phase jitter is a concern, the PL903 or PL904 are the better choices.
- When the dirty clock is differential, the PL904 is the most ideal choice because it has a true differential input.
- When having two differential outputs is a plus, versus just one output pair, the PL904 is the most ideal choice.
- When the dirty clock is single-ended and phase noise or phase jitter is a concern, rather than period jitter, the PL903 is the best choice. The PL903 output can still be differential.

Performance

Low frequency noise can really close the eye when looking at intervals of multiple clock cycles. The below example has noise around 100kHz and jitter is measured with a 100ns interval or 10 cycles of a 100MHz clock.



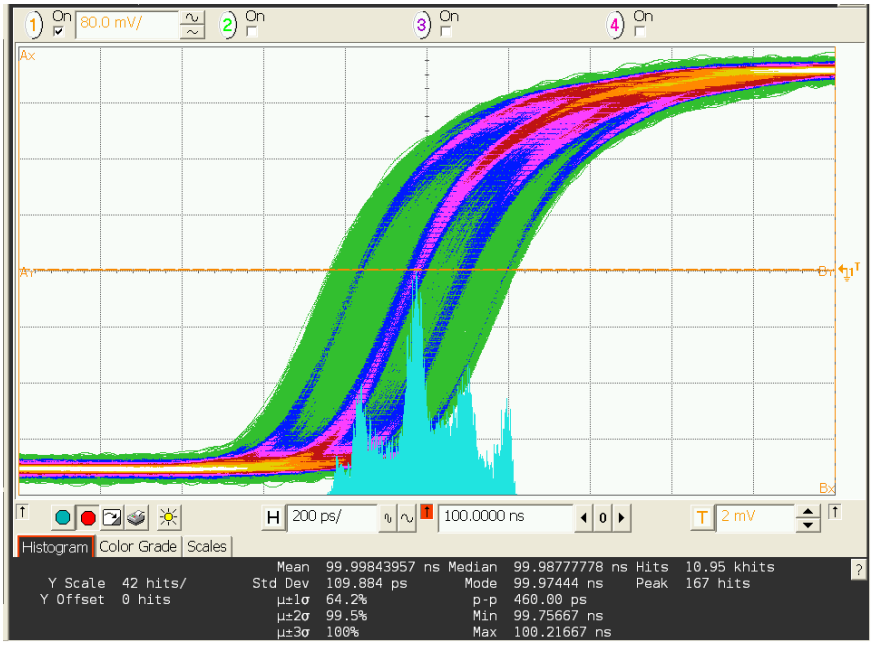
Incoming 100MHz Clock at 10th Edge After the Trigger



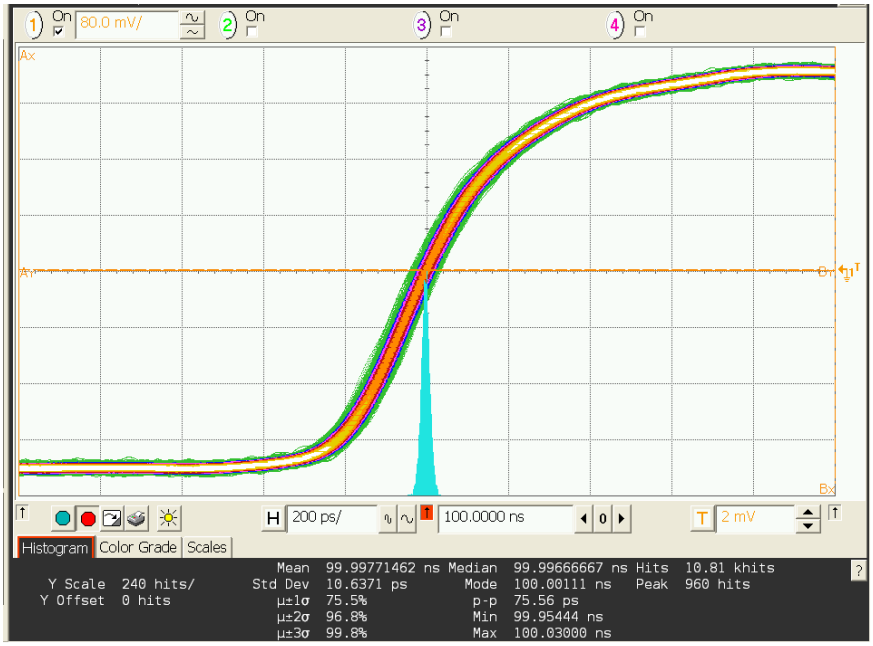
Output Clock from PL902 JitterBlocker

The JitterBlocker effectively blocks the noise and opens the eye.

Cleaning up a noisy 10MHz clock with deterministic jitter:



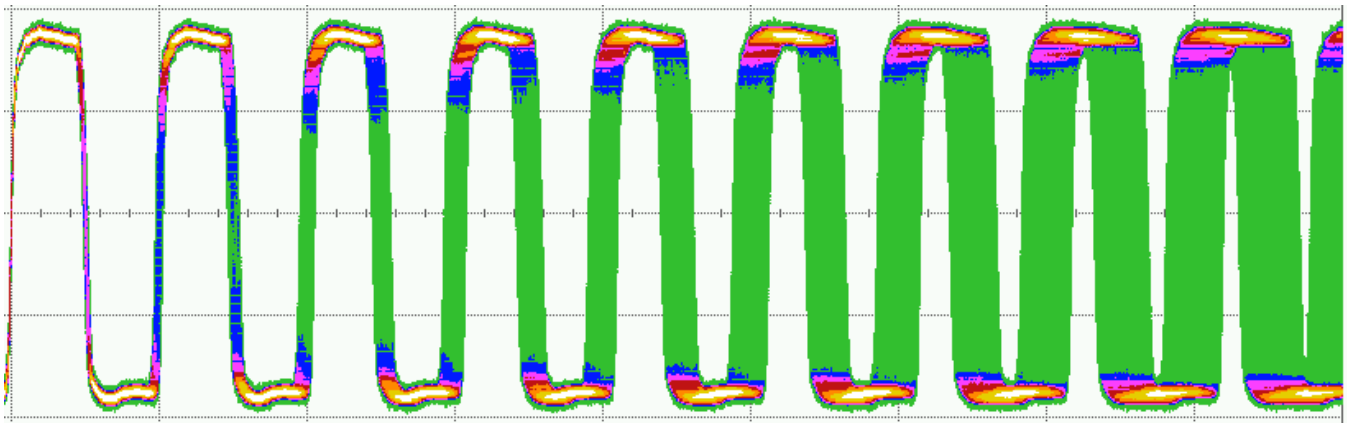
Input 10MHz with Typical Interference from Various Signals



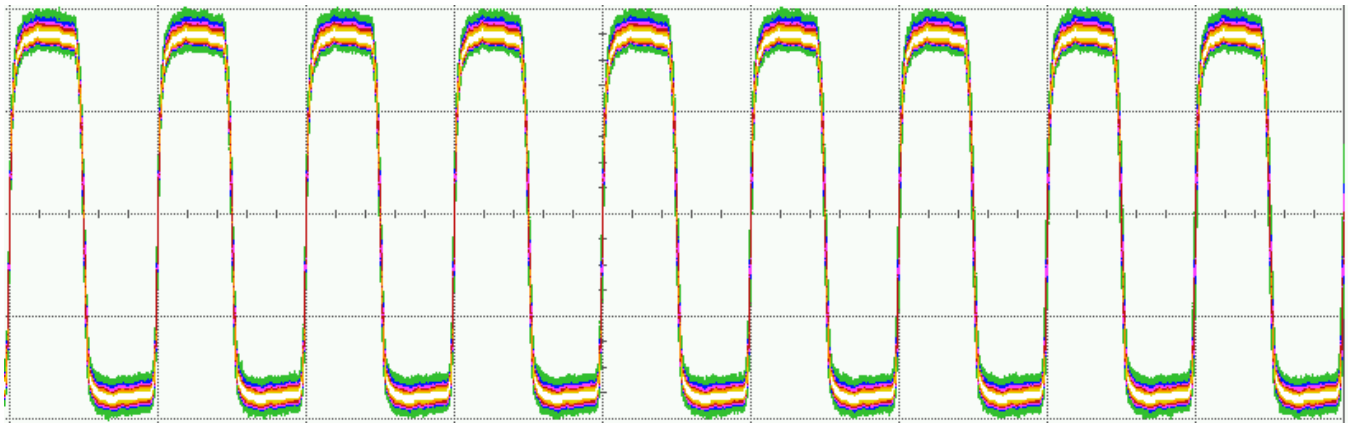
Output Clock from PL902 JitterBlocker

The noisy 10MHz clock with 460ps$_{PP}$ is cleaned up to 76ps$_{PP}$ by the JitterBlocker.

Interference with lower-frequency modulation causes jitter accumulation when looking at intervals of multiple periods. The loop bandwidth of the PL902 JitterBlocker is low enough to also block the accumulation.

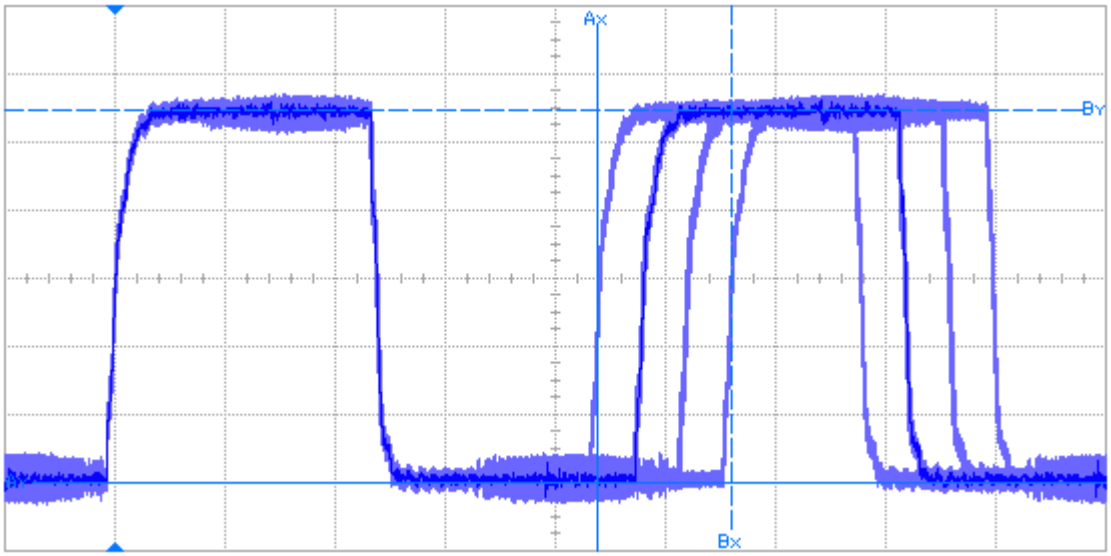


Accumulation from 100kHz Modulation in a 100MHz Clock

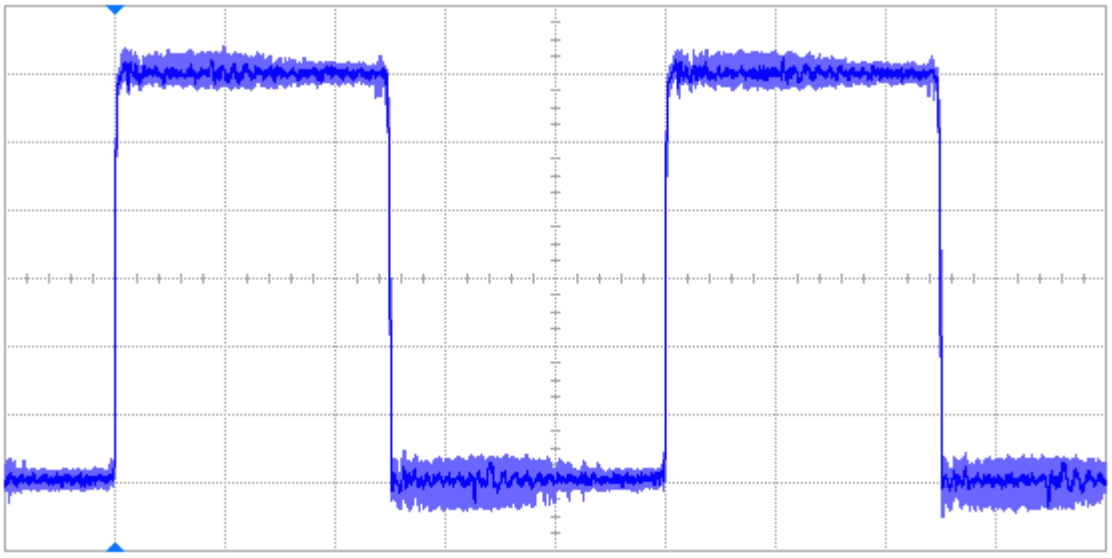


The Same Accumulation at the PL902 JitterBlocker Output

The last period jitter example is of a 10MHz precision clock from Micrel's IEEE1588 system. The clock is assembled from 8ns time slices and has very large deterministic jitter.



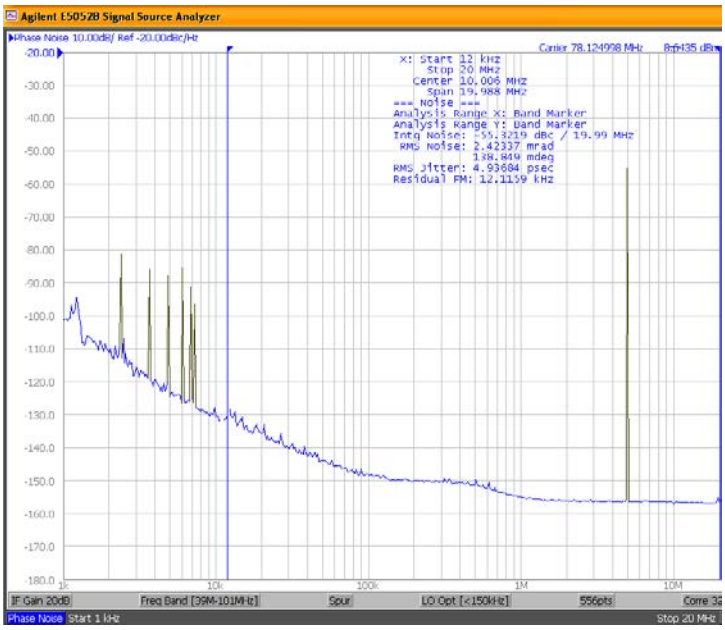
10MHz Clock from GPIO on an IEEE1588 System



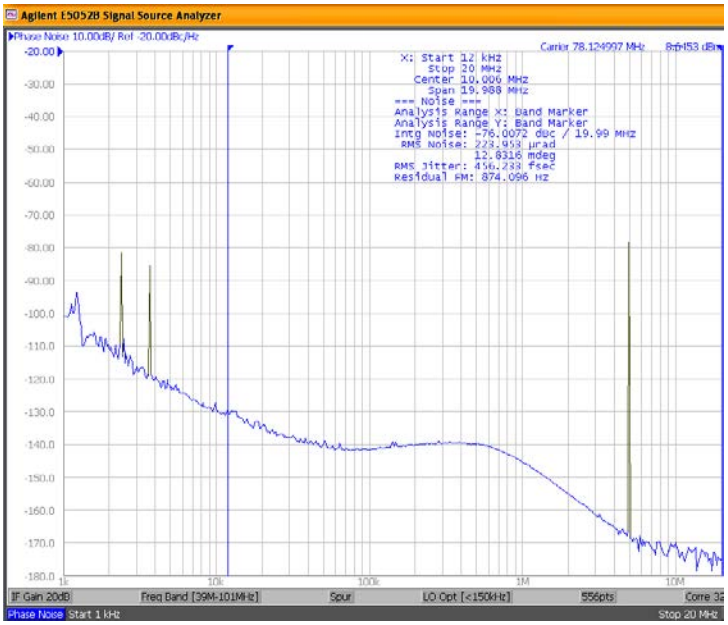
The Same Clock after Passing Through the PL902 JitterBlocker

The IEEE1588 precision clock output shows about 24ns or 24,000ps$_{PP}$ of period jitter. The JitterBlocker succeeds in removing this very large deterministic jitter and leaves only 100ps$_{PP}$ in its output signal. Now this clock can be used for many more applications than was previously possible.

The PL903 and PL904 can improve the phase noise of a clock significantly.



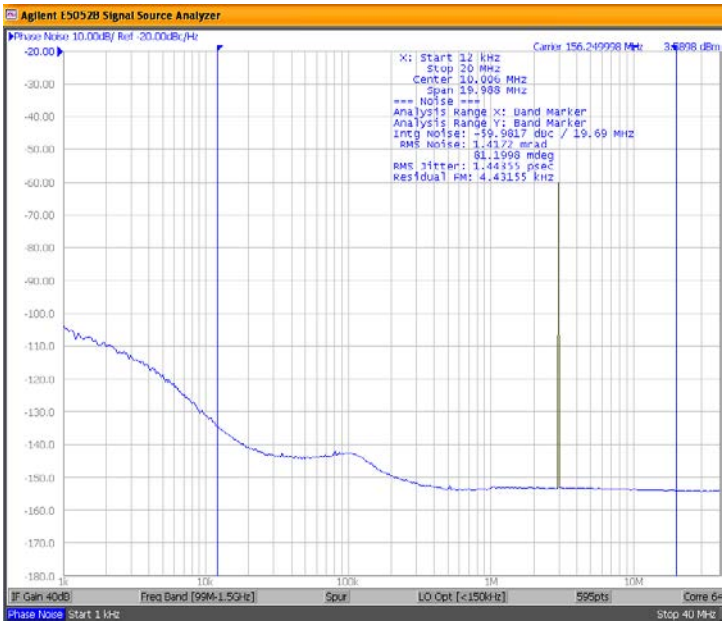
78.125MHz Clock with a Bad Spur at 5MHz, Causing 4.9ps$_{RMS}$ Phase Jitter



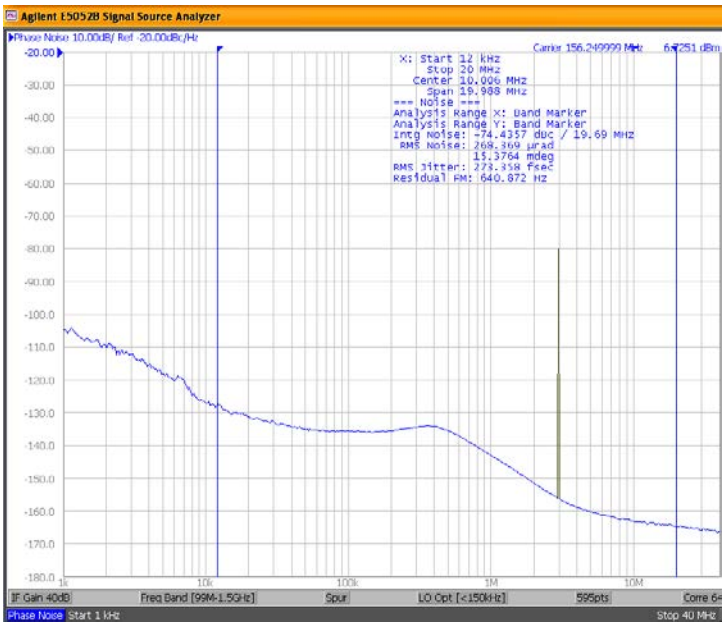
The Same Clock after Passing Through the PL903 JitterBlocker. Remaining Phase Jitter 0.46ps$_{RMS}$.

The PL903 JitterBlocker attenuated the 5MHz spur with 20dB and also lowered the phase noise floor, resulting in a factor of 10 phase jitter improvement.

The PL903 and PL904 have very similar performance. The next plots are measured with the PL904.



156.25MHz Input Clock with Bad Spur at 3MHz, Causing 1.4ps$_{RMS}$ Phase Jitter



The Same Clock after Passing Through the PL904 JitterBlocker. Remaining Phase Jitter 0.27ps$_{RMS}$

The phase noise floor of the PL903 and PL904 JitterBlockers is very low. The above plot shows the remaining phase jitter below 0.3psRMS. This means that the PL903 and PL904 JitterBlockers are suited for high speed communications applications that require very low phase jitter.

Conclusion

The PL902 JitterBlocker is a small 6-pin IC with amazing properties for removing period jitter from reference clocks. The PL902 JitterBlocker is especially suited for cleaning extremely noisy clocks with period jitter from a few hundred picoseconds peak-to-peak to thousands of picoseconds peak-to-peak. Reference clocks—from the IEEE1588 chipset, for example—can now be used for many more applications, simply by adding a little 6-pin JitterBlocker in series with the clock. The PL902 JitterBlocker output clock performance is in the 50ps to 100ps peak-to-peak region, even when the input clock has thousands of picoseconds of period jitter.

Applications that need phase noise or phase jitter improvement can use a PL903 or PL904 JitterBlocker. The PL903 and PL904 JitterBlockers will attenuate spurs and lower the phase noise floor, resulting in phase jitter reduction. The remaining phase jitter in the output clock is low enough for high speed communications applications that require very low phase jitter.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com