Zero Power HDMI® 1.3 Transmitter

A CoolHD™ family product

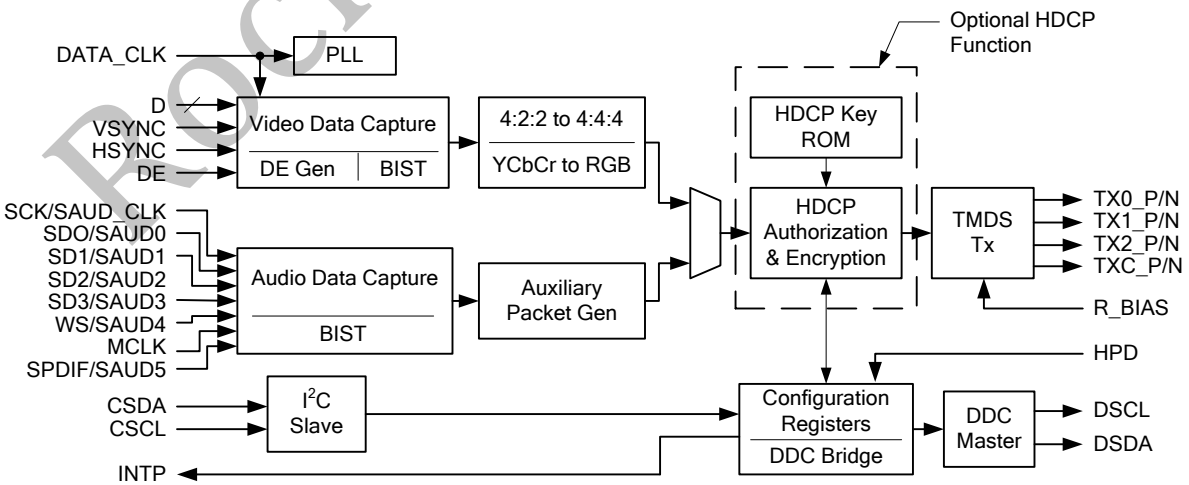
- HDMI 1.3 compatible transmitter with patented Zero power HDMI transmitter technology
- Optional HDCP function with internal keys
- Supports link date rates up to 165Mpixel/sec
- Flexible video pixel input interface, supports DVD and HD MPEG decoders
  - 24-bit RGB/YCbCr 4:4:4
  - 16/20/24-bit YCbCr 4:2:2
  - 8/10/12-bit YC Mux(ITU 601 and 656)
  - YCbCr-to-RGB colour space conversion
  - YCbCr 4:2:2 to 4:4:4 up-sample
  - 12-bit, dual-edge clocking input mode
  - 8-bit DDR YCMux (ITU 601 and 656)
- Advanced digital audio interface
  - 8-channel I^2S support Dolby Digital and DVD-Audio
  - Up to 6 channels 1-bit super audio support
  - S/PDIF supports PCM, Dolby Digital and DTS digital audio transmission
  - IEC 60958 or 61937 compatible
  - 2:1 and 4:1 down-sample to handle 96 KHz and 192 KHz audio stream
- Software-controlled power management
- Backward compatible with DVI1.1
- Programmable output swing
- 6KV ESD performance
- RoHS compliant and Halogen free package
- Package offered
  - 48-pin QFN
  - 80-pin LQFP
  - 81-pin VFBGA
  - 81-pin TFBGA

ANX7150, a CoolHD™ family product, it is a revolutionary breakthrough technology that makes a zero power HDMI transmitter a reality. CoolHD™ technology solves the problem by recovering power from the HDMI link that is normally wasted as heat and using it to power the HDMI transmitter. This technology is transforming the mobile and handheld markets.

ANX7150 can be ordered with an optional HDCP 1.2 function (including internal keys) to support content protection.

Built-in video pattern generator and audio tone generator are included for system self-test. Power requirement is 1.8V and 3.3V.

For package and HDCP options, refer to the parts ordering information.



ANX7150 Block Diagram

1 Typical Application Block Diagram

The block diagram of ANX7150 is shown in Figure 1-1. The ANX7150 chip has flexible video and audio input interfaces to receive the video and audio data from Video/Audio Processor. The ANX7150 can be controlled and configured by the system host micro controller through the dedicated host I^2C control interface. The I^2C control interface is also used to read HDMI sink E-EDID data received by DDC master through the DDC link, which means the host controller does not need extra DDC master for reading E-EDID data. The ANX7150 packages the video data, audio data and other control information into the TMDS link and generated HDMI signals that fully support HDMI 1.3 standard.

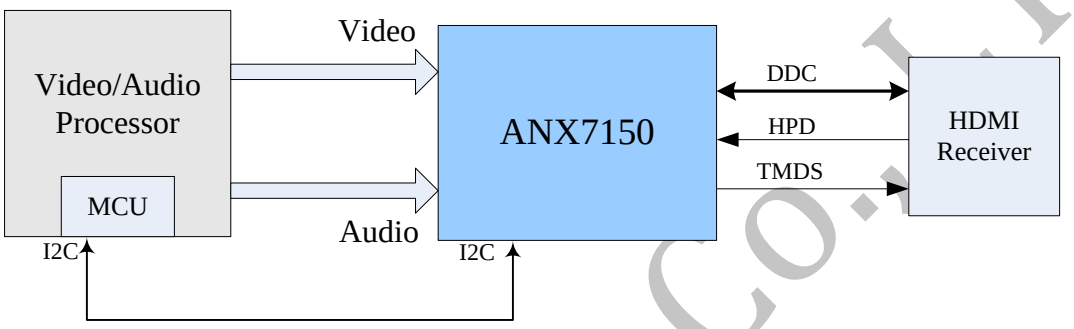


Figure 1- 1 System application of ANX7150

2 Pin Descriptions

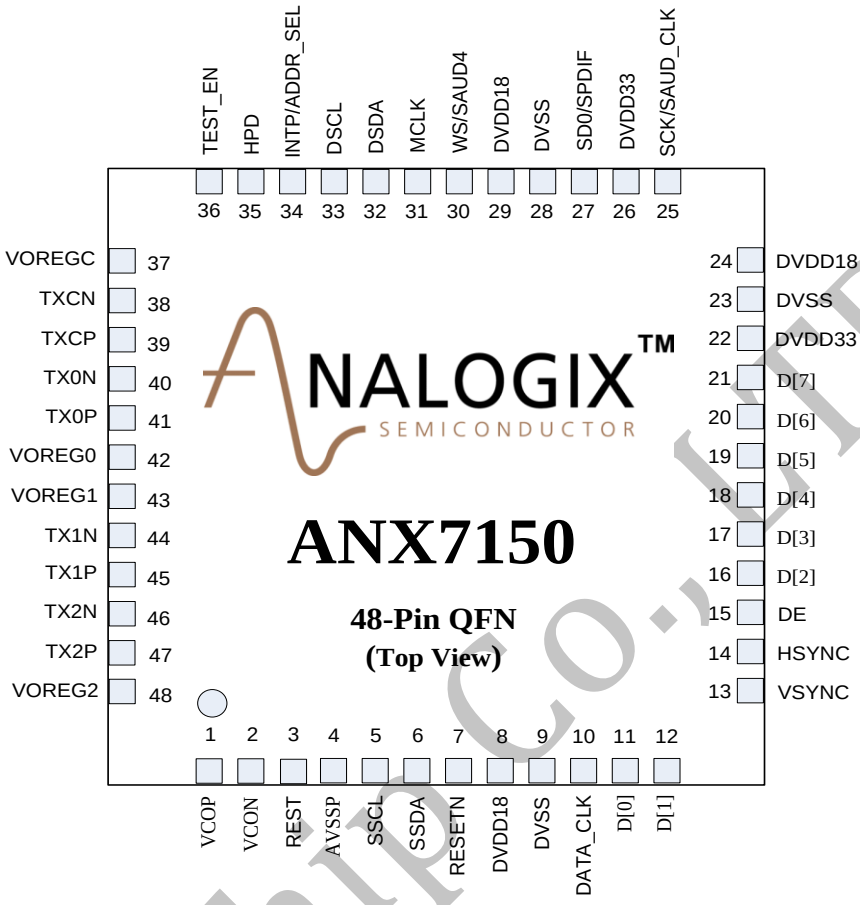


Figure 2-1 ANX7150 48-pin QFN

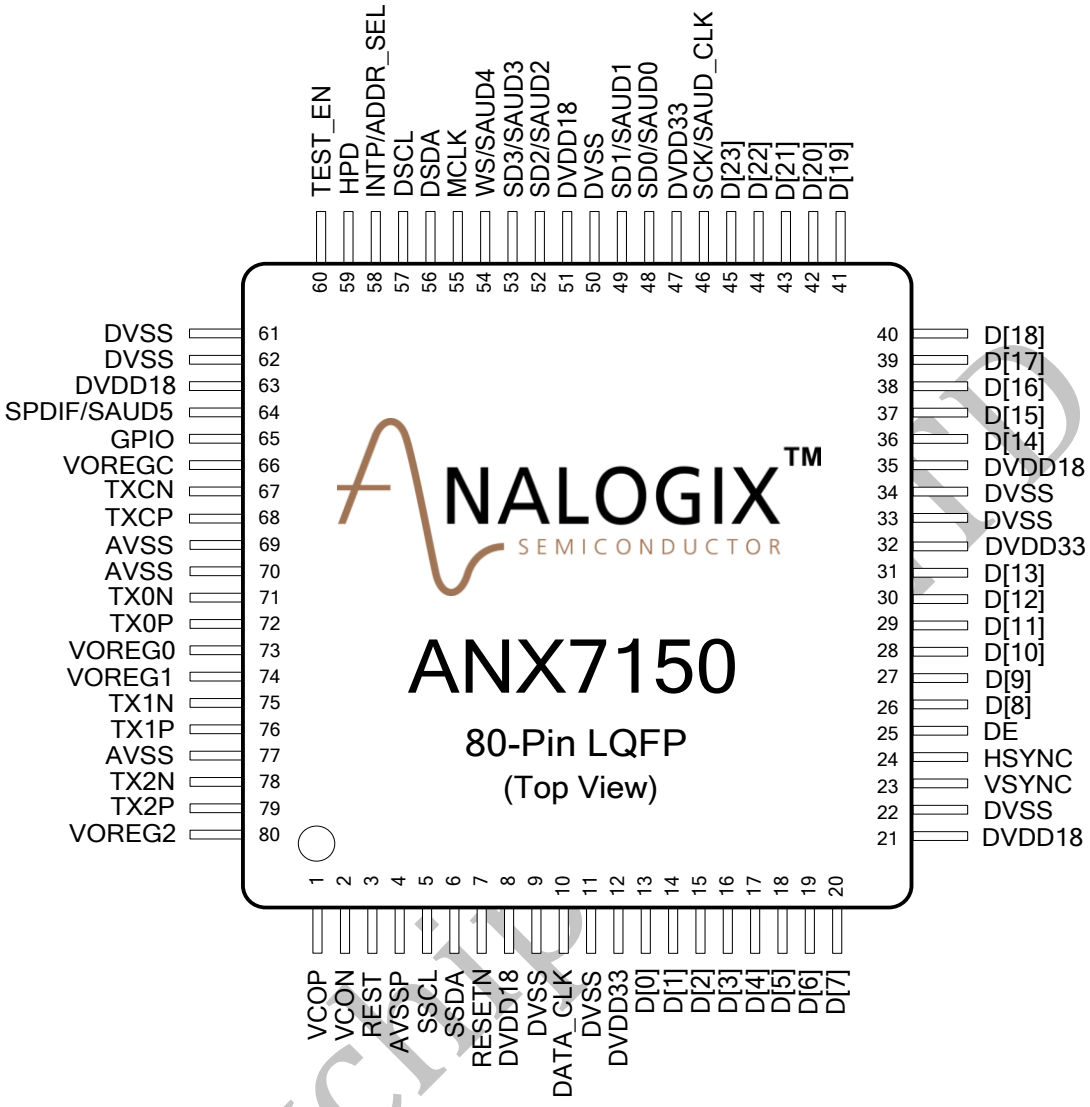


Figure 2-2 ANX7150 80-pin LQFP

	1	2	3	4	5	6	7	8	9	
A	VOREG 2	TX1P	TX1N	VOREG 1	TX0P	TX0N	AVSS	TXCP	TXCN	A
B	TX2N	AVSSP	AVSS	VOREG 0	GPIO	TEST_E N	AVSS	INTP/ ADDR_ SEL	VOREG C	B
C	TX2P	SSCL	REXT	NC	SPDIF/ SAUD5	HPD	DVSS	DSDA	DSCL	C
D	VCOP	SSDA	RESET_ N	DVSS	DVDD18	DVDD18	DVSS	MCLK	WS/SAU D4	D
E	VCON	DATA_C LK	DVDD18	DVSS	DVSS	DVSS	DVDD33	SD2/SAI D2	SD3/SA UD3	E
F	D0	D1	DVDD33	DVDD33	DVSS	DVSS	SCK/ SAUD_ CLK	SD0/SAI D0	SD1/SA UD1	F
G	D2	D3	D4	DVDD18	D12	DVDD18	D23	D22	D21	G
H	D5	D6	HSYNC	D9	D11	D14	D16	D18	D20	H
J	D7	VSYNC	DE	D8	D10	D13	D15	D17	D19	J
	1	2	3	4	5	6	7	8	9	

Figure 2-3 ANX7150 81-pin VFBGA

	1	2	3	4	5	6	7	8	9	
A	VOREG 2	TX1P	TX1N	VOREG 1	TX0P	TX0N	AVSS	TXCP	TXCN	A
B	TX2N	AVSSP	AVSS	VOREG 0	GPIO	TEST_E N	AVSS	INTP/ ADDR_ SEL	VOREG C	B
C	TX2P	SSCL	REXT	NC	SPDIF/ SAUD5	HPD	DVSS	DSDA	DSCL	C
D	VCOP	SSDA	RESET_ N	DVSS	DVDD18	DVDD18	DVSS	MCLK	WS/SAU D4	D
E	VCON	DATA_C LK	DVDD18	DVSS	DVSS	DVSS	DVDD33	SD2/SAI D2	SD3/SA UD3	E
F	D0	D1	DVDD33	DVDD33	DVSS	DVSS	SCK/ SAUD_ CLK	SD0/SAI D0	SD1/SA UD1	F
G	D2	D3	D4	DVDD18	D12	DVDD18	D23	D22	D21	G
H	D5	D6	HSYNC	D9	D11	D14	D16	D18	D20	H
J	D7	VSYNC	DE	D8	D10	D13	D15	D17	D19	J
	1	2	3	4	5	6	7	8	9	

Figure 2-4 ANX7150 81-pin TFBGA

2.1 Pin Definition

2.1.1 Video Interface Pins

Table 2-1 Video Interface Pins

81-pin VFBGA/TFBGA	80-pin	48-pin	Name	I/O	Type	Description
E2	10	10	DATA_CLK	I	LVTTL	Pixel clock input. 25 MHz ~ 165 MHz.
J3	25	15	DE	I	LVTTL	Data enable.
J2	23	13	VSYNC	I	LVTTL	Vertical sync. Input control signal.
H3	24	14	HSYNC	I	LVTTL	Horizontal sync. Input control signal.
F1,F2,G1,G2,G3,H1, H2,J1,J4,H4,J5,H5, G5,J6,H6,J7,H7,J8, H8,J9,H9,G9,G8,G7	13-20, 26-31, 36-45	11,12, 16-21	D	I	LVTTL	Pixel data input.

2.1.2 Audio Interface Pins

Table 2-2 Audio Interface Pins

81-pin VFBGA/TFBGA	80-pin	48-pin	Name	I/O	Type	Description
C5	64	NC	SPDIF/SAUD5	I	LVTTL	S/PDIF audio input or super audio input channel 5.
D8	55	31	MCLK	I	LVTTL	Audio master clock input.
F7	46	25	SCK/SAUD_CLK	I	LVTTL	I^2S audio clock or super audio clock input.
D9	54	30	WS/SAUD4	I	LVTTL	I^2S audio word select or super audio input channel 4.
E9	53	NC	SD3/SAUD3	I	LVTTL	8-channel I^2S audio data input or super audio input channel 0–3. For 48-pin QFN device, it is S/PDIF audio input.
E8	52	NC	SD2/SAUD2	I	LVTTL	
F9	49	NC	SD1/SAUD1	I	LVTTL	
F8	48	27	SD0/SAUD0 SD0/SPDIF	I	LVTTL	

2.1.3 I2C Interface Pins

Table 2-3 I2C Interface Pins

81-pin VFBGA/TFBGA	80-pin	48-pin	Name	I/O	Type	Description
C2	5	5	SSCL	I	LVTTL	Slave I^2C clock input.
D2	6	6	SSDA	I/O	LVTTL	Slave I^2C data. Open drain output.
C9	57	33	DSCL	O	LVTTL	DDC (Master I^2C) clock output.
C8	56	32	DSDA	I/O	LVTTL	DDC (Master I^2C) data. (open drain output).
B6	60	36	TEST_EN	I/O	LVTTL	Scan test enable

2.1.4 Serial Interface Pins

Table 2-4 Serial Interface Pins

81-pin VFBGA/TFBGA	80-pin	48-pin	Name	I/O	Type	Description
A5,A6	71,72	40,41	TX0N/P	O	TMDS	Channel 0 TMDS differential output.
A2,A3	75,76	44,45	TX1N/P	O	TMDS	Channel 1 TMDS differential output.
B1,C1	78,79	46,47	TX2N/P	O	TMDS	Channel 2 TMDS differential output.

A8,A9	67,68	38,39	TXCN/ P	O	TMDS	Differential TMDS clock output.

2.1.5 Miscellaneous Signal

Table 2-5 Miscellaneous Pins

81-pin VFBGA/TFBGA	80-pin	48-pin	Name	I/O	Type	Description
D3	7	7	RESETN	I	Schmitt	Reset signal, active low.
C6	59	35	HPD	I	LVTTL	Hot-plug detect signal.
B8	58	34	INTP	O	LVTTL	Interrupt output signal[1]. During chip reset, used as I^2C slave device address select
C3	3	3	REXT	I	Analog	Bias circuit resistor input, 3.5K Ohms to Ground
D1	1	1	VCOP	I	Analog	Analog filtering, positive
E1	2	2	VCON	I	Analog	Analog filtering, negative
B5	65	NC	GPIO	I	Analog	Generic purpose IO

1. The INTP pin needs a weak pull-up of approximately 10KOhm

2.1.6 Power and Ground Pins

Table 2-6 Power and Ground Pins

81-pin VFBGA/TFBGA	80-pin	48-pin	Name	Type	Description
D5,D6,E3,G4,G6	8, 21, 35, 51, 63	8, 24, 29	DVDD18	Power	1.8V core power pins
F3,F4,E7	12, 32, 47	22,26	DVDD33	Power	3.3V power pins
C7,D4,D7,E4,E5, E6,F5,F6,	9, 11, 22, 33, 34, 50, 61, 62	9, 23, 28	DVSS	Ground	Digital ground pins
A7,B7,B3,	69, 70, 77	NC	AVSS	Ground	Analog ground pins
B2	4	4	AVSSP	Ground	Analog ground pin

2.1.7 Internal Pins

Table 2-7 Internal Pins

81-pin VFBGA/TFBGA	80-pin	48-pin	Name	Type	Description
B4,A4,A1,B9	66,73,74,80	37,42,43,48	VOREG 0 VOREG 1 VOREG 2 VOREG C		Internal analog power pins, which are not provided for customer, Every pin provides internal using voltage individually.

3 Electrical Specifications

3.1 Absolute Maximum Conditions

Permanent damage may occur if absolute maximum conditions are violated. Refer to Section 3.2 for functional operating limits.

Table 3-1 Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
DVDD33	Digital I/O supply voltage	-0.3		3.8	V
DVDD18	Digital core logic supply voltage	-0.3		1.96	V
V_{IN}	Input voltage	-1.0		DVDD33+0.3	V
T_J	Junction Temperature	--		125	°C
ESD_H	ESD protection (Human body model)			6	KV

1. Power supply sequencing must guarantee these conditions.

3.2 Normal Operating Conditions

Table 3-2 Normal operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
DVDD33	Digital I/O supply voltage[1]	3.0	3.3	3.6	V
DVDD18	Digital core logic supply voltage	1.62	1.8	1.96	V
V_{RIP}	Power supply noise[2]	--	200	--	mVp-p
T_A	Ambient temperature	-10	25	75	°C

1. DVDD33 and AVDDXX should be controlled from the same power supply source.
2. Measured at the input pin after power supply filtering.

3.3 DC Specifications

These specifications apply under normal operating conditions with output pin load CL= 10pF unless otherwise stated. Minimum output drives are specified at 70 °C ambient temperature, 3.0V supply voltage. Maximum output drives are specified at 0 °C, 3.6V supply voltage.

3.3.1 Input and Output Parameters

Table 3-3 Input and output parameters

Symbol	Parameter	Min	Typ	Max	Units
V_{IH}	High level input voltage	2.0			V
V_{IL}	Low level input voltage			0.8	V
V_{T+}	Low to high threshold voltage	1.9			V
V_{T-}	High to low threshold voltage			0.7	V
V_{OH}	High level output voltage	2.4			V
V_{OL}	Low level output voltage			0.4	V
I_{IL}	Input leakage current	-10		10	uA

Symbol	Parameter	Min	Typ	Max	Units
I_{DDPD}	Output leakage current	-10		10	uA
R_{PD}	Internal pull-down resistor		83		KΩ
I_{OPD}	Output pull-down current		60	75	uA
I_{IPD}	Input pull-down current		60	75	uA

3.3.2 Power Consumption

Current consumption is a function of the link frequency of the selected HDMI input.

Table 3-4 Power Consumptions

Item	Typical Values [1]		Total Power	Units
	DVDD33	DVDD18		
Stand-by(No AV input)	0.38	0.12	1.08	mW
720*480p@60Hz, 27MHz	0.25	0	0.9	mW
1280*720p@60Hz, 74.25MHz	0.33	0	1.1	mW

1 . All the data in the table above is the typical value, but not worst case power consumptions.

Table 3-5 Standby Power Consumption [1]

Video pattern	DVDD33 (V)	3.3 (mA)	DVDD18 (V)	1.8 (mA)	Power (mW)
Video format: **1080p**					
Color bar	3.078	0.18	1.573	0.45	1.27
Grill (toggle max)	3.020	0.88	1.546	1.12	4.39
Windows desktop	3.068	0.22	1.571	0.49	1.45
Video format: **720p**					
Color bar	3.092	0.14	1.575	0.40	1.07
Grill (toggle max)	3.082	0.42	1.559	0.7	2.39
Windows desktop	3.078	0.18	1.574	0.44	1.25
Video format: **480p**					
Color bar	3.095	0.11	1.578	0.37	0.93
Grill (toggle max)	3.086	0.23	1.570	0.49	1.48
Windows desktop	3.090	0.13	1.578	0.39	1.02

1. This table just shows the standby power consumption when the input is active.

3.3.3 Slave I²C Interface Specifications

The I2C Interface operates at a reduced signaling level to better match the operating voltages of the Intel® product. The specifications for the reduced operating voltage are provided in Table 3-6. In addition, the Slave I2C Interface must be compliant with the AC specifications provided in the I2C-Bus Specification.

Table 3-6 Slave I2C DC Specifications

Symbol	Parameter	Min	Typ	Max	Units
V_{IN}	Input voltage range	-0.25	--	3.6	V
V_{IL}	Low level input voltage	--	--	0.3	V
V_{IH}	High level input voltage	0.8	--	--	V
V_{OL}	Low level output voltage	--	--	0.2	V
I_{IL}	Input leakage current (Hi-Z)	--	--	50	uA
Z_{OUT}	Output impedance	--	--	50	ohms
C_{IN}	Input capacitance	--	--	3.0	pF
C_L	I2C signal load capacitance	--	--	20	pF

3.4 AC Specifications

3.4.1 HDMI Output Timing

These specifications apply under normal operating conditions with output pin load C_L = 10 pF unless otherwise stated.

Table 3-7 HDMI Output Timings

Symbol	Parameter	Min	Typ	Max	Units
S_{LH}	TMDS differential output rise time (20%-80%) [1]	100			ps
				0.25	T_{BIT} [2]
S_{HL}	TMDS differential output fall time (80%-20%)	80			ps
				0.2	T_{BIT}
T_{SDF}	Delay from DE falling edge to VSYNC or HSYNC rising edge	1			T_{CP}
T_{SDR}	Delay from VSYNC or HSYNC falling edge to DE rising edge	1			T_{CP}

1. Limits are defined by the HDMI Specification.
2. T_{BIT} is the time required to carry a single bit across an HDMI channel, and is governed by the active input clock. (10 x T_{BIT}) = T_{CP}

3.4.2 Digital Video Data Input Timing

These specifications apply under normal operating conditions with output pin load C_L = 10 pF unless otherwise stated.

Table 3-8 Digital Video Input Timing

Symbol	Parameter	Min	Typ	Max	Units
T_{CDC}	DATA_CLK input duty cycle	15		85	%
T_{CJ}	DATA_CLK input peak-to-peak jitter tolerance [1]			2	ns
Single-edge clock mode (one pixel per clock)					
T_{CP}	Clock period of DATA_CLK	5.56		40	ns
f_{CP}	Clock frequency of DATA_CLK	25		180	MHz
T_{DSF}	Data set-up time to DATA_CLK falling edge	0.6			ns
T_{DHF}	Data hold time from DATA_CLK falling edge	1			ns
T_{DSR}	Data set-up time to DATA_CLK rising edge	0.6			ns
T_{DHR}	Data hold time from DATA_CLK rising edge	1			ns
Dual-edge clock mode (DDR Mode)					
T_{CPD}	Clock period of DATA_CLK, DDR input mode	11.12		80	ns
f_{CPD}	Clock frequency of DATA_CLK, DDR input mode	12.5		90	MHz

T_{DSD}	Data set-up time to DATA_CLK rising or falling edge	0.6			ns
T_{DHD}	Data hold time from DATA_CLK rising or falling edge	1			ns

1. Actual jitter tolerance may be higher depending on jitter phase modulation frequency.

3.4.3 Audio Data Input Timing

3.4.3.1 I²S Input Port Timing

These specifications apply under normal operating conditions with output pin load C_L = 10 pF unless otherwise stated.

Table 3-9 Audio Data Input Timing

Symbol	Parameter	Min	Typ	Max	Units
F_{SI2S}	Audio Sample Rate (2 channels)	32		192	kHz
	Audio Sample Rate (>2 channels)	32		192	kHz
T_{CYCI2S}	Cycle Time			1	UI
T_{DCI2S}	Clock duty cycle	90%		110%	UI
T_{SUI2S}	Set-up time	5			ns
T_{HI2S}	Hold time	1.5			ns

3.4.3.2 S/PDIF Input Port Timing

These specifications apply under normal operating conditions with output pin load C_L = 10 pF unless otherwise stated.

Table 3-10 S/PDIF Input Port Timing

Symbol	Parameter	Min	Typ	Max	Units
F_{SSPDIF}	Audio Sample Rate (2 channels)	32		192	kHz
T_{SPCYC}	S/PDIF cycle time[1]			1	UI
$T_{DC, SPDIF}$	S/PDIF duty cycle	90		110	%UI
T_{MCLK}	MCLK cycle time	20.8			ns
f_{MCLK}	MCLKOUT frequency			48	MHz
T_{DCMCLK}	MCLKOUT duty cycle	30		70	%
T_{DLYAUD}	Audio pipeline delay		30	70	µs

1. S/PDIF cycle time is proportional to audio sample rate.

4 Functional Descriptions

4.1 Video Capture Input Modes

Video data can be input to the ANX7150 in various 12-bit or 24-bit interface formats. Single or dual-edge clock latching is supported. Pixel rates up to 165 MHz enables video formats such as 1080p and WUXGA (1920x 1200 at 60 Hz) with reduced blanking. HSYNC and VSYNC inputs are provided, or embedded sync can be detected when using ITU.656 format. A DE input is also provided, or a DE blanking period can be generated internally based on HSYNC timing and register settings. To comply with the 4:4:4 RGB output base level requirement of HDMI, a 4:2:2 to 4:4:4 sample rate interpolation filter is included, as well as an YCbCr to RGB color-space converter; either ITU.601 or ITU.709 color-matrix coefficients can be selected.

4.2 Video Capture Input Modes

The video capture logic receives the video data from the 24-bit video interface. The interface is configured by registers to set the bus width and format as well as rising and falling edge latching. Several video input formats are supported; these and their respective pixel bit mapping are listed in the following tables.

4.2.1 RGB and YCbCr 4:4:4 Formats

Table 4-1 RGB and YCbCr 4:4:4 Formats with Separate Sync (24-bpp mode)

Pin Name	24-Bit RGB	24-Bit YCbCr
D0	B0	Cb0
D1	B1	Cb1
D2	B2	Cb2
D3	B3	Cb3
D4	B4	Cb4
D5	B5	Cb5
D6	B6	Cb6
D7	B7	Cb7
D8	G0	Y0
D9	G1	Y1
D10	G2	Y2
D11	G3	Y3
D12	G4	Y4
D13	G5	Y5
D14	G6	Y6
D15	G7	Y7
D16	R0	Cr0
D17	R1	Cr1
D18	R2	Cr2
D19	R3	Cr3
D20	R4	Cr4
D21	R5	Cr5
D22	R6	Cr6
D23	R7	Cr7

Pin Name	24-Bit RGB	24-Bit YCbCr
HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC
DE	DE	DE

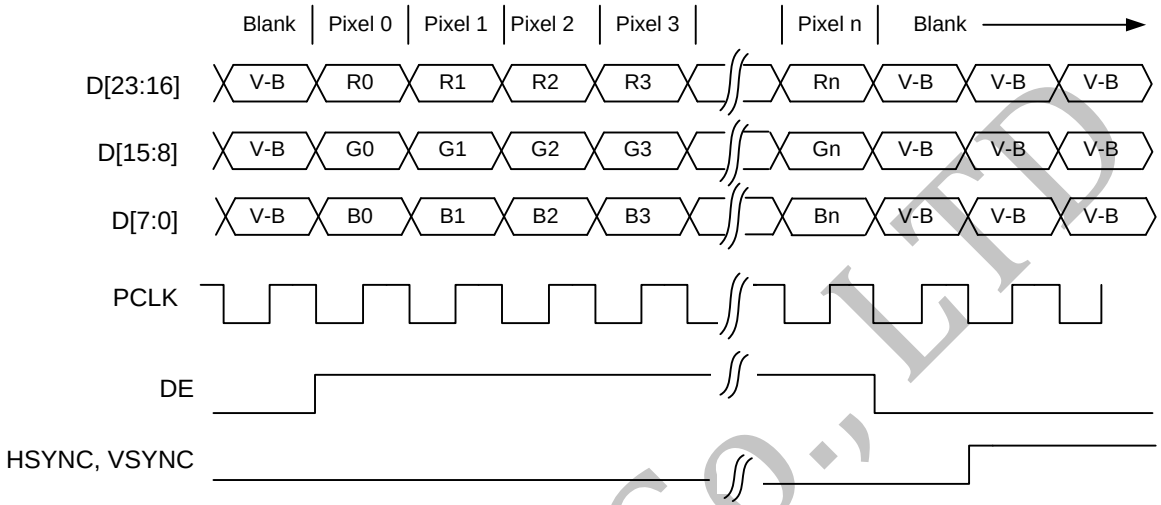


Figure 4-1 RGB 4:4:4 SDR Input Timing

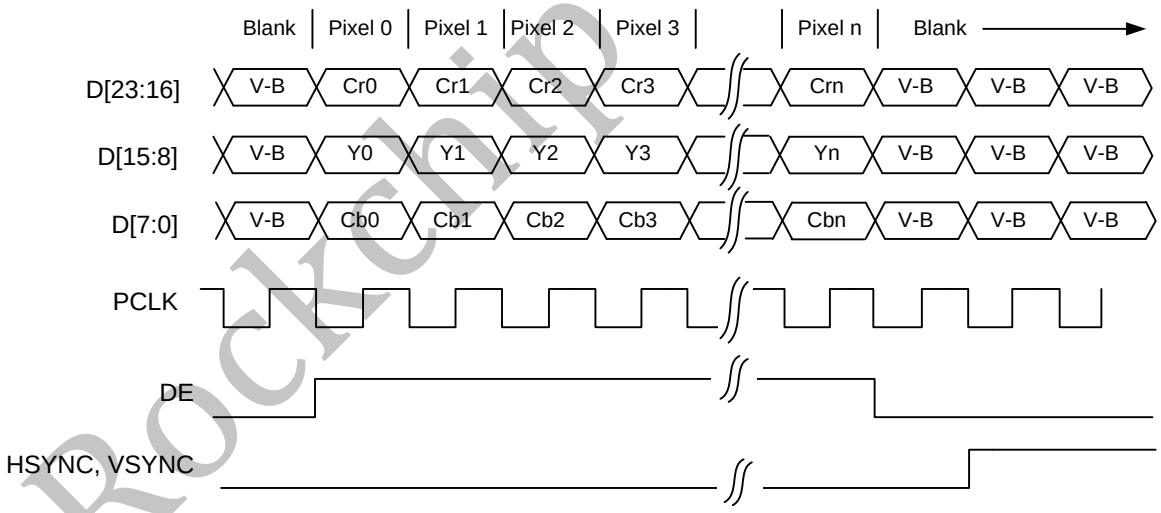


Figure 4-2 YCbCr 4:4:4 SDR Input Timing

4.2.2 YCbCr 4:2:2 Formats

Table 4-2 YCbCr 4:2:2 Formats with Separate Sync

Pin Name	16-Bit YC		20-Bit YC		24-Bit YC	
	Pixel0	Pixel1	Pixel0	Pixel1	Pixel0	Pixel1
D0	GND	GND	GND	GND	Y0	Y0
D1	GND	GND	GND	GND	Y1	Y1
D2	GND	GND	Y0	Y0	Y2	Y2
D3	GND	GND	Y1	Y1	Y3	Y3

Pin Name	16-Bit YC		20-Bit YC		24-Bit YC	
	Pixel0	Pixel1	Pixel0	Pixel1	Pixel0	Pixel1
D4	GND	GND	GND	GND	Cb0	Cr0
D5	GND	GND	GND	GND	Cb1	Cr1
D6	GND	GND	Cb0	Cr0	Cb2	Cr2
D7	GND	GND	Cb1	Cr1	Cb3	Cr3
D8	Y0	Y0	Y2	Y2	Y4	Y4
D9	Y1	Y1	Y3	Y3	Y5	Y5
D10	Y2	Y2	Y4	Y4	Y6	Y6
D11	Y3	Y3	Y5	Y5	Y7	Y7
D12	Y4	Y4	Y6	Y6	Y8	Y8
D13	Y5	Y5	Y7	Y7	Y9	Y9
D14	Y6	Y6	Y8	Y8	Y10	Y10
D15	Y7	Y7	Y9	Y9	Y11	Y11
D16	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
D17	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
D18	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
D19	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
D20	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
D21	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
D22	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
D23	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

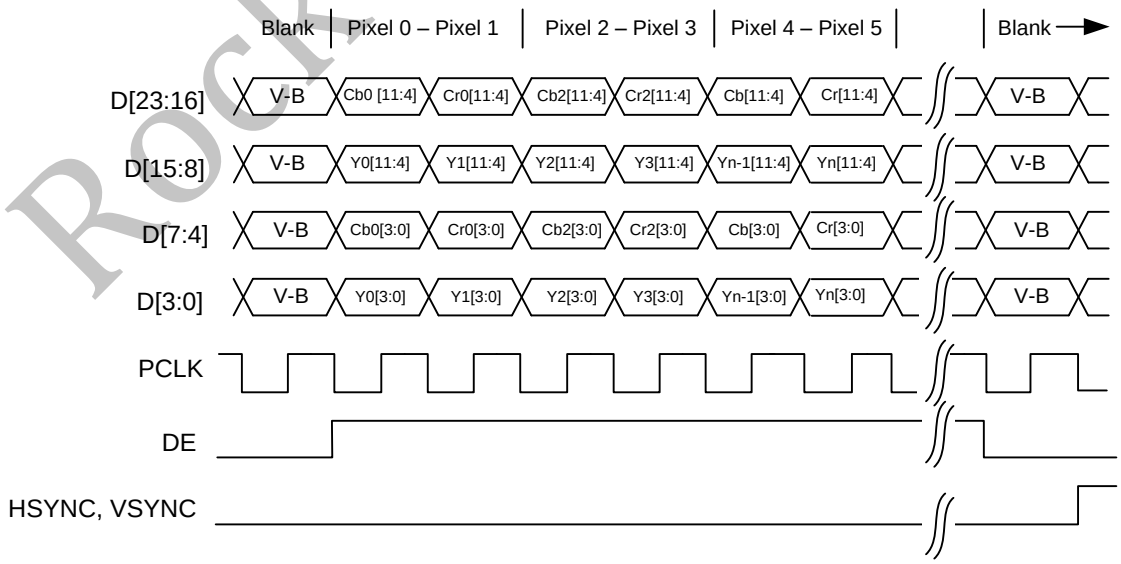


Figure 4-3 YCbCr 4:2:2 Input Timing with Separate Sync

Table 4-3 YCbCr 4:2:2 Formats with Embedded Sync

Pin Name	16-Bit YC		20-Bit YC		24-Bit YC	
	Pixel0	Pixel1	Pixel0	Pixel1	Pixel0	Pixel1
D0	GND	GND	GND	GND	Y0	Y0
D1	GND	GND	GND	GND	Y1	Y1
D2	GND	GND	Y0	Y0	Y2	Y2
D3	GND	GND	Y1	Y1	Y3	Y3
D4	GND	GND	GND	GND	Cb0	Cr0
D5	GND	GND	GND	GND	Cb1	Cr1
D6	GND	GND	Cb0	Cr0	Cb2	Cr2
D7	GND	GND	Cb1	Cr1	Cb3	Cr3
D8	Y0	Y0	Y2	Y2	Y4	Y4
D9	Y1	Y1	Y3	Y3	Y5	Y5
D10	Y2	Y2	Y4	Y4	Y6	Y6
D11	Y3	Y3	Y5	Y5	Y7	Y7
D12	Y4	Y4	Y6	Y6	Y8	Y8
D13	Y5	Y5	Y7	Y7	Y9	Y9
D14	Y6	Y6	Y8	Y8	Y10	Y10
D15	Y7	Y7	Y9	Y9	Y11	Y11
D16	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
D17	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
D18	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
D19	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
D20	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
D21	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
D22	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
D23	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	GND	GND	GND	GND	GND	GND
VSYNC	GND	GND	GND	GND	GND	GND
DE	GND	GND	GND	GND	GND	GND

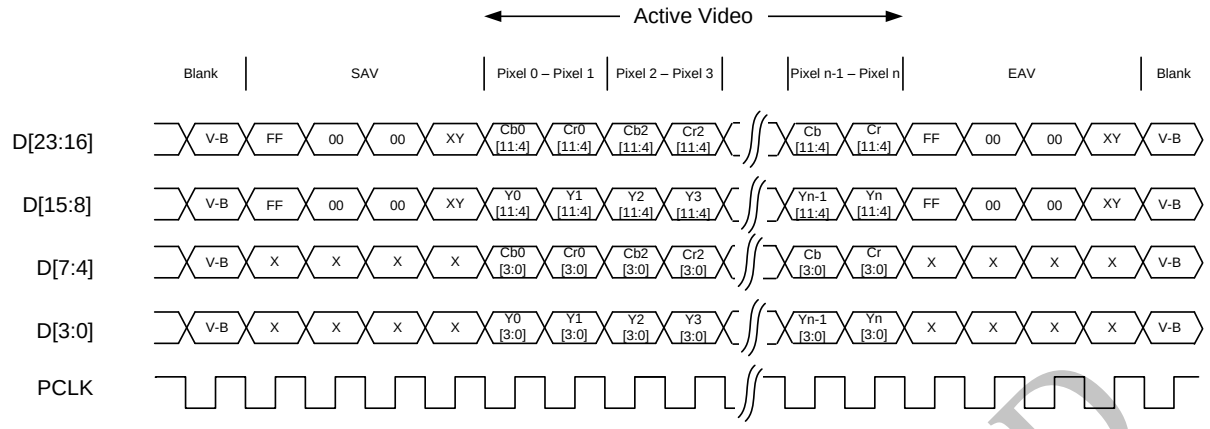


Figure 4-4 YCbCr 4:2:2 with Embedded Sync

4.2.3 YC Mux 4:2:2 Formats

Table 4-4 YC Mux 4:2:2 Formats with Separate Sync (bit-mapping option 1)

Pin Name	8-Bit YC		10-Bit YC		12-Bit YC	
	1st clk	2nd clk	1st clk	2nd clk	1st clk	2nd clk
D0	GND	GND	GND	GND	C0	Y0
D1	GND	GND	GND	GND	C1	Y1
D2	GND	GND	C0	Y0	C2	Y2
D3	GND	GND	C1	Y1	C3	Y3
D4	GND	GND	GND	GND	GND	GND
D5	GND	GND	GND	GND	GND	GND
D6	GND	GND	GND	GND	GND	GND
D7	GND	GND	GND	GND	GND	GND
D8	C0	Y0	C2	Y2	C4	Y4
D9	C1	Y1	C3	Y3	C5	Y5
D10	C2	Y2	C4	Y4	C6	Y6
D11	C3	Y3	C5	Y5	C7	Y7
D12	C4	Y4	C6	Y6	C8	Y8
D13	C5	Y5	C7	Y7	C9	Y9
D14	C6	Y6	C8	Y8	C10	Y10
D15	C7	Y7	C9	Y9	C11	Y11
D16	GND	GND	GND	GND	GND	GND
D17	GND	GND	GND	GND	GND	GND
D18	GND	GND	GND	GND	GND	GND
D19	GND	GND	GND	GND	GND	GND
D20	GND	GND	GND	GND	GND	GND
D21	GND	GND	GND	GND	GND	GND
D22	GND	GND	GND	GND	GND	GND
D23	GND	GND	GND	GND	GND	GND
HSYNC	HSYNC		HSYNC		HSYNC	

Pin Name	8-Bit YC		10-Bit YC		12-Bit YC	
	1st clk	2nd clk	1st clk	2nd clk	1st clk	2nd clk
VSYNC	VSYNC		VSYNC		VSYNC	
DE	DE		DE		DE	

Table 4-5 YC Mux 4:2:2 Formats with Separate Sync (bit-mapping option 2)

Pin Name	8-Bit YC		10-Bit YC		12-Bit YC	
	1st clk	2nd clk	1st clk	2nd clk	1st clk	2nd clk
D0	GND	GND	GND	GND	C0	Y0
D1	GND	GND	GND	GND	C1	Y1
D2	GND	GND	C0	Y0	C2	Y2
D3	GND	GND	C1	Y1	C3	Y3
D4	C0	Y0	C2	Y2	C4	Y4
D5	C1	Y1	C3	Y3	C5	Y5
D6	C2	Y2	C4	Y4	C6	Y6
D7	C3	Y3	C5	Y5	C7	Y7
D8	C4	Y4	C6	Y6	C8	Y8
D9	C5	Y5	C7	Y7	C9	Y9
D10	C6	Y6	C8	Y8	C10	Y10
D11	C7	Y7	C9	Y9	C11	Y11
HSYNC	HSYNC		HSYNC		HSYNC	
VSYNC	VSYNC		VSYNC		VSYNC	
DE	DE		DE		DE	

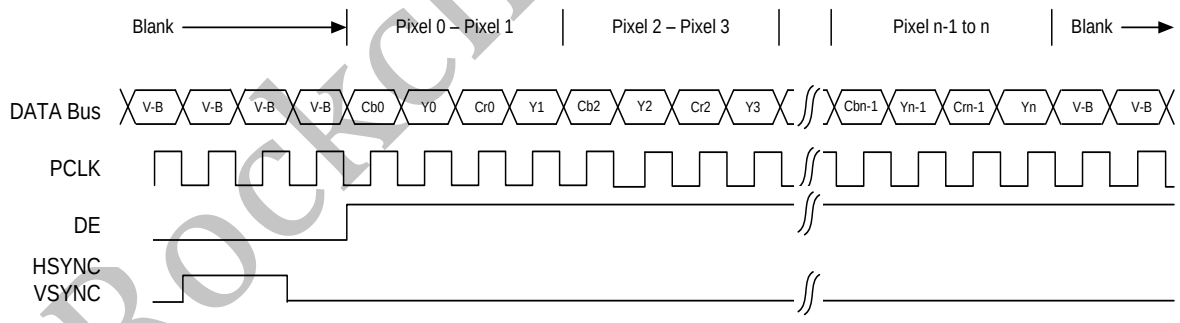


Figure **4-5** YC Mux 4:2:2 with Separate Sync

4.2.4 12-Bit RGB and YCbCr 4:4:4 DDR Formats with Separate Sync

Table 4-6 12-bit RGB and YCbCr 4:4:4 DDR Formats with Separate Sync. (24-bpp)

Pin Name	12-Bit RGB		12-Bit YCbCr	
	1st edge	2nd edge	1st edge	2nd edge
D0	B0	G4	Cb0	Y4
D1	B1	G5	Cb1	Y5
D2	B2	G6	Cb2	Y6
D3	B3	G7	Cb3	Y7

Pin Name	12-Bit RGB		12-Bit YCbCr	
	1st edge	2nd edge	1st edge	2nd edge
D4	B4	R0	Cb4	Cr0
D5	B5	R1	Cb5	Cr1
D6	B6	R2	Cb6	Cr2
D7	B7	R3	Cb7	Cr3
D8	G0	R4	Y0	Cr4
D9	G1	R5	Y1	Cr5
D10	G2	R6	Y2	Cr6
D11	G3	R7	Y3	Cr7
HSYNC	HSYNC		HSYNC	
VSYNC	VSYNC		VSYNC	
DE	DE		DE	

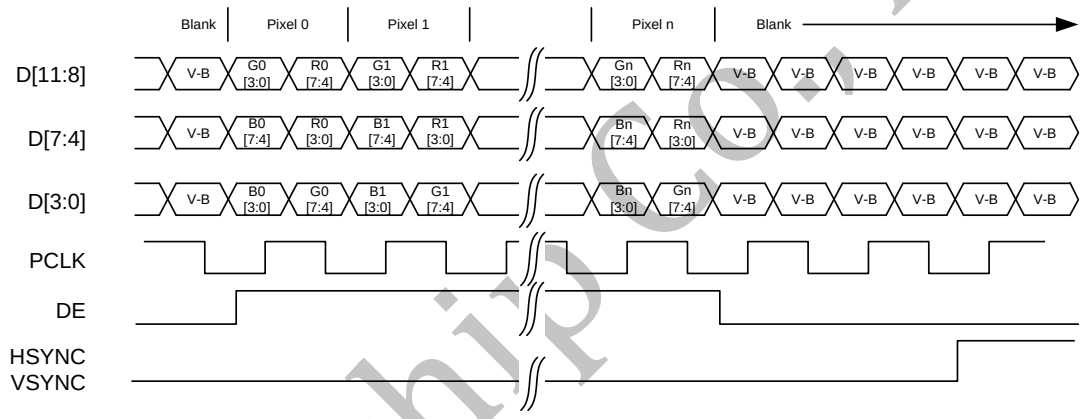


Figure 4-6 12-Bit RGB 4:4:4 DDR Input Timing with Separate Sync

Table 4-7 12-bit RGB2 4:4:4 DDR Format with Separate Sync. (24-bpp)

Pin Name	12-Bit RGB	
	1st edge	2nd edge
D0	B0	G1
D1	B1	R0
D2	B2	R1
D3	G0	R2
D4	B3	G5
D5	B4	G6
D6	B5	G7
D7	B6	R3
D8	B7	R4
D9	G2	R5
D10	G3	R6
D11	G4	R7

Pin Name	12-Bit RGB	
	1st edge	2nd edge
HSYNC	HSYNC	
VSYNC	VSYNC	
DE	DE	

Table 4-8 12-bit RGB and YCbCr 4:4:4 Formats with Separate Sync. (18-bpp)

Pin Name	12-Bit RGB		12-Bit YCbCr	
	1st edge	2nd edge	1st edge	2nd edge
D0	GND	G2	GND	Y2
D1	GND	G3	GND	Y3
D2	B0	G4	Cb0	Y4
D3	B1	G5	Cb1	Y5
D4	B2	GND	Cb2	GND
D5	B3	GND	Cb3	GND
D6	B4	R0	Cb4	Cr0
D7	B5	R1	Cb5	Cr1
D8	GND	R2	GND	Cr2
D9	GND	R3	GND	Cr3
D10	G0	R4	Y0	Cr4
D11	G1	R5	Y1	Cr5
HSYNC	HSYNC		HSYNC	
VSYNC	VSYNC		VSYNC	
DE	DE		DE	

4.3 DE Generator and Video BIST Function

The ANX7150 chip includes logic to construct a DE signal from the incoming HSYNC, VSYNC and clock. Registers are programmed to enable this DE signal to define the size of the active display region. This feature is useful when interfacing to MPEG decoders which do not provide a specific DE output signal.

The video BIST function within this block internally generates several of the most popular video formats according to the specified format selection. These BIST video formats simplify the chip debug.

4.4 Audio Capture and Audio BIST

The audio capture block takes the S/PDIF, I^2S or Super-audio input. The S/PDIF stream can carry two-channel uncompressed PCM data (IEC 60958) or a compressed bit stream for multi-channel (IEC 61937) formats. The audio data capture logic forms the audio data into packets in accordance with the HDMI 1.3 specification. The audio capture block supports audio sampling rates from 32 kHz to 192 kHz.

The appropriate registers must be configured to accept the input audio format. This information is passed over the HDMI link in the CEA-861B Audio Info packets.

The audio BIST function in this block generates sine wave with controllable amplitude and frequency. It is used conveniently to test the audio output of the HDMI receiver. The sine wave amplitude and frequency are set by the registers.

4.5 HDMI Processor Datapath

The HDMI processor block takes the video data from the video capture block and passes it through a video data repeater block. The video data is repeated if it is 2X or 4X mode. The color space converter and up converter that follow convert the video data if necessary. The audio data from the audio FIFO passes to the Aux. Packet generator block and merges with the video data to form the HDMI link frame. The link data is encoded with the TMDS encoder and traverses an output FIFO to perform clock domain conversion. The output of the FIFO is synchronized with the 'tx_clk' from the transmitter analog core.

4.5.1 HDCP Encryption Engine/XOR Mask

The HDCP encryption engine contains all necessary logic to encrypt the incoming audio and video data. The encryption process is entirely controlled by the system microcontroller/microprocessor through a set sequence of register reads and writes. Preprogrammed HDCP keys and Key Selector Value (KSV) stored in the internal EEPROM are used in the encryption process. A resulting calculated value is applied to an XOR mask during each clock cycle to encrypt the audio/video data.

4.5.2 TMDS Encoder

The TMDS encoder performs 8-to-10-bit TMDS encoding on the audio/video/aux data received from the HDCP XOR mask. This data is output to three TMDS differential data lines along with a TMDS differential clock.

4.5.3 HDCP Key EEPROM

The ANX7150 comes pre-programmed with a set of production HDCP keys stored in the internal EEPROM. System manufacturers do not need to purchase key sets from the Digital-Content LLC. The pre-programmed HDCP keys provide the highest level of security, as there is no way to read out the keys once the devices are programmed.

4.5.4 Interrupt Output

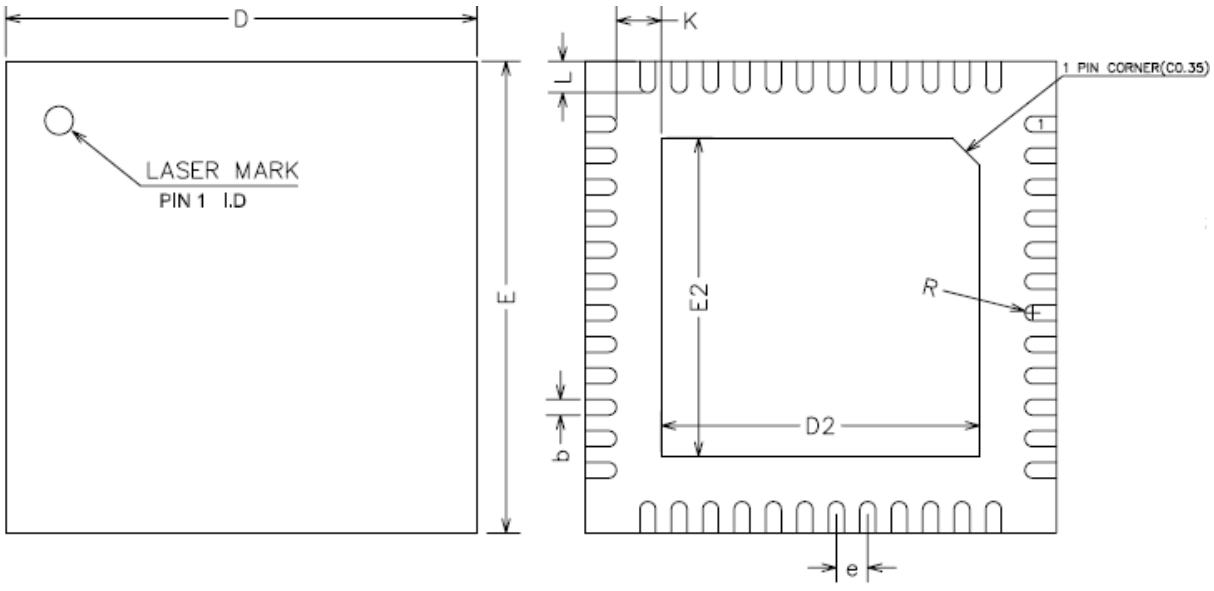
The INTP pin outputs a signal to interrupt the microcontroller on conditions inside the ANX7150, including:

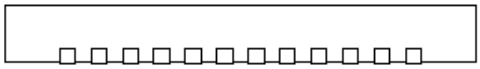
- Monitor Detect (either from the HPD input level, or from the Receiver Sense feature)
- VSYNC (useful for synchronizing a microcontroller to the vertical timing interval)
- Error in the audio format

A connected display may be detected with the internal Receiver Sense logic. This is useful to the host controller monitoring the chip. The state of Receiver Sense may be output on the INTP pin as a level or as an interrupt of either polarity.

5 Package Specifications

5.1 ANX7150 48-Pin QFN Package Drawings





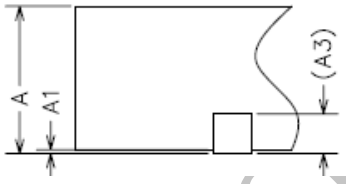


Figure 5-1 ANX7150 48-pin QFN Package

ANX7150 48-PIN QFN Package Dimensions

Ref	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 Ref	
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	3.95	4.05	4.15
E2	3.95	4.05	4.15
e	0.35	0.40	0.45
K	0.20	-	-
L	0.35	0.40	0.45

R	0.09	-	-

Notes:

All dimensions conform to JEDEC Standard MO-220 WJJE.

5.2 ANX7150 80-Pin LQFP Package Drawings

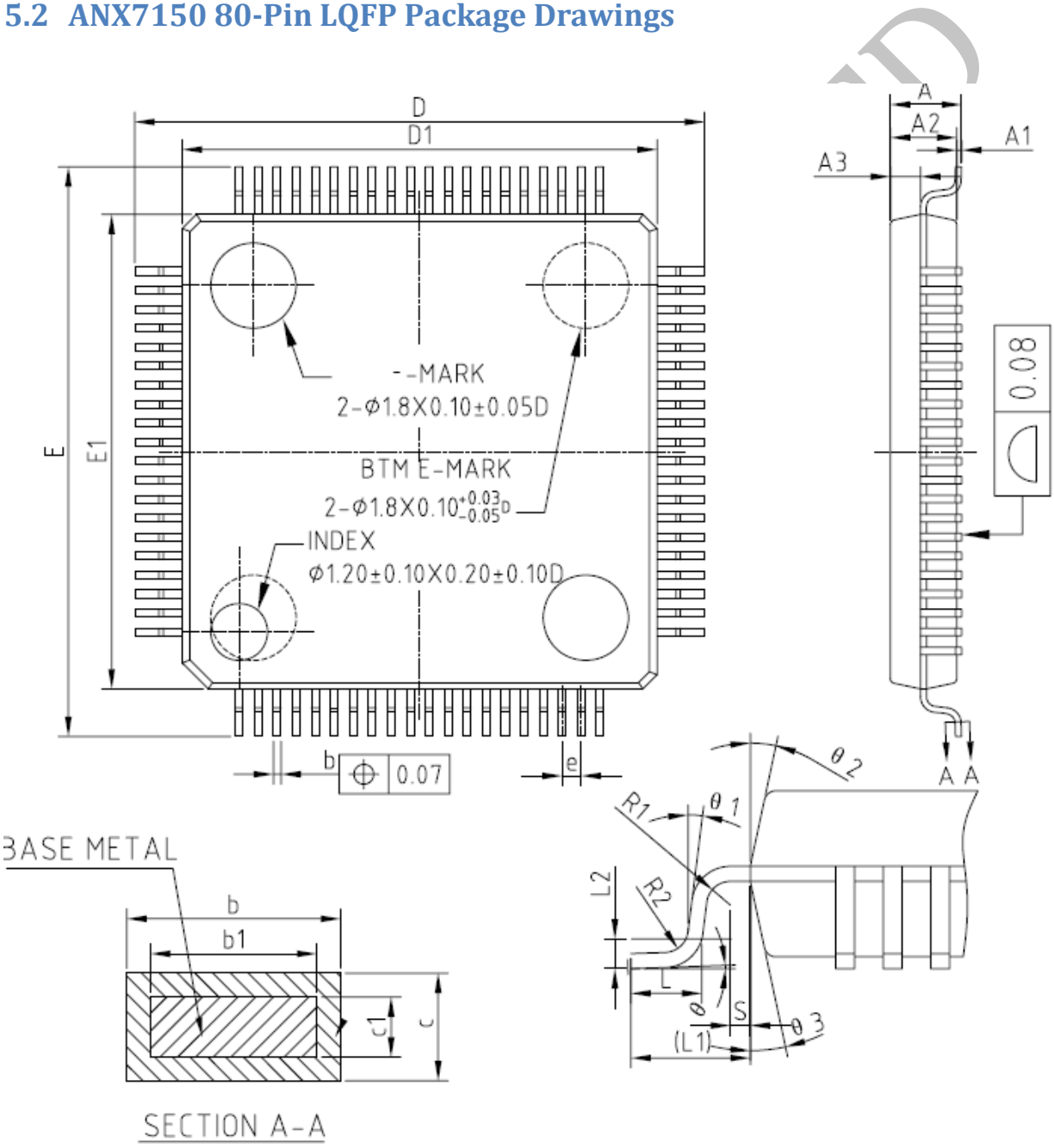


Figure 5-2 ANX7150 80-pin LQFP Package

ANX7150 80-PIN LQFP Package Dimensions

Ref	Min	Nom	Max
A	-	--	1.60
A1	0.05	--	0.20
A2	1.30	1.40	1.50
A3	0.59	0.64	0.69
b	0.13	--	0.23
B1	0.13	0.16	0.19
c	0.13	--	0.18
C1	0.12	0.13	0.14
D	11.80	12.00	12.20
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25BSC		
R1	0.08	--	--
R2	0.08	--	0.20

θ		3.5°	7°
Θ1	0°	--	--
Θ2	11°	12°	13°
Θ3	11°	12°	13°

5.3 ANX7150 81-Pin VFBGA Package Drawings

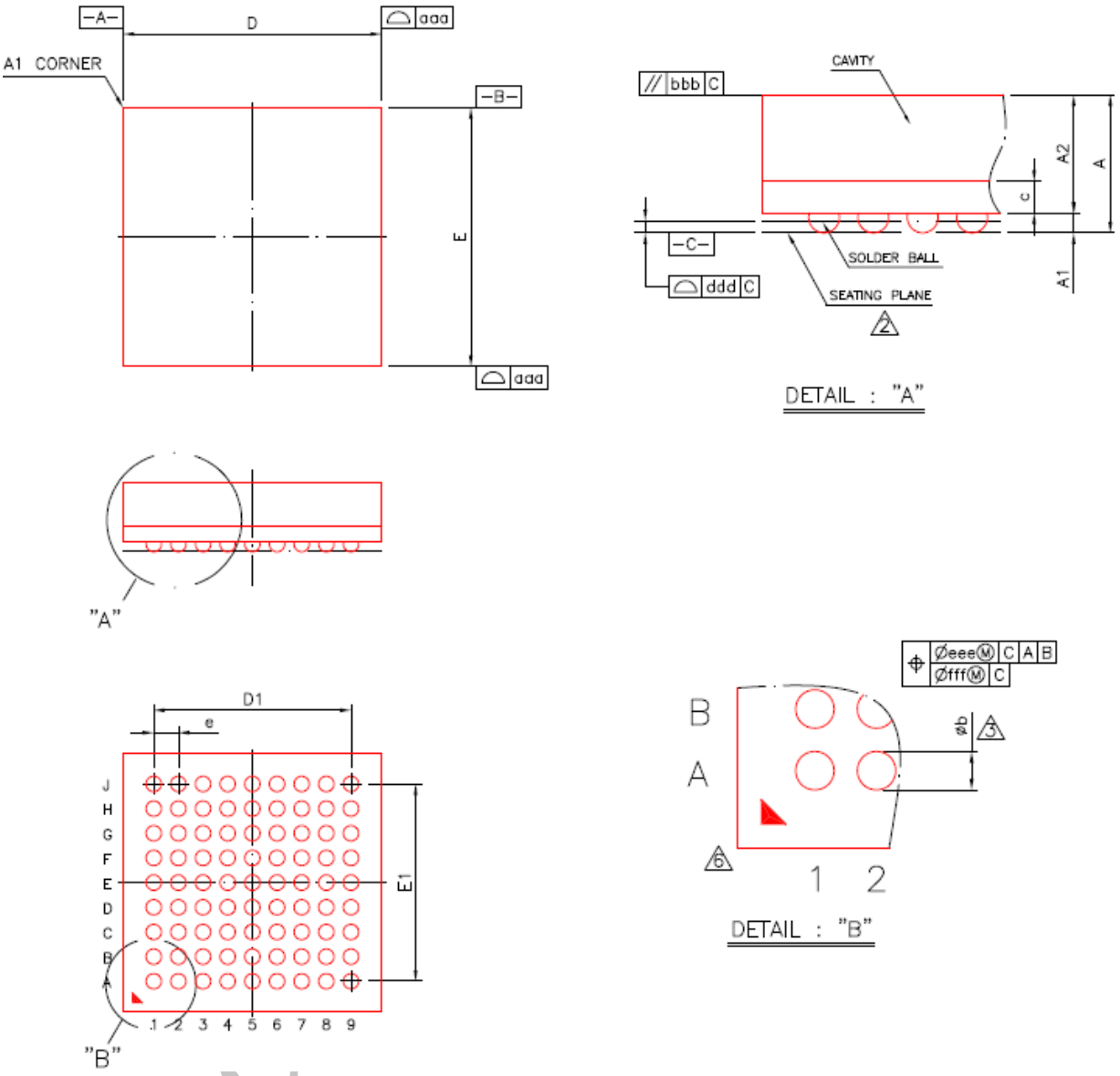


Figure 5-3 ANX7150 81-pin VFBGA Package

ANX7150 81-PIN VFBGA Package Dimensions

Ref	Min	Nom	Max
A	--	--	1.30
A1	0.11	0.16	0.21
A2	0.91	0.96	1.01
c	0.22	0.26	0.30
D	4.10	4.20	4.30
E	4.10	4.20	4.30
D1	--	3.20	--
E1	--	3.20	--
e	--	0.40	--

b	0.20	0.25	0.30
aaa	0.10		
bbb	0.10		
ddd	0.08		
eee	0.15		
fff	0.05		

Notes:

1. CONTROLLING DIENSION: MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERANCE DOCUMENT: JEDEC MO-195.
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
7. SPECIAL CHARACTERISTICS C CLASS: bbb,ddd.

5.4 ANX7150 81-Pin TFBGA Package Drawings

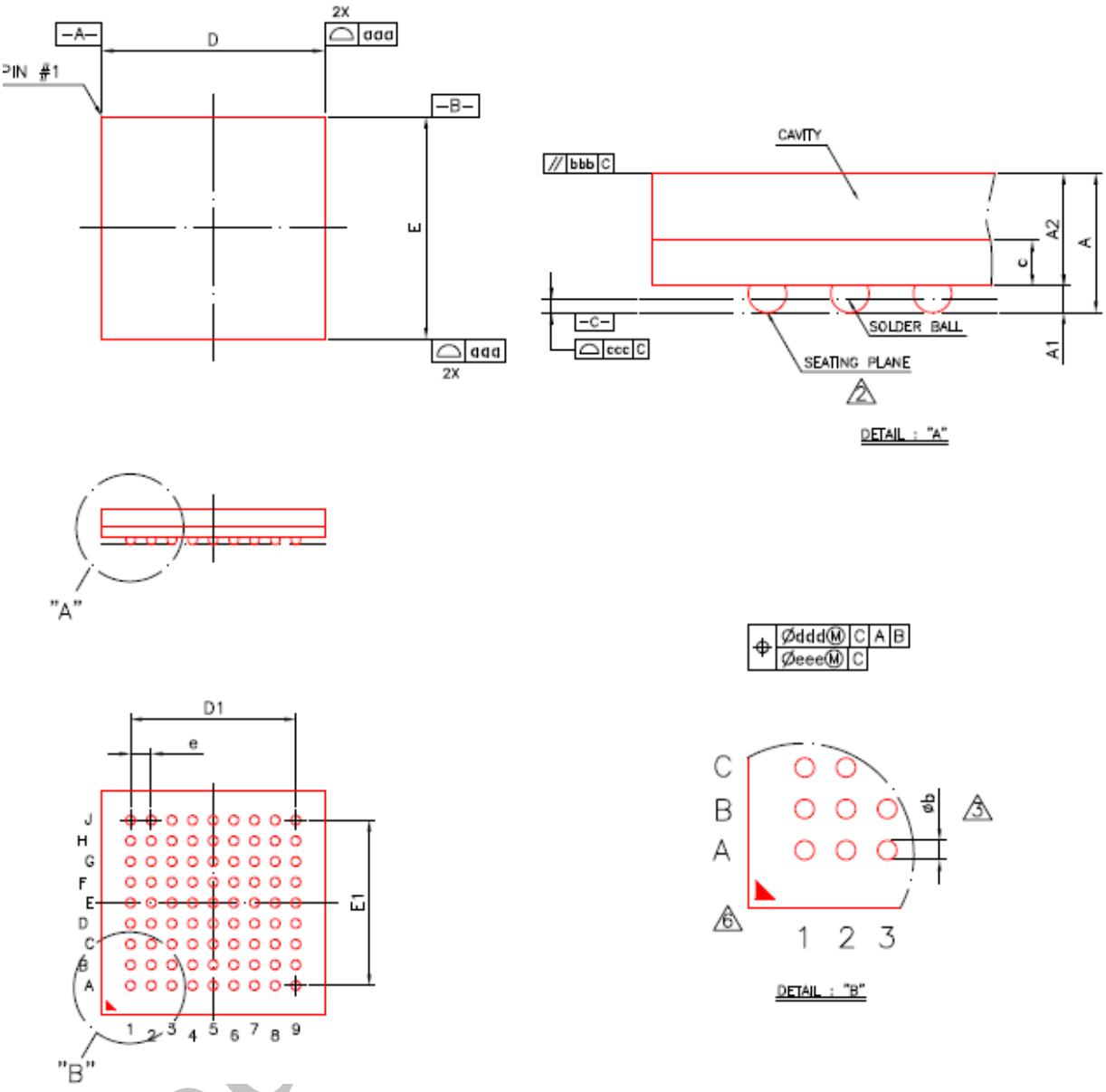


Figure 5-4 ANX7150 81-pin TFBGA Package

ANX7150 81-PIN TFBGA Package Dimensions

Ref	Min	Nom	Max
A	--	--	1.20
A1	0.16	0.21	0.26
A2	0.84	0.89	0.94
c	0.32	0.36	0.40
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D1	--	5.20	--
E1	--	5.20	--

e	--	0.65	--
b	0.25	0.30	0.35
aaa	0.15		
bbb	0.20		
ccc	0.10		
ddd	0.15		
eee	0.08		
MD/ME	9/9		

Notes:

1. CONTROLLING DIENSION: MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
6. SPECIAL CHARACTERISTICS C CLASS: bbb,ccc.

6 Ordering Information

The ANX7150 device is available with QFN, QFP and BGA package options and an HDCP option. Table 6-1 shows the part ordering information and the corresponding package markings. Contact Analogix for further information.

Table 6-1 ANX7150 Ordering Information

Part No.	Description	Availability
ANX7150F	No HDCP function 48 pin, 6 x 6 mm, QFN package	Now
ANX7150FH	HDCP function enabled 48 pin, 6 x 6 mm, QFN package	Now
ANX7150L	No HDCP function 80 pin, 10 x 10 mm, LQFP package	Now
ANX7150LH	HDCP function enabled 80 pin, 10 x 10 mm, LQFP package	Now
ANX7150B	No HDCP function 81 ball, 4.2 x 4.2 mm, BGA package	Now
ANX7150BH	HDCP function enabled 81 ball, 4.2 x 4.2 mm, BGA package	Now
ANX7150V	No HDCP function 81 ball, 7 x 7 mm, BGA package	TBD
ANX7150VH	HDCP function enabled 81 ball, 7 x 7 mm, BGA package	TBD

7 Marking Information

7.1 ANX7150 VFBGA Package Marking Information

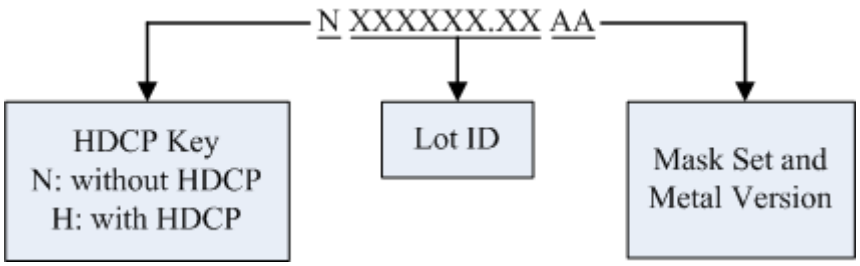
Line 1= Analogix Semiconductor logo

Line 2 = Marking name

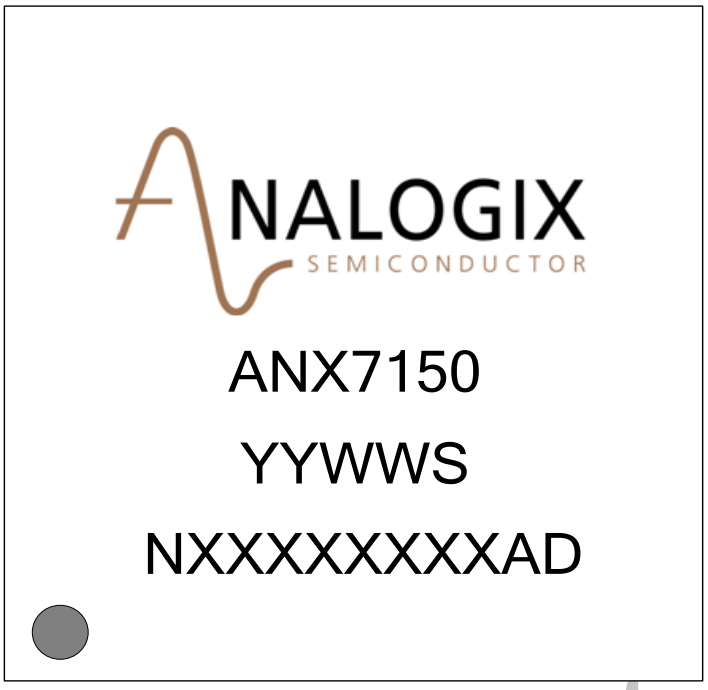
Line 3 = Date Code+F, Location (CN)

Line 4 = N+Lot number+Rev i.e.: NXXXXXX.XXAA

Line 4:



7.2 ANX7150 TFBGA Package Marking Information (No HDCP Function)



Line 1= Analogix Semiconductor logo

Line 2 = Marking name

Line 3 = Date Code+S

Line 4 = N+Lot number+Rev+AD

Notes:

1). Font: Arial

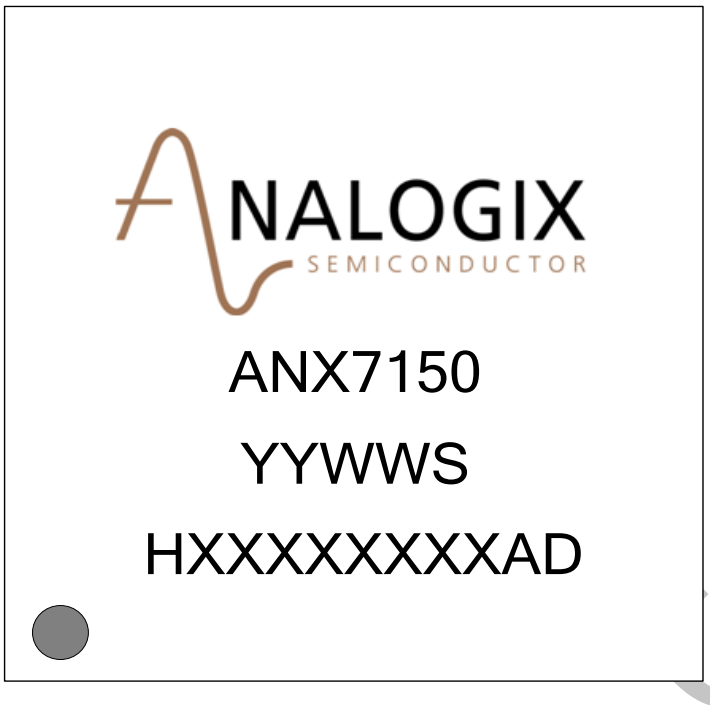
2). For line 4:

a. 1st letter: It is fixed: N

b. 2nd~9th letter: it is Lot ID, please follow our ABI

c. 10th~11th letter: it is fixed: AD

7.3 ANX7150 TFBGA Package Marking Information (HDCP Function Enabled)



Line 1= Analogix Semiconductor logo

Line 2 = Marking name

Line 3 = Date Code+S

Line 4 = H+Lot number+Rev+AD

Notes:

1). Font: Arial

2). For line 4:

a. 1st letter: It is fixed: H

b. 2nd~9th letter: it is Lot ID, please follow our ABI

c. 10th~11th letter: it is fixed: AD

Reference

Application Notes	Comments
Design SPEC of ANX7150	
DisplayPort™ Specification, Ver.1 Rev.1a	
VESA E-EDID STANDARD	
I²C SPECIFICATION	
IEC 60958	
IEC 61937	

3211 Scott Blvd., Suite 102
Santa Clara, CA 95054, USA

(1) 408-988-8848

http://www.analogix.com/