ANX9832

Low Power DisplayPort™ to VGA Converter

Datasheet Revision 1.8

June 2012

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1 General Description

ANX9832 is an ultra-low power DisplayPort to VGA translator that provides a cost-effective method of sending digital signals to end users.

The AUX CH is a half duplex, bi-directional differential pair that provides 1Mbps data rate for link configuration and management. It is also used to read display EDID (Extended Display Identification Data), and can also be used to carry data from the receiver (sink) device to the transmitter (source) device, such as compressed video data in a teleconferencing application.

Configuration registers support standard DPCD and internal registers. DPCD registers are used to configure the receiver capability, link configuration/status, and other miscellaneous functions.

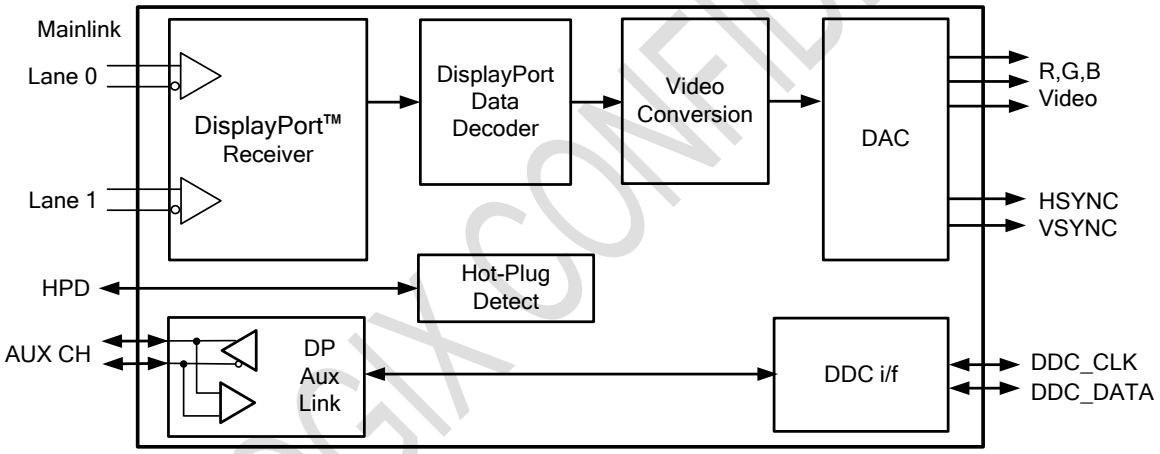

Figure 1-1 **ANX9832 Block Diagram**

2 Features

- **DisplayPort Input Interface**

  - VESA Compliant DisplayPort 1.1a Converter

  - Programmable 1 or 2 lanes Main Link and 1.62/2.7Gbps data rate support

  - Compliance with Proposed DisplayPort Interoperability Guideline, Version 1.1a

  - AUX Channel link up to 1Mbps bandwidth

  - Down Spread Spectrum Clock (SSC) support

  - Advanced WideEye™ SerDes

  - Capable of receiving data over long and/or low quality cables

  - Low power architecture

- **Output Interface**

  - Integrated 8-bits Video DAC

  - Support resolution up to 1920*1200@60Hz

  - VGA output pixel rate up to 180MHz for 24-bits

  - VGA output pixel rate up to 235MHz for 18-bits

  - Automatic monitor plug and unplug detect for VGA output

  - VGA output meet VESA VSIS v1r2 clock jitter target

  - EDID and MCCS pass-through support

- **Ultra-fast video image recovery**
- **27MHz crystal input**
- **1.2V and 3.3V power supplies**
- **5V output pin available for VGA interface**
- **8KV ESD performance**
- **Package: 48-pin QFN**
- **RoHS compliant and Halogen free package**

3 Typical Applications

The block diagram of ANX9832 is shown in Figure 3-1. The DP receiver block of ANX9832 chip is used to receive 2/1 lane(s) high speed DP signals that carry video data and other control information. ANX9832's VGA can output pixel clock frequency up to 180MHz, and 24 bit-per-pixel (or 8 bit-per-color). Note that the actual supported video format is limited by DisplayPort input bandwidth.

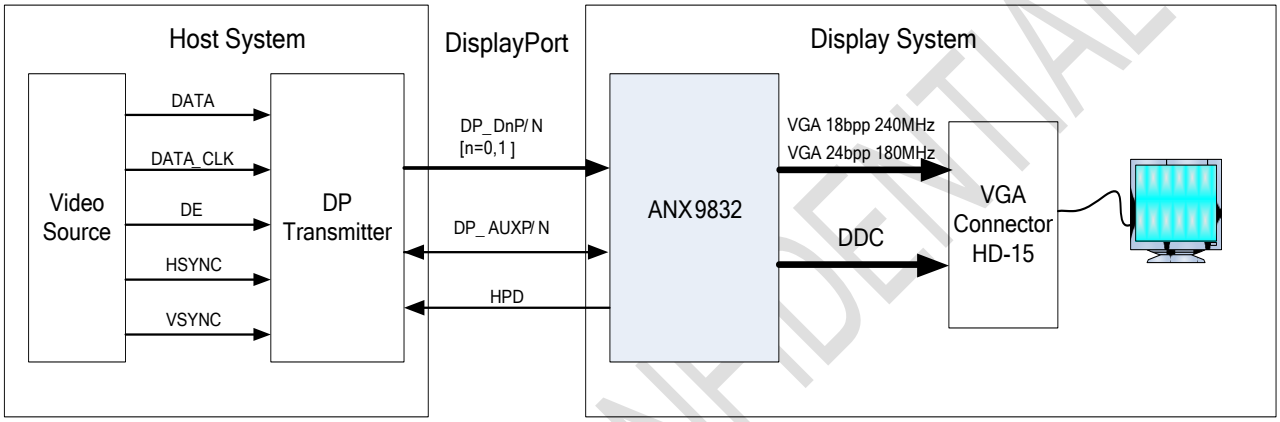

Figure 3-1 System Application of ANX9832

As one product of SlimPort® family, the ANX9832 acts as SlimPort® receiver to VGA transmitter. The ANX9832 requires just 3 signals to receive the video, status and side-band information. There is a single lane Main Link which takes two signals, and the C-WIRE, which replaces the AUX-channel pair and HPD signals from the standard DP connector. Figure 3-2, below, shows the ANX9832 in a SlimPort® application using a mini or micro USB 2.0 connector.

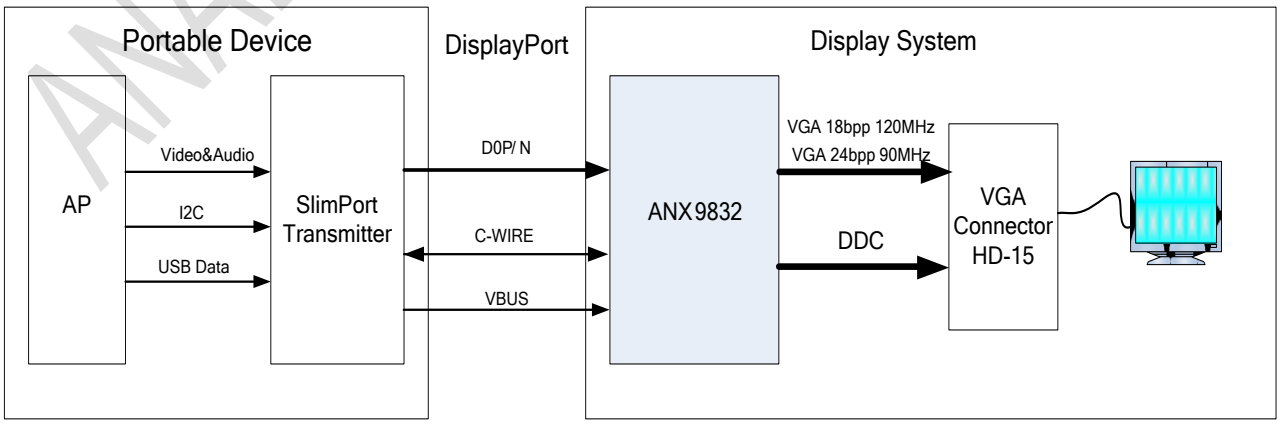

Figure 3-2 SlimPort® Application of ANX9832

4 Pin Descriptions

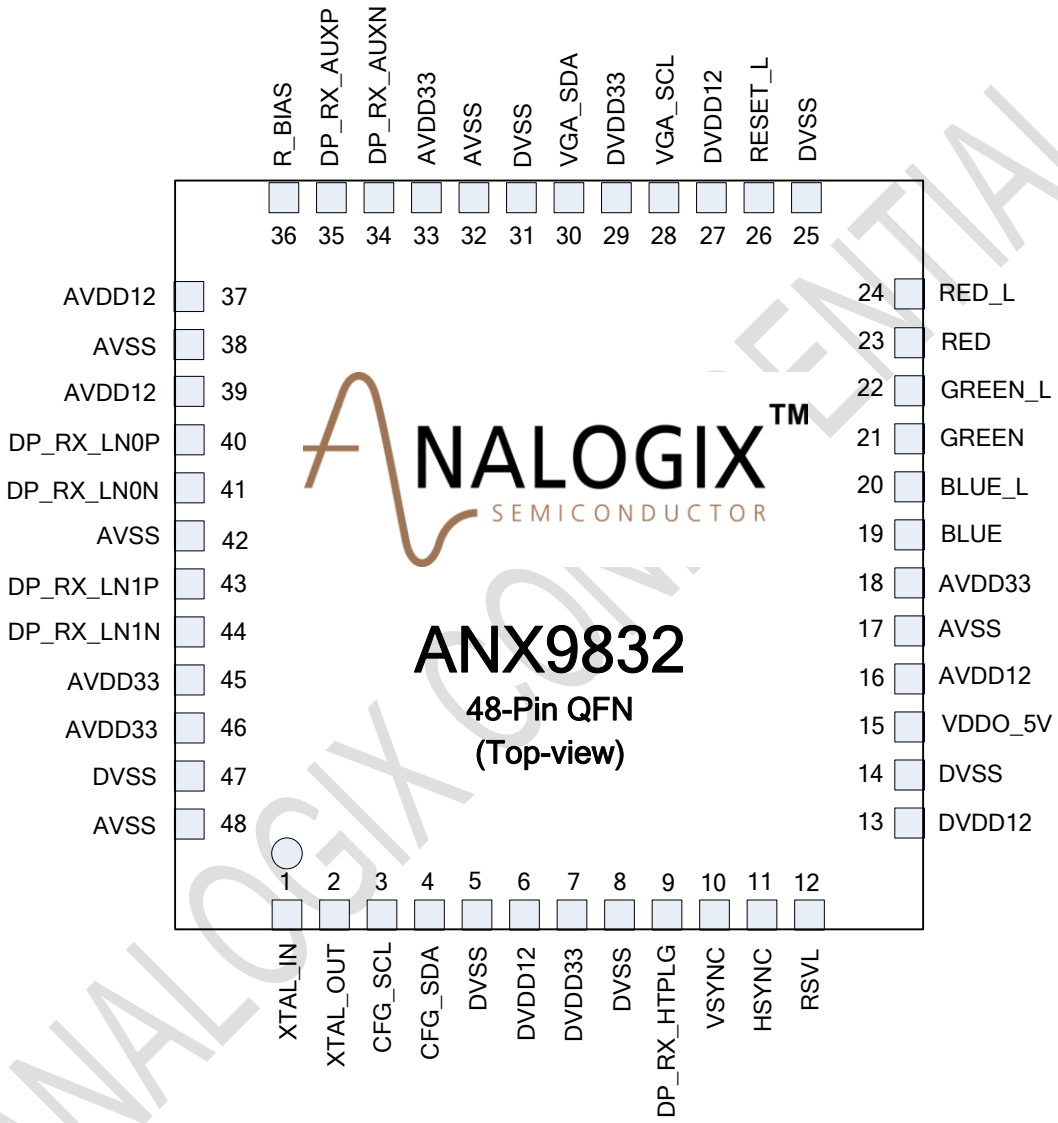

Figure 4-1 ANX9832 48-pin QFN

4.1 Pin Definition

Table 4-1 Pin Definition

Pin Number	Name	Type	Description
40,41,43,44	DP_RX_LN{0,1}{P,N}	Analog	DP port main link signals
35,34	DP_RX_AUX{P,N}	Analog	DP port AUX channel signals
9	DP_RX_HTPLG	LVTTL	DP port HPD signal
23,24	RED, RED_L	Analog	Red Video
21,22	GREEN, GREEN_L	Analog	Green Video
19,20	BLUE, BLUE_L	Analog	Blue Video
11	HSYNC	LVTTL	Horizontal sync
10	VSYNC	LVTTL	Vertical sync
30	VGA_SDA	LVTTL	DDC Channel I^2C data
28	VGA_SCL	LVTTL	DDC Channel I^2C clock
26	RESET_L	Schmitt	Asynchronous chip reset pin, active low, with internal pull-down, with Schmitt trigger
12	RSVL		Reserved and default low
4	CFG_SDA		Reserved to High
3	CFG_SCL		Reserved to High
1,2	XTAL_IN, XTAL_OUT	Analog	Crystal clock input and output
36	R_BIAS	Analog	Bias resistor, connected to analog ground via an adjustable resistor 12 KΩ (precision 1%).

Table 4-2 Power Supply Definition

Pin Number	Name	Type	Description
16,37,39	AVDD12	Power	1.2V analog core power supply
6,13,27	DVDD12	Power	1.2V digital core power supply
18,33,45,46	AVDD33	Power	3.3V analog I/O power supply
7,29	DVDD33	Power	3.3V digital I/O power supply
15	VDDO_5V	Power	5V power supply output
17,32,38,42,48	AVSS	Ground	Analog ground
5,8,14,25,31,47	DVSS	Ground	Digital ground

5 Functional Descriptions and Interfaces

5.1 DisplayPort Receiver

The DisplayPort receiver consists of the Main Link, the AUX CH and the Hot Plug Detect (HPD). The receiver Main Link is an un-directional, high bandwidth interface designed to transport one uncompressed stream of video data. The Main Link consists of 2 differential pairs, which can support a total data throughput of 5.4Gbps per second. The AUX CH is a half-duplex, bi-directional low speed interface operating at 1Mbps. It is used for link management and device control. It is also used as a bridge for DDC/I^2C transactions. The Hot Plug Detect signal is an output to the transmitter. When the HPD signal goes high, the transmitter receives confirmation that a sink device is connected.

5.2 Analog VGA Interface

The Analog VGA interface is compliant with the VESA® Video Signal Standard, Version 1, Revision 2. The Analog VGA interface is capable of up to 180MHz output for 24-bits or 235MHz output for 18-bits, supporting up to 1920x1200 resolutions at 60Hz refresh rate and 8-bits per color (reduced video timing). The Analog VGA interface supports hot plug detection, via circuitry internal to the ANX9832 as well as a DDC channel to retrieve the monitor EDID information. The Table 5-1 shows maximum supported video format in 24 and 18 bit per pixel.

Table 5-1 Maximum Supported Video Format in 24 Bit per Pixel

24 bit per pixel		18 bit per pixel	
Video Format	**Pixel Clock Frequency**	**Video Format**	**Pixel Clock Frequency**
1600x1200@65Hz	175.5MHz	1600x1200@85Hz	229.5MHz
1920X1200@60Hz(RB)	154MHz	1920X1200@60Hz(RB)	193.25MHz

The maximum frequency is determined by following formula:

F_{max} = Lane_Count * Link_Bandwidth * 0.8 / bpp

Where Lane_Count is 1 or 2, Link_Bandwidth is 1.62G or 2.7G, bpp is bit per pixel (18, 24, 30, etc.)

5.2.1 Analog VGA DAC Interface Block

The Analog VGA DAC Interface Block provides a conversion from a digital representation of the display data to an analog representation using three 8-bit high-speed Digital-to-Analog Converters (DAC), where one DAC is assigned to each of the three color spaces: red, green, or blue. Color depth support is limited to 24-bits per pixel (or 8-bits per color) due to the DAC width of 8 bits. ANX9832 supports other color depth (up to 36-bits per pixel or 12-bits per color) input, and will translate it to 8-bits per color.

The DDC together with AUX CH, provide the means for DisplayPort source to read EDID from the VGA monitor.

5.3 Hot Plug Support

The Analog VGA DAC interface supports sensing of the attachment and detachment (hot plug detection) of a VGA sink device. The hot plug detection functions supports the following features: 1) Attaching a sink device to

any one of the three Analog VGA DAC signals will create a hot plug event, 2) Detaching a sink device from all three of the Analog VGA DAC signals will create a hot plug event, 3) All hot plug events will generate an IRQ on DisplayPort DP_RX_HTPLG pin.

6 Electrical Specifications

6.1 Absolute Maximum Conditions

Permanent damage may occur if absolute maximum conditions are violated. Refer to Section 6.2 for functional operating limits.

Table 6-1 Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
DVDD33	Digital I/O supply voltage	-0.3		3.8	V
AVDD33	Analog I/O supply voltage	-0.3		3.8	V
DVDD12	Digital core logic supply voltage	-0.3		1.4	V
AVDD12	Analog core supply voltage	-0.3		1.4	V
ΔVDD33	Difference between AVDD33 and DVDD33[1]			0.6	V
ΔVDD12	Difference between AVDD12 and DVDD12[1]			0.2	V
V_{IN}	Input voltage	-1.0	--	DVDD33+0.3	V
T_J	Junction temperature			125	°C
T_{STG}	Storage temperature	-65	--	150	°C
ESD_H	ESD protection (Human body model)			8	KV

1. Power supply sequencing must guarantee these conditions.

6.2 Normal Operating Conditions

Table 6-2 Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
DVDD33	Digital I/O supply voltage[1]	3.0	3.3	3.6	V
AVDD33	Analog I/O supply voltage[1]	3.0	3.3	3.6	V
DVDD12	Digital core logic supply voltage	1.1	1.2	1.32	V
V_{RIP}	Power supply noise[2]	--	--	--	mVp-p
T_A	Ambient temperature	-10	25	75	°C

1. DVDD33 and AVDD33 should be controlled from the same power supply source.
2. Measured at the input pin after power supply filtering.

6.3 DC Specifications

These specifications apply under normal operating conditions with output pin load CL= 10pF unless otherwise stated. Minimum output drives are specified at 70 °C ambient temperature, 3.0V supply voltage. Maximum output drives are specified at 0 °C, 3.6V supply voltage.

6.3.1 Input and Output Parameters

Table 6-3 Input and Output parameters

Symbol	Parameter	Min	Typ	Max	Units
V_{IH}	High level input voltage	2.0			V
V_{IL}	Low level input voltage			0.8	V
V_{T+}	Low to high threshold voltage	1.9			V
V_{T-}	High to low threshold voltage			0.7	V
V_{OH}	High level output voltage	2.4			V
V_{OL}	Low level output voltage			0.4	V
I_{IL}	Input leakage current	-10		10	uA
I_{DDPD}	Output leakage current	-10		10	uA
R_{PD}	Internal pull-down resistor		83		KΩ
I_{OPD}	Output pull-down current		60	75	uA
I_{IPD}	Input pull-down current		60	75	uA

6.3.2 Power Consumptions

Table 6-4 Power consumptions in normal work model

Item	Bandwidth /Lane count	Typical Value			Maximum Value		
		VDD33 (mA)	VDD12 (mA)	Power Consumption (mW)	VDD33 (mA)	VDD12 (mA)	Power Consumption (mW)
800X600@60Hz PCLK = 40MHz	1.62G/1lane	76	63	326.4	77	67	334.5
1280x720@60Hz PCLK = 74.25MHz	2.7G/1lane	78	80	353.4	79	84	361.5
1280x1024@60Hz PCLK = 108MHz	1.62G/2lanes	81	111	400.5	82	114	407.4
1920x1080@60Hz PCLK = 148.5MHz	2.7G/2lanes	83	131	431.1	84	135	439.2
1920X1200@60Hz PCLK = 154MHz	2.7G/2lanes	84	132	435.6	85	136	443.7
1600x1200@65Hz PCLK = 175.5MHz	2.7G/2lanes	84	133	436.8	84	137	441.6

Table 6-5 Power consumptions in standby model

Item	Condition	Typical Value		
		VDD33 (mA)	VDD12 (mA)	Power Consumption (mW)
Standby mode	power up +5V output[1]	13	1	44.1
	power down +5V output[1]	4	1	14.4

1. +5V output is generated by ANX9832 chip. It is used for DDC pull up, and can be power down by register in standby mode.

6.3.3 Analog VGA DAC Electrical Specifications

The VESA® Video Signaling Standard, Version 1, Revision 2 provides the minimum requirements for an Analog VGA DAC. Table 6-6 lists the electrical parameters for the ANX9832 chip.

Table 6-6 Analog VGA Output Specifications

Symbol	Parameter	Min	Typ	Max	Units
	Resolution		8		Bits
INL	Integral non-linearity [1]	-1	+/-0.5	+1	Bits
DNL	Differential non-linearity	-1	+/-0.3	+1	Bits
V_{MATCH}	DAC-to-DAC matching	--	4.0	6.0	%
V_{O_MAX}	Maximum output voltage (@FFh)	0.665	0.700	0.77	V
V_{O_MIN}	Minimum output voltage (@00h)	0.000	--	0.000	
V_{OC}	Output compliance voltage range	0	--	1.4	V
V_{OS}	Output overshoot voltage	--	6	12	%
V_{US}	Output undershoot voltage [2]	--	6	12	%
T_{STL}	Overshoot/undershoot settling time [3]	--	500	833	pS
T_{SKEW}	Channel-to-channel output skew [3]	--	800	1350	pS
Z_{OUT}	DAC output impedance [4]	10	--	--	kOhms
C_{OUT}	DAC output capacitance [5]	--	--	20	pF
T_{RF}	Output rise/fall time [6]	--	1000	--	pS

1. Monotonicity must be guaranteed.
2. Percent of maximum output voltage (V_{O_MAX}).
3. Settling to within +/- 5% of final output voltage (V_{O_MAX}).
4. Minimum output impedance for the current mode DAC.
5. Measured with the DAC output at 0V.
6. Rise/fall time measured between 10 and 90% of steady state Vmin to Vmax, as defined in Section 2.4 of the "VESA Video Signal Standard, Version1, Revision 2". Note this is affected by the pi filter setting and layout of RGB signal. Large capacitor and long RGB trace will increase the rise/fall time.

6.4 AC Specifications

6.4.1 DisplayPort Receiver

Table 6-7 DisplayPort Receiver Main Link

Symbol	Parameter	Min	Nom.	Max	Units
UI_High_Rate	Unit Interval for high bit rate(2.7 Gbps/lane)		370		ps
UI_Low_Rate	Unit Interval for high bit rate(1.62 Gbps/lane)		617		ps
Down_Spread_Amplitude	Link clock down spreading	0.0		0.5	%
$V_{RX-DIFFp-p}$	Differential Peak-to-peak Input Voltage at RX package pins()2.7G	120			mV
$V_{RX-DIFFp-p}$	Differential Peak-to-peak Input Voltage at RX package pins(1.62G)	40			mV
T_{RX-EYE_CONN}	Minimum Receiver Eye Width at Rx-side connector pins	0.51			UI
T_{RX-EYE_CHIP}	Minimum Receiver Eye Width at Rx package pins	0.47			UI
$T_{RX-EYE-MEDIAN-tp-MAX-ITTER\_CHIP}$	Maximum time between the jitter median and maximum deviation from the median at Rx package pins			0.265	UI

Table 6-8 DisplayPort Auxiliary Channel

Symbol	Parameter	Min	Typ	Max	Units
U_{IN}	AUX Unit Interval	0.4	0.5	0.6	µs
Pre-charge	Number of pre-charge pulses	10	--	16	
$T_{AUX-BUS-PARK}$	Aux CH bus park time	10	--	--	ns
$T_{cycle-to-cycle\ jitter}$	Maximum allowable UI variation within a single transaction at connector pins of a receiving device	--	--	0.05	UI
$V_{AUX-DIFFp-p}$	AUX peak-to-peak voltage at a receiving device	0.32	--	1.36	V
$V_{AUX\_TERM\_R}$	AUX CH termination DC resistance	--	100	--	Ω
$V_{AUX-DC-CM}$	AUX DC common mode voltage	0	--	2.0	V
$V_{LAUX-TURN-CM}$	AUX turn around common mode voltage	--	--	0.4	V
I_{AUX_SHORT}	AUX short circuit current	--	--	90	mA
C_{AUX}	Aux AC coupling capacitor	75	--	200	nF

Table 6-9 DisplayPort Hot Plug Detect Signal

Parameter	Min	Nom.	Max	Units
HPD Voltage	2.25		3.6	V
HPD sink termination	100			kΩ
IRQ HPD Pulse Width Driven by Sink	0.5		1.0	ms

7 Package Specifications

ANX9832 is packaged in 48-pin QFN, The package dimensions are shown below.

7.1 Mechanical Drawings (CE048-SW4)

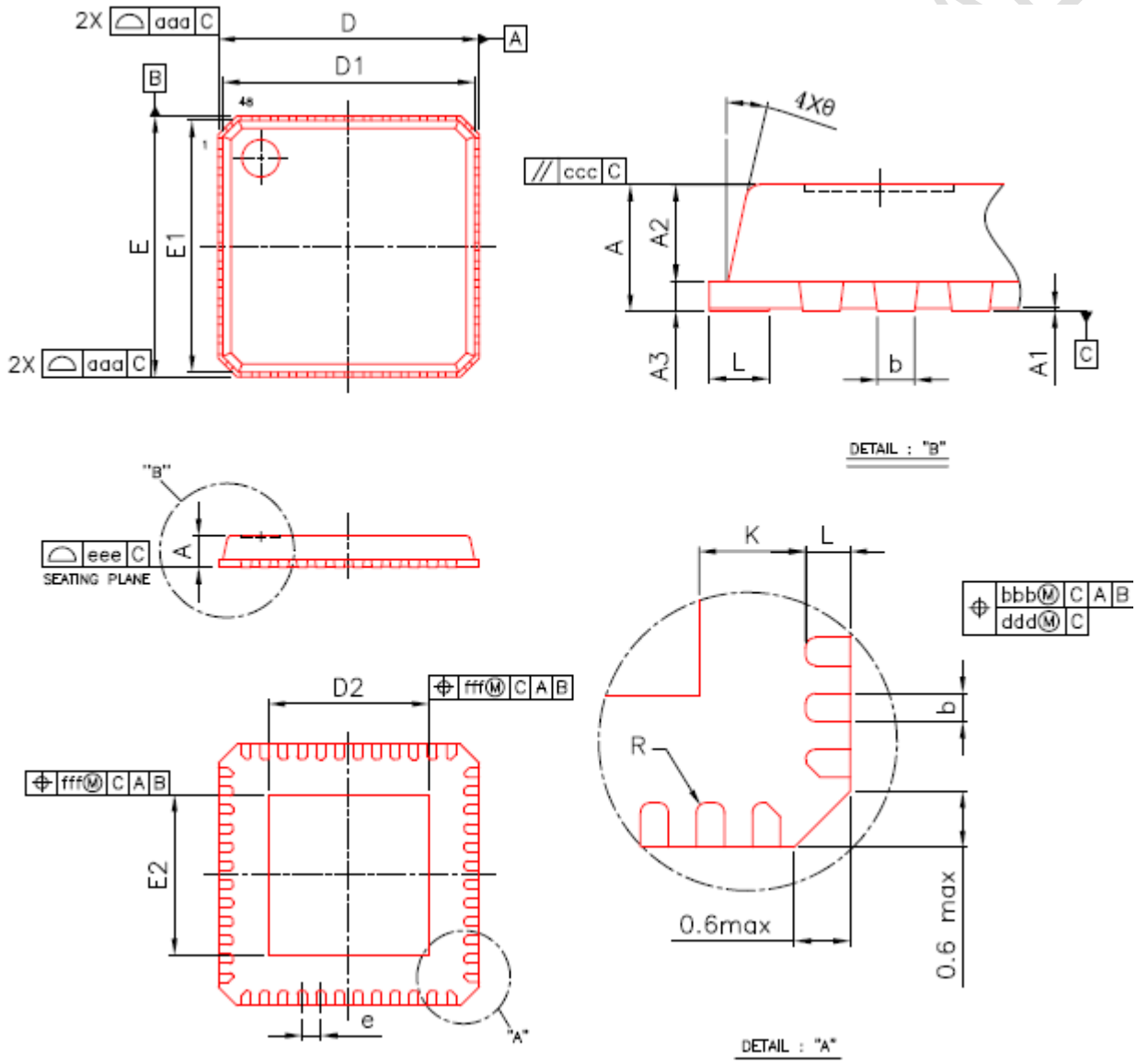

Figure 7-1 ANX9832 Mechanical Diagram (CE048-SW4)

ANX9832 QFN Package Dimensions (CE048-SW4)

Ref	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	0.60	0.65	0.70
A3	0.20 Ref		
b	0.18	0.25	0.30
D/E	6.90	7.00	7.10
D1/E1	6.75 BSC		
D2/E2	4.15	4.30	4.45
e	0.50 BSC		
L	0.30	0.40	0.50
θ	0°	---	14°
R	0.09	---	---
K	0.20	---	---
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Notes:

1. All dimensions are in millimeters.
2. Reference document: JEDEC MO-220

8 Ordering Information

Table 8-1 ANX9832 Ordering Information

Part No.	Description	Availability
ANX9832FN-BB-T	Low Power DisplayPort™ Converter with VGA Output 48 pin, 7 x 7 mm, QFN package	March, 2012
ANX9832EV	ANX9832 Evaluation Kit	June, 2009

9 Marking Information

Top View

Line 1= Analogix Semiconductor logo.

Line 2 = Product name

Line 3 = Date Code+X XX

Line 4 = N + Lot number + Chip revision ID

Note:

For initial letter of line 4, its meaning is:

N (None): without HDCP key in assembly

H (HDCP): with HDCP key in assembly

Appendix A

Revision History

Rev. #	Date	Comments
Rev 1.0	Sep. 2010	Initial release
Rev 1.1	Aug. 2011	Modify feature list
Rev 1.2	Sep. 2011	Modified the format
Rev 1.3	Jan. 2012	Added the description for the Table 6-5
Rev 1.4	Feb. 2012	Added the Standby power consumption
Rev 1.5	Feb. 2012	Modified the format
Rev 1.6	Mar. 2012	Modified the Ordering information
Rev 1.7	Mar. 2012	Modified the Feature List
Rev1.8	May. 2012	Add system block of SlimPort® application

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