## DESCRIPTION

The AO2007 offers low offset and long-term stability by means of a low noise and high voltage operational amplifier circuit. For most applications, external components are not required for offset nulling and frequency compensation.

The AO2007 has a gain-bandwidth product of 2MHz, a slew rate of 1.2V/us and a quiescent current of 1mA at wide power supply range.

The AO2007 is designed to provide optimal performance in low noise systems. It provides rail-to-rail output swing into heavy loads.

The AO2007 is available in SOP8 package.

## ORDERING INFORMATION

| Package Type | Part Number | |
|---|---|---|
| SOP8<br>SPQ: 4,000pcs/Reel | M8 | AO2007M8R |
| | | AO2007M8VR |
| Note | V: Halogen free Package<br>R: Tape & Reel | |
| AiT provides all RoHS products | | |

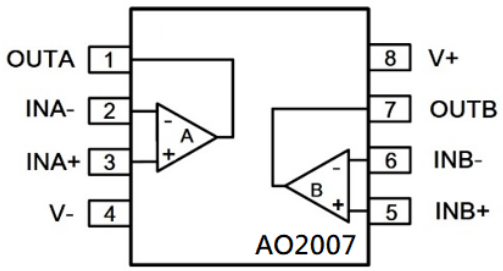
## FEATURES

- No External Components Required
- Supply Voltage Range: 3.3V to 32V
- Low Offset Voltage: ±0.2mV (TYP)
- Low Bias Current: ±10pA (TYP)
- Gain Bandwidth Product: 2MHz
- Low Quiescent Current: 1mA (TYP)
- Overload Recovery Time: 1.6us
- Temperature: -40°C to +125°C

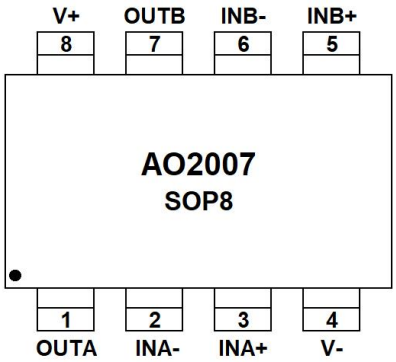
## APPLICATION

- Wireless Base Station Control Circuits
- Optical Network Control Circuits
- Instrumentation
- Sensors and Controls
- Precision Filters
- Cellular and Cordless Phones
- Photodiode Amplification
- A/D Converters
- Laptops and PDAs
- Medical and Industrial Instrumentation

## TYPICAL APPLICATION



## PIN DESCRIPTION




SOP8, M8

Top View

| Pin # | Symbol | I/O (1) | Functions |
|---|---|---|---|
| SOP8 | | | |
| 1 | OUTA | O | Output, Channel A |
| 2 | INA- | I | Inverting Input, Channel A |
| 3 | INA+ | I | Noninverting Input, Channel A |
| 4 | V- | - | Negative (Lowest) Power Supply |
| 5 | INB+ | I | Noninverting Input, Channel B |
| 6 | INB- | I | Inverting Input, Channel B |
| 7 | OUTB | O | Output, channel B |
| 8 | V+ | - | Positive (Highest) Power Supply |

(1) I = Input, O = Output.

## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)

| | | |
|---|---|---|
| Vs=(V+) - (V-), Supply Voltage | | 36V |
| Signal Input Pin Voltage (1) | | (V-)-0.3V~(V+) +0.3V |
| Signal Output Pin Voltage (2) | | (V-)-0.3V~(V+) +0.3V |
| Signal Input Pin Current (1) | | ±10mA |
| Signal Output Pin Current (2) | | ±10mA |
| $\theta_{JA}$, Package Thermal Impedance (3) | SOP8 | 110℃/W |
| $T_A$, Operating Range | | -40°C ~ +125°C |
| $T_J$, Junction Temperature (4) | | -40°C ~ +150°C |
| $T_{STG}$, Storage Temperature | | -65°C ~ +150°C |
| **ESD Susceptibility** | | |
| $V_{(ESD)}$, Electrostatic Discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(5) | ±2000V |
| | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(6) | ±1000V |
| | Machine Model (MM) | ±200V |

Stresses above may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(1) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current-limited to 10mA or less.

(2) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.3V beyond the supply rails should be current-limited to ±10mA or less.

(3) The package thermal impedance is calculated in accordance with JESD-51.

(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and TA. The maximum allowable power dissipation at any ambient temperature is PD = ($J_{J(MAX)}$ - $T_A$) / $R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

(5) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

(6) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

## Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| | | Min. | Non. | Max. | Unit |
|---|---|---|---|---|---|
| Supply voltage , Vs= (V+) - (V-) | Single-supply | 3.3 | - | 32 | V |
| | Dual-supply | ±1.65 | - | ±16 | |

## ELECTRICAL CHARACTERISTICS

$T_A$=+25°C, $V_S$=3.3V to 32V, $R_L$=10kΩ connected to $V_S$/2, and $V_{OUT}$=$V_S$/2, $V_{CM}$=$V_S$/2,unless otherwise noted (1)

| Parameter | Symbol | Conditions | | Min. (2) | Typ. (3) | Max. (2) | Units |
|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | |
| Operating Voltage Range | $V_S$ | | | 3.3 | - | 32 | V |
| Quiescent Current Per Amplifier | $I_Q$ | $V_S$=±2.5V, $I_O$=0mA | | - | 1.0 | 1.5 | mA |
| | | $V_S$=±16V, $I_O$=0mA | | - | 1.4 | 1.8 | |
| Power-Supply Rejection Ratio | PSRR | $V_S$=5V to 32V | | 82 | 100 | - | dB |
| **INPUT** | | | | | | | |
| Input Offset Voltage | $V_{OS}$ | $V_S$=5V, $V_{CM}$=$V_S$/2 | +25℃ | -0.4 | ±0.2 | 0.4 | mV |
| | | | -40°C ~+125°C | - | ±1.0 | - | |
| | | $V_S$=32V, $V_{CM}$=$V_S$/2 | +25℃ | -0.9 | ±0.4 | 0.9 | |
| | | | -40°C ~+125°C | - | ±1.0 | - | |
| Input Offset Voltage Average Drift | $V_{OS}$ $T_C$ | $V_{CM}$= $V_S$/2<br>-40°C ~+125°C | | - | ±5.0 | - | μV/℃ |
| Input Bias Current (4)(5) | $I_B$ | $V_{CM}$= 0V | | - | ±10 | - | pA |
| Input Offset Current (4) | $I_{OS}$ | $V_{CM}$= 0V | | - | ±10 | - | pA |
| Common-Mode Voltage Range | $V_{CM}$ | | | (V-) | - | (V+)-2 | V |
| Common-Mode Rejection Ratio | CMRR | $V_S$= ±16V<br>$V_{CM}$=(V-) to (V+)-2V | | 87 | 115 | - | dB |
| **OUTPUT** | | | | | | | |
| Open-Loop Voltage Gain | $A_{OL}$ | $R_L$=10KΩ,<br>$V_O$=(V-)+0.5V to (V+)-0.5V | | 117 | 150 | - | dB |
| Output Swing from Rail | $V_{OH}$ | $V_S$=±16V, $R_L$=10KΩ | | 15.7 | - | - | V |
| | $V_{OL}$ | | | - | - | -15.7 | |
| Output Source Current (6) (7) | $I_{SOURCE}$ | $V_S$=10V | | 65 | 142 | - | mA |
| Output Sink Current (6) (7) | $I_{SINK}$ | | | 45 | 103 | - | |
| Capacitive Load Drive | $C_{LOAD}$ | | | - | 1 | - | nF |

| Parameter | Symbol | Conditions | Min. (2) | Typ. (3) | Max. (2) | Units |
|---|---|---|---|---|---|---|
| **FREQUENCY RESPONSE** | | | | | | |
| Slew Rate (8) | $S_R$ | G=+1, $C_L$=100pF | - | 1.2 | - | V/μs |
| Gain-Bandwidth Product | GBW | G=10, $R_L$=10KΩ<br>VPPvin=50mV, | - | 2.0 | - | MHz |
| Settling Time,0.1% | $t_S$ | $V_S$=±16V, G=+1,<br>$C_L$=100pF, Step=7V | - | 8.0 | - | μs |
| Overload Recovery Time | $t_{OR}$ | $V_{IN}$ x Gain ≥ $V_S$, G=-100 | - | 1.6 | - | μs |
| Turn on Time | $t_{ON}$ | G=1 | - | 75 | - | μs |
| **NOISE** | | | | | | |
| Input Voltage Noise | $E_N$ | f = 0.1Hz to 10Hz, $V_S$=±2.5V | - | 4.3 | - | μVpp |
| Input Voltage Noise Density (4) | $e_n$ | f =1KHz | - | 14 | - | nV/$\sqrt{Hz}$ |

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(4) This parameter is ensured by design and/or characterization and is not tested in production.

(5) Positive current corresponds to current flowing into the device.

(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and TA. The maximum allowable power dissipation at any ambient temperature is PD = ($T_{J(MAX)}$ - $T_A$) / $R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

(7) Short circuit test is a momentary test.

(8) Number specified is the slower of positive and negative slew rates.

## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = +25°C, $V_S$= ±16V, unless otherwise noted.

Fig 1. Supply Voltage vs. Quiescent Current

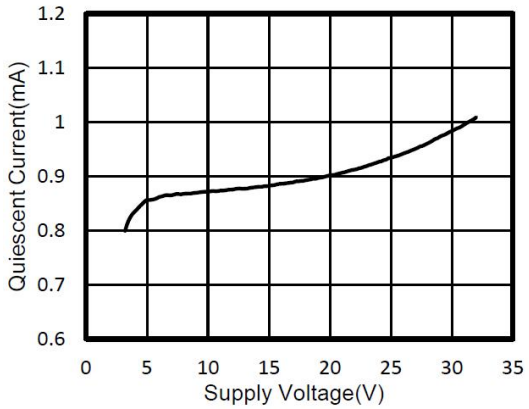



Fig 2. Supply Voltage vs. Output Current

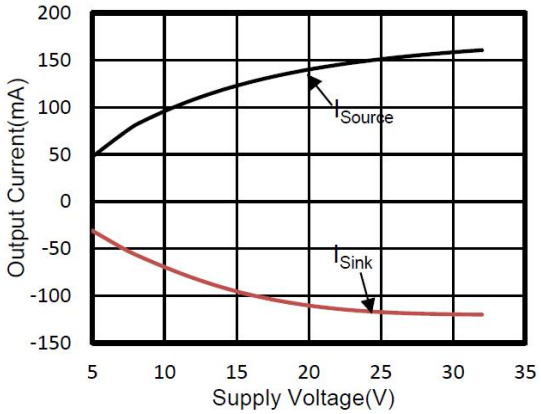



Fig 3. Large-Signal Step Response

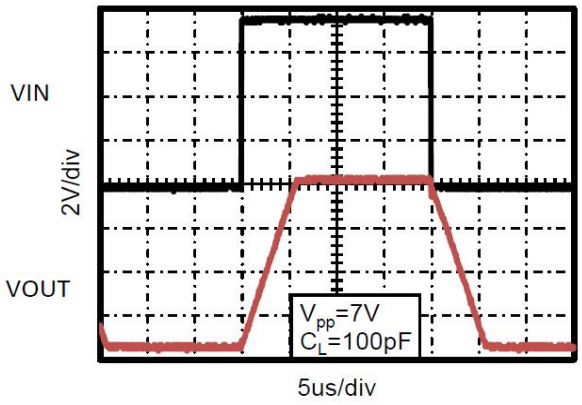



Fig 4. Input Bias Current
vs. Input Common Mode Voltage

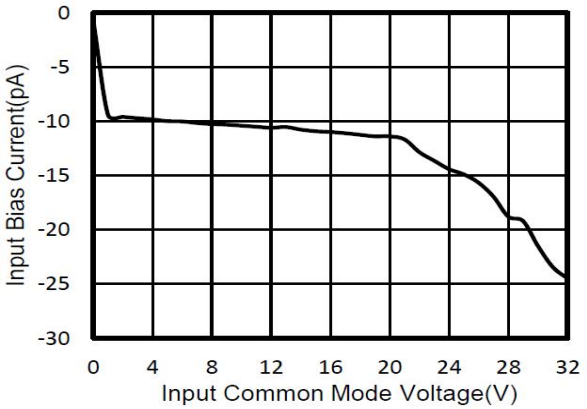



Fig 5. Output Voltage vs. Output Current

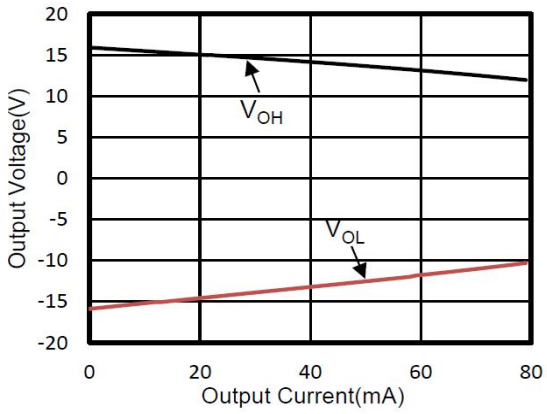



Fig 6. Output Current vs. Temperature

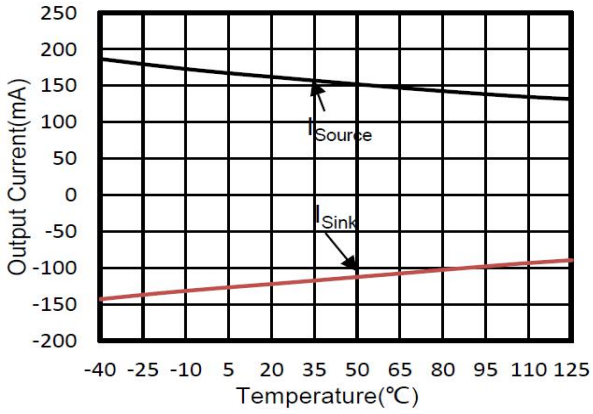
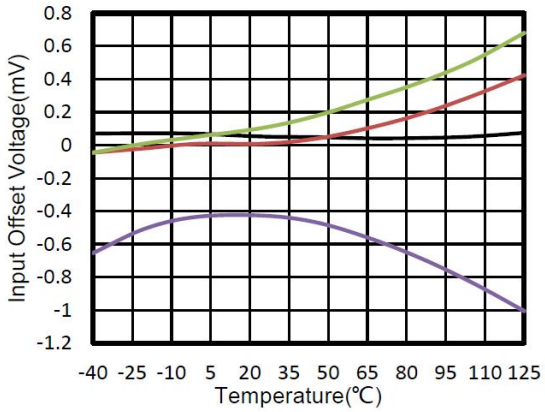
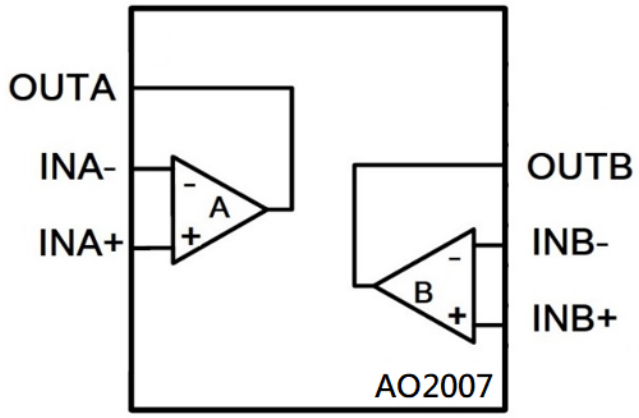


Fig 7. Input Offset Voltage vs. Temperature




## BLOCK DIAGRAM



## DETAILED INFORMATION

The AO2007 operates from either a single 3.3V to 32V supply or dual ±1.65V to ±16V supplies. For single-supply operation, bypass the power supply V+ with a 0.1μF ceramic capacitor which should be placed close to the V+ pin. For dual-supply operation, both the V+ and the V- supplies should be bypassed to ground with separate 0.1μF ceramic capacitors. 10μF tantalum capacitor can be added for better performance. Good PC board layout techniques optimize performance by decreasing the amount of stray capacitance at the operational amplifier's inputs and output. To decrease stray capacitance, minimize trace lengths and widths by placing external components as close to the device as possible. Use surface-mount components whenever possible. For the operational amplifier, soldering the part to the board directly is strongly recommended. Try to keep the high frequency current loop area small to minimize the EMI (electromagnetic interference).

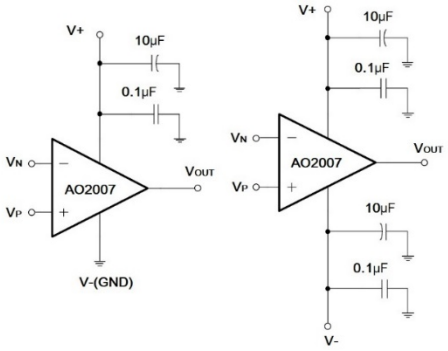



Fig 8. Amplifier with Bypass Capacitors

## Grounding

A ground plane layer is important for AO2007 circuit design. The length of the current path in an inductive ground return will create an unwanted voltage noise. Broad ground plane areas will reduce the parasitic inductance.

### Input-to-Output Coupling

To minimize capacitive coupling, the input and output signal traces should not be in parallel. This helps reduce unwanted positive feedback.

### Differential Amplifier

The circuit shown in Fig 9 performs the difference function.

If the resistor ratios are equal ($R_4/R_3 = R_2/R_1$),

then $V_{OUT} = (V_P - V_N) \times R_2/R_1 + V_{REF}$.

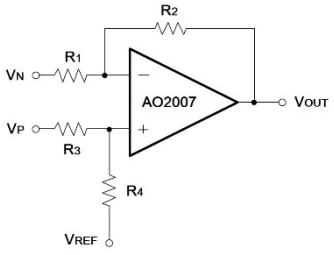



Fig 9. Differential Amplifier

### Instrumentation Amplifier

The circuit in Fig 10 performs the same function as that in Fig 9 but with a high input impedance.

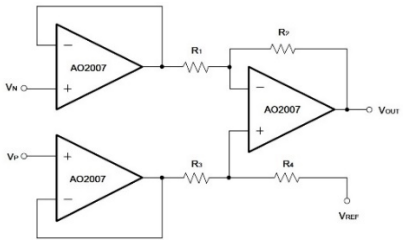



Fig 10. Instrumentation Amplifier

### Active Low-Pass Filter

The low-pass filter shown in Fig 11 has a DC gain of (-R2/R1) and the -3dB corner frequency is $1/2\pi R_2C$. Make sure the filter bandwidth is within the bandwidth of the amplifier. Feedback resistors with large values can couple with parasitic capacitance and cause undesired effects such as ringing or oscillation in high-speed amplifiers. Keep resistor values as low as possible and consistent with output loading consideration

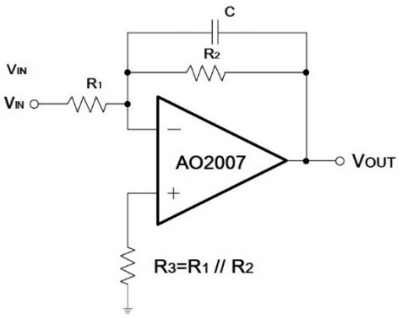



Fig 11. Active Low-Pass Filter

### Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1uF capacitor closely across the supply pins.

These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI susceptibility.

### Layout Example

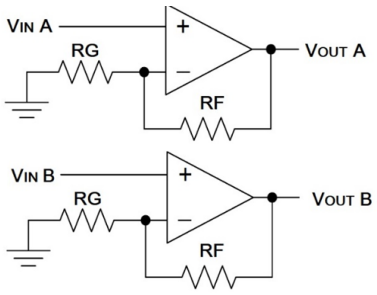



Fig 12. Schematic Representation

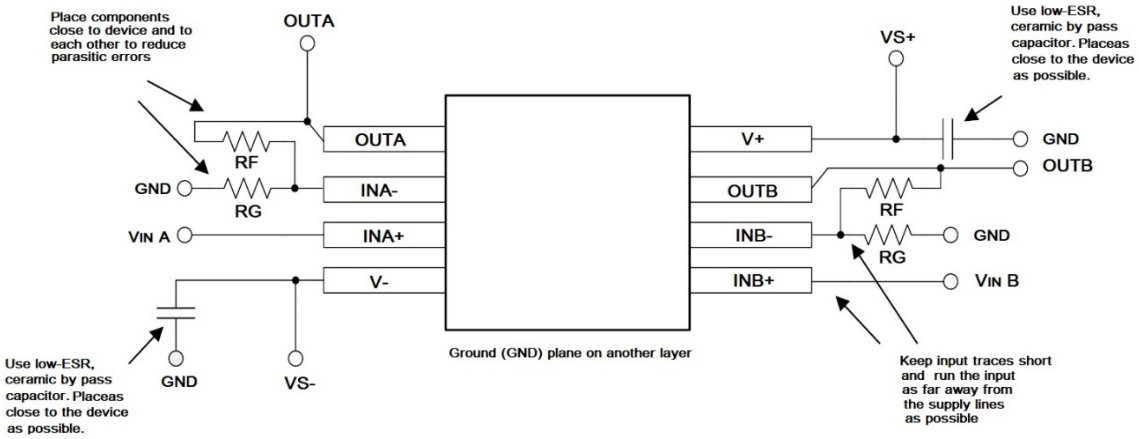
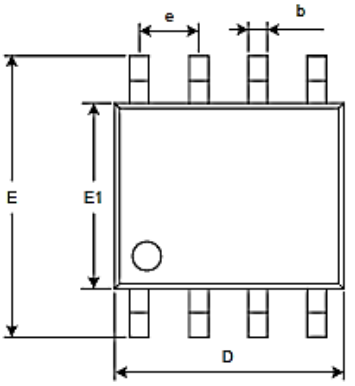
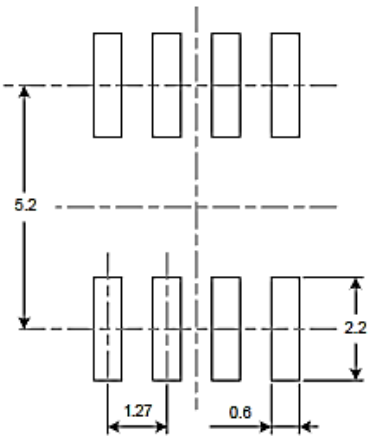



Fig 13. Layout Example

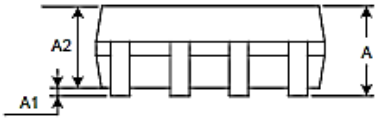
## PACKAGE INFORMATION

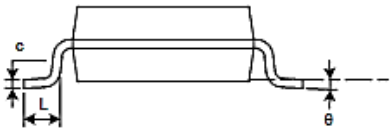
Dimension in SOP8 (Unit: mm)




RECOMMENDED LAND PATTERN




| Symbol | Millimeters | |
|---|---|---|
| | Min | Max |
| A | 1.350 | 1.750 |
| A1 | 0.100 | 0.250 |
| A2 | 1.350 | 1.550 |
| b | 0.330 | 0.510 |
| c | 0.170 | 0.250 |
| D | 4.800 | 5.000 |
| e | 1.270 BSC | |
| E | 5.800 | 6.200 |
| E1 | 3.800 | 4.000 |
| L | 0.400 | 1.270 |
| θ | 0° | 8° |

## IMPORTANT NOTICE

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