

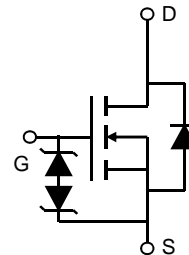
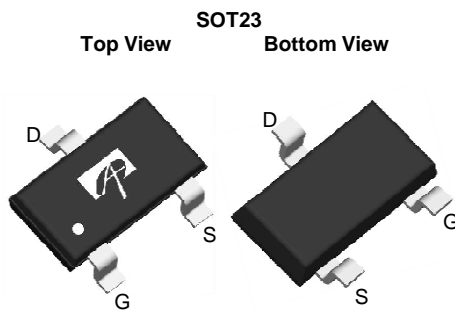
General Description

The AO3434 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications. It is ESD protected.

Product Summary

V_{DS} (V) = 30V
 I_D = 4.2A ($V_{GS} = 10V$)
 $R_{DS(ON)} < 52m\Omega$ ($V_{GS} = 10V$)
 $R_{DS(ON)} < 75m\Omega$ ($V_{GS} = 4.5V$)

ESD protected



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum		Units	
		10 sec	Steady-State		
Drain-Source Voltage	V_{DS}	30		V	
Gate-Source Voltage	V_{GS}	± 20		V	
Continuous Drain Current ^{A,F}	I_D	$T_A=25^\circ\text{C}$	4.2	3.5	A
		$T_A=70^\circ\text{C}$	3.3	2.8	
Pulsed Drain Current ^B	I_{DM}	30			
Power Dissipation	P_D	$T_A=25^\circ\text{C}$	1.4	1.0	W
		$T_A=70^\circ\text{C}$	0.9	0.64	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		$^\circ\text{C}$	

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	70	90	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Ambient ^A		Steady-State	100	125
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	63	80	$^\circ\text{C}/\text{W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±16V			10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	1	1.32	1.8	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =4.2A T _J =125°C		43 58	52 74	mΩ
		V _{GS} =4.5V, I _D =2A		59	75	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =4.2A		8.5		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.77	1	V
I _S	Maximum Body-Diode Continuous Current				1.8	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		269	340	pF
C _{oss}	Output Capacitance			65		pF
C _{riss}	Reverse Transfer Capacitance			41		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		1	1.5	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =4.2A		5.7	7.2	nC
Q _{g(4.5V)}	Total Gate Charge			3		nC
Q _{gs}	Gate Source Charge			1.37		nC
Q _{gd}	Gate Drain Charge			0.65		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =3.6Ω, R _{GEN} =3Ω		2.6	3.8	ns
t _r	Turn-On Rise Time			5.5	8	ns
t _{D(off)}	Turn-Off DelayTime			15.2	23	ns
t _f	Turn-Off Fall Time			3.7	5.5	ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =4.2A, di/dt=100A/μs		15.5	21	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =4.2A, di/dt=100A/μs		7.1		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The SOA curve provides a single pulse rating.

F: The current rating is based on the t≤10s thermal resistance rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

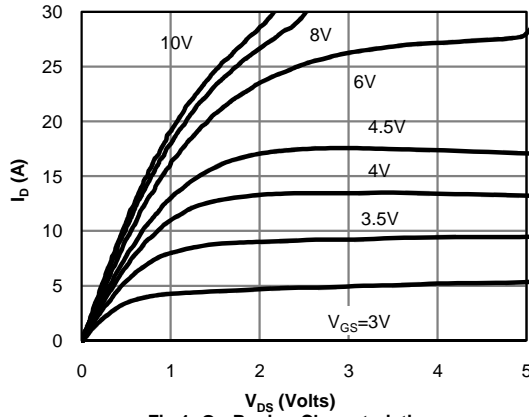


Fig 1: On-Region Characteristics

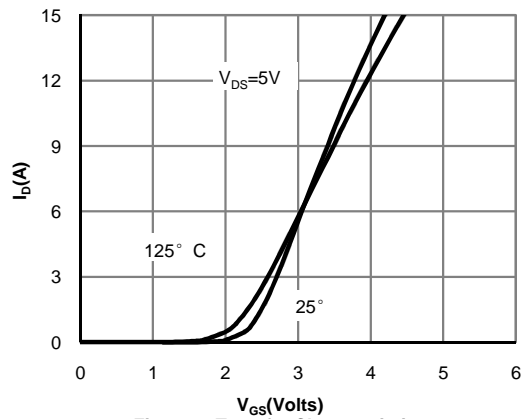


Figure 2: Transfer Characteristics

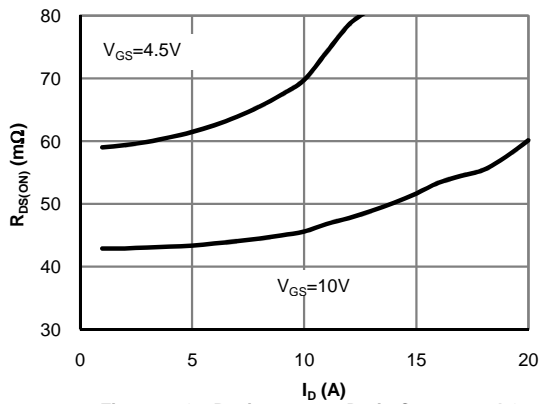


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

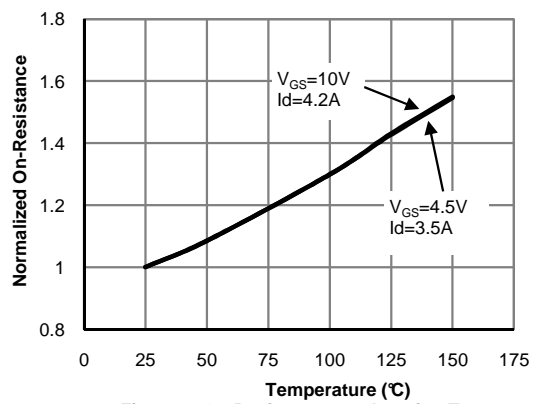


Figure 4: On-Resistance vs. Junction Temperature

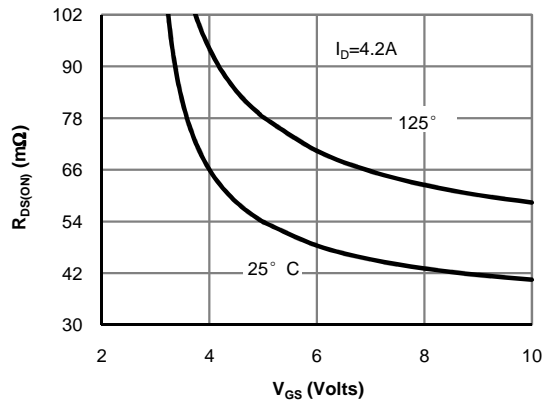


Figure 5: On-Resistance vs. Gate-Source Voltage

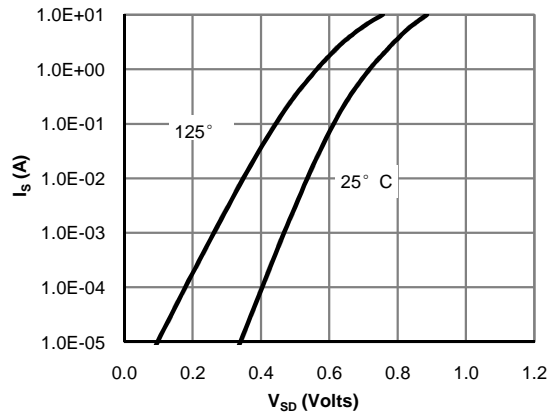


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

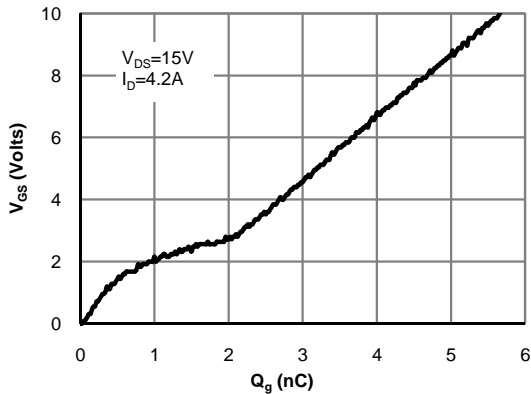


Figure 7: Gate-Charge Characteristics

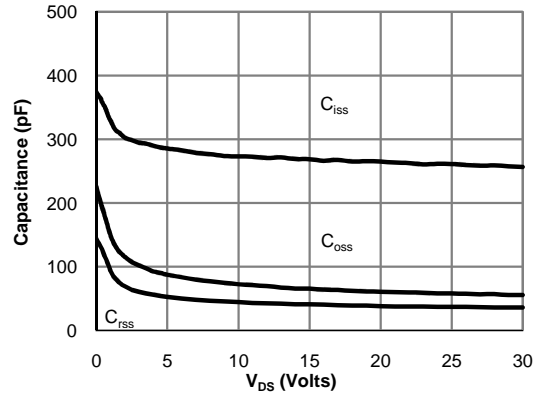


Figure 8: Capacitance Characteristics

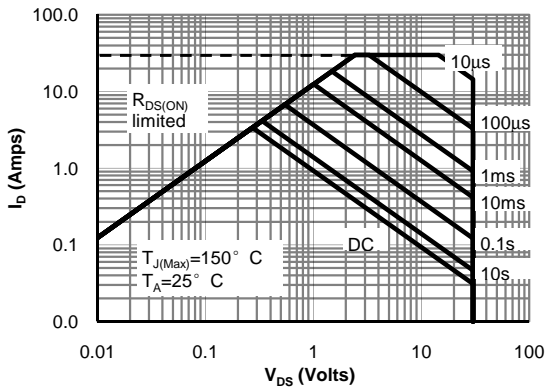


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

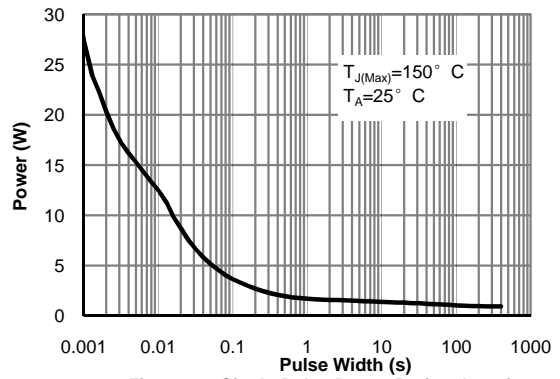


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

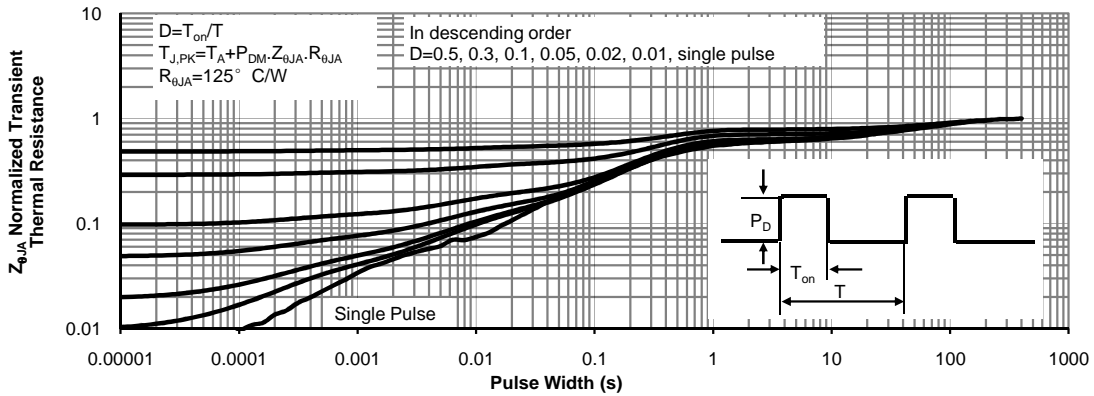


Figure 11: Normalized Maximum Transient Thermal Impedance