AO4480

40V N-Channel Enhancement Mode MOSFET

MAOYUAN semiconductor

General Description

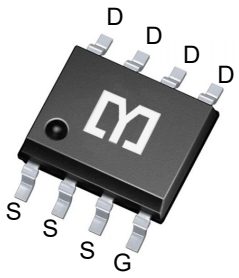
The AO4480 uses advanced trench technology to provide excellent RDS(ON), low gate charge.It is ESD Protected. This device is suitable for use as a low side switch in SMPS and general purpose applications.

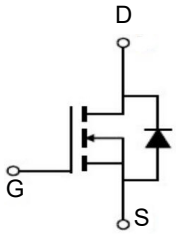
Features

V_{DSS}	40	V
I_D	14	A
$R_{DS(ON)}$(atV_{GS}=10V)	<11.5	mΩ
$R_{DS(ON)}$(atV_{GS}=4.5V)	<15.5	mΩ

Application

- Battery protection
- Load switch
- PWM application





Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AO4480	SOP-8	4480	3000

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [AF]	T_A=25℃	I_{DSM}	14	A
	T_A=70℃		11	
Pulsed Drain Current [B]		I_{DM}	70	
Power Dissipation	T_A=25℃	P_D	3.1	W
	T_A=70℃		2.0	
Avalanche Current [B]		I_{AR}	30	A
Repetitive avalanche energy 0.3mH [B]		E_{AR}	135	mJ
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	30	40	℃/W
Maximum Junction-to-Ambient [A]	Steady-State		59	75	℃/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	16	24	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250uA, V_{GS}=0V	40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=32V, V_{GS}=0V			1	uA
		T_J=55℃			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			±100	μA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250μA	1	2	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	70			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=14A		9	11.5	mΩ
		T_J=125℃		13		
		V_{GS}=4.5V, I_D=5A		12	15.5	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=14A		50		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				4	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=20V, f=1MHz		1600	1920	pF
C_{oss}	Output Capacitance			320		pF
C_{rss}	Reverse Transfer Capacitance			100		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		3.4		Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=20V, I_D=14A		22		nC
Q_g(4.5V)	Total Gate Charge			10.5		nC
Q_{gs}	Gate Source Charge			4.2		nC
Q_{gd}	Gate Drain Charge			4.8		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=20V, R_L=1.5Ω, R_{GEN}=3Ω		3.5		ns
t_r	Turn-On Rise Time			6		ns
$t_{D(off)}$	Turn-Off DelayTime			13.2		ns
t_f	Turn-Off Fall Time			3.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=14A, dI/dt=100A/μs		31		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=14A, dI/dt=100A/μs		33		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25℃. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25℃. The SOA curve provides a single pulse rating.

F. The current rating is based on the t≤ 10s junction to ambient thermal resistance rating.

Rev2: Nov. 2010

Typical Characteristics

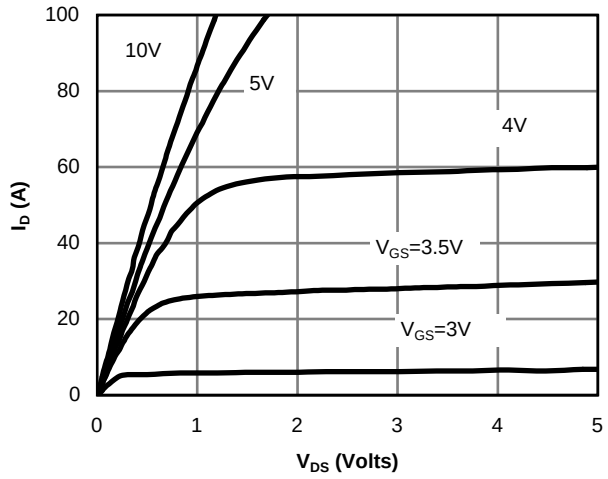


Figure 1: On-Region Characteristics

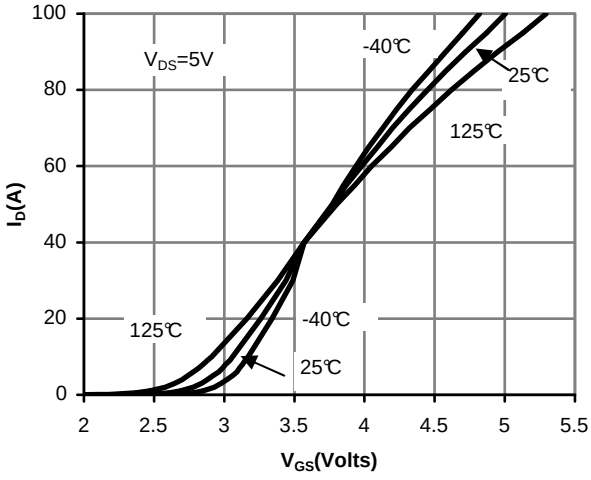


Figure 2: Transfer Characteristics

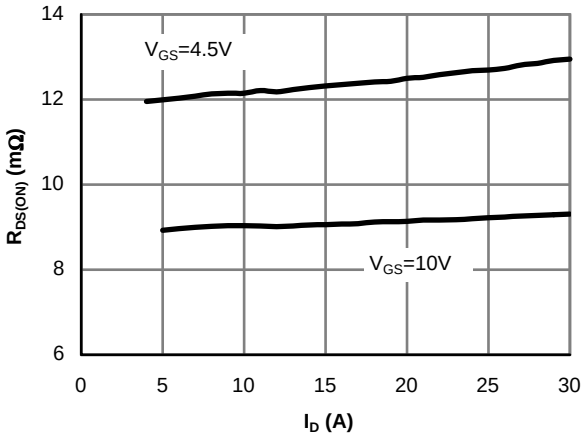


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

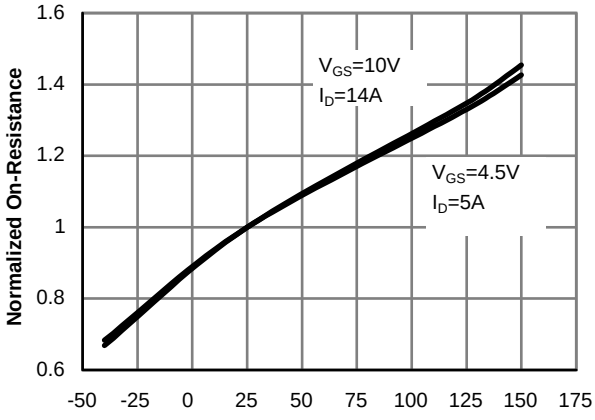


Figure 4: On-Resistance vs. Junction Temperature

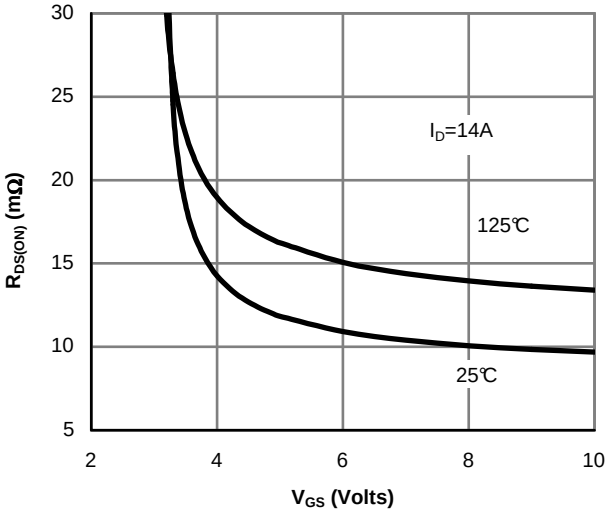


Figure 5: On-Resistance vs. Gate-Source Voltage

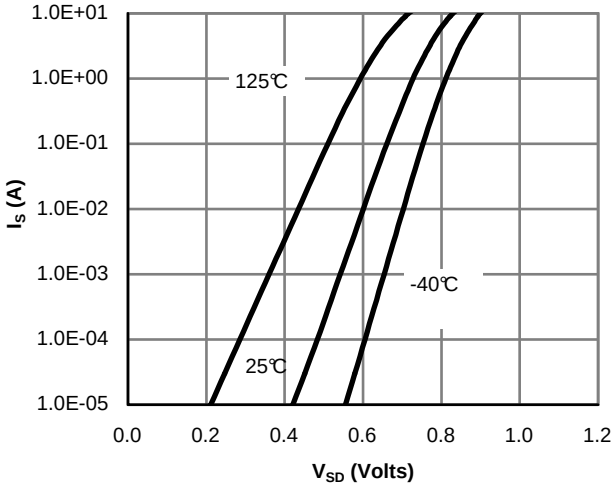


Figure 6: Body-Diode Characteristics

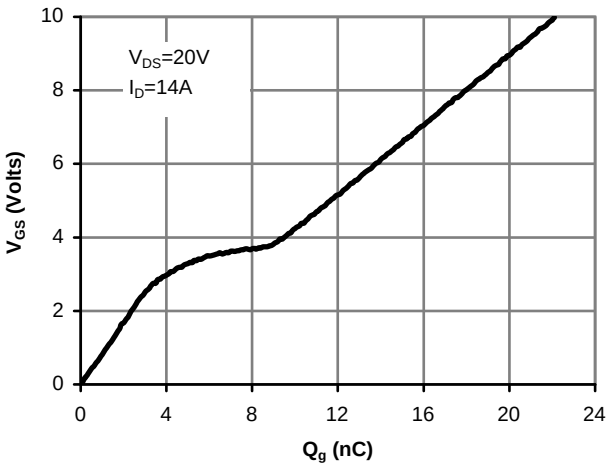


Figure 7: Gate-Charge Characteristics

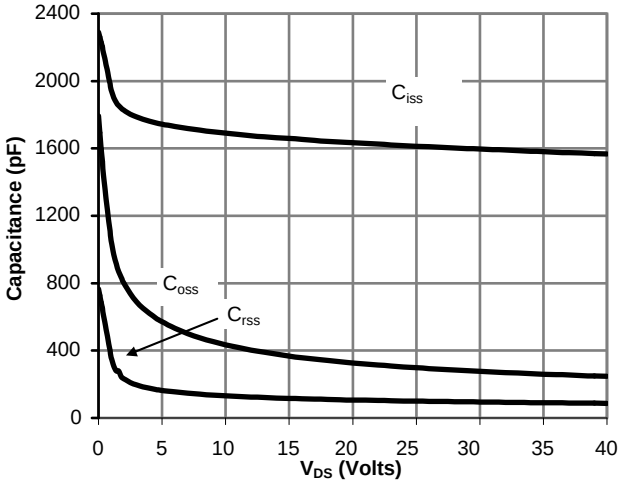


Figure 8: Capacitance Charact eristics

500

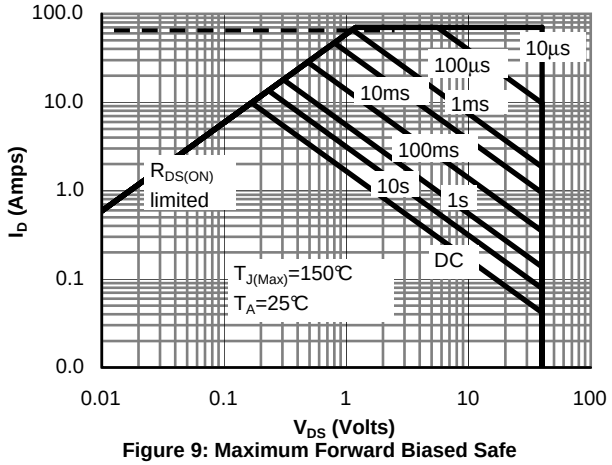


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

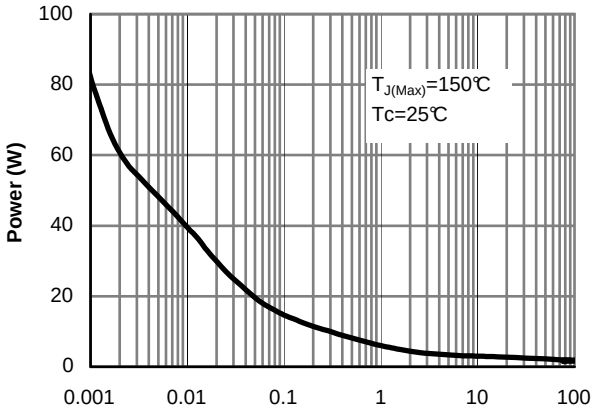


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

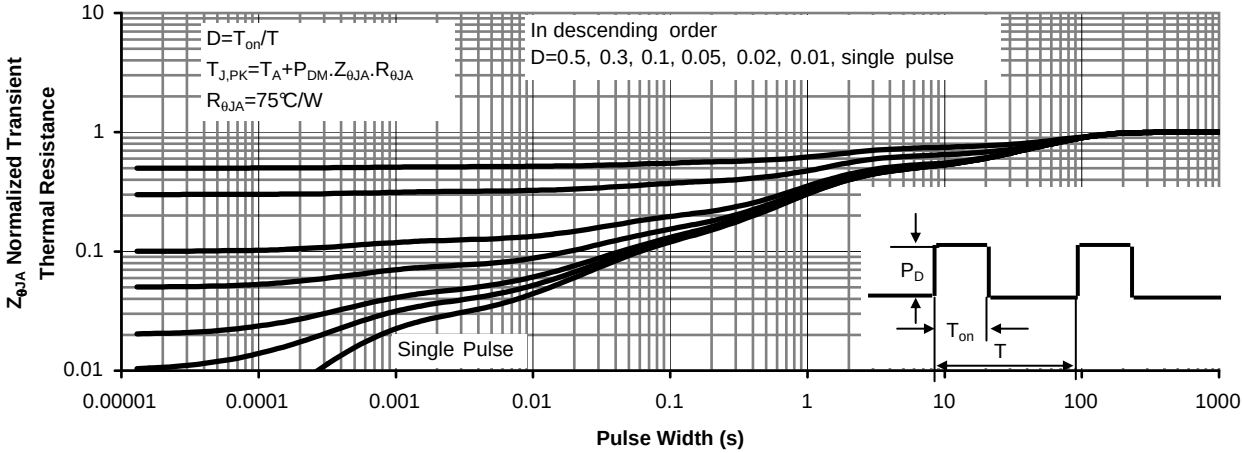
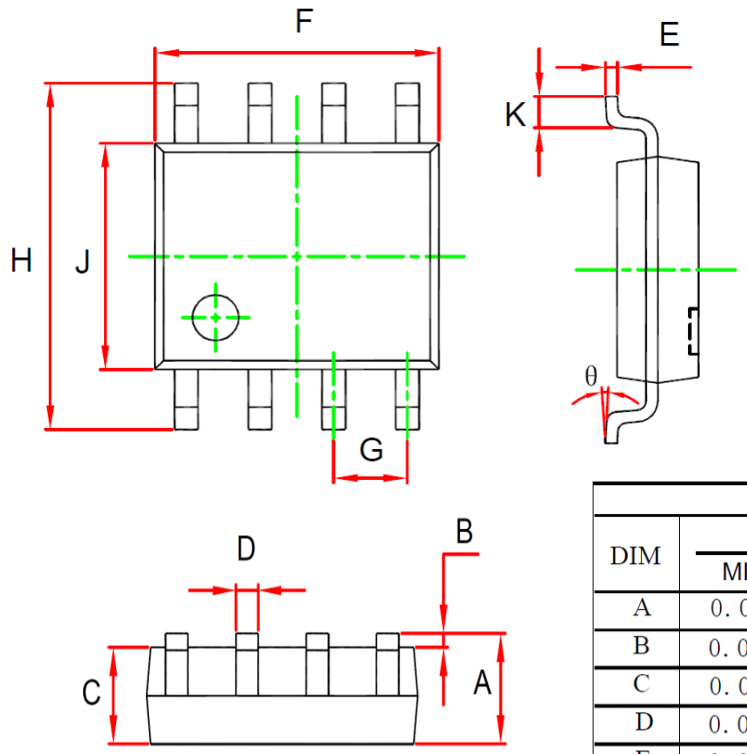


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Package Mechanical Data-SOP-8



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.350	1.750	
B	0.004	0.010	0.100	0.250	
C	0.053	0.061	1.350	1.550	
D	0.013	0.020	0.330	0.510	
E	0.007	0.010	0.170	0.250	
F	0.189	0.197	4.800	5.000	
G	0.050 (BSC)		1.270 (BSC)		
H	0.228	0.244	5.800	6.200	
J	0.150	0.157	3.800	4.000	
K	0.016	0.050	0.400	1.270	
θ	0°	8°	0°	8°	