



AO4621

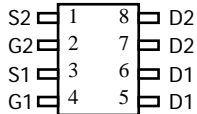
Complementary Enhancement Mode Field Effect Transistor

General Description

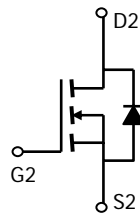
The AO4621 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications. *Standard Product AO4621 is Pb-free (meets ROHS & Sony 259 specifications). AO4621L is a Green Product ordering option. AO4621 and AO4621L are electrically identical.*

Features

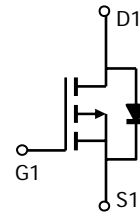
n-channel	p-channel
$V_{DS} (V) = 40V$	-40V
$I_D = 6A (V_{GS}=10V)$	-5A ($V_{GS} = -10V$)
$R_{DS(ON)}$	$R_{DS(ON)}$
< 31m Ω ($V_{GS}=10V$)	< 45m Ω ($V_{GS} = -10V$)
< 45m Ω ($V_{GS}=4.5V$)	< 63m Ω ($V_{GS} = -4.5V$)



SOIC-8



n-channel



p-channel

Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	40	-40	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current ^A	I_D	$T_A=25^\circ C$	6	-5
		$T_A=70^\circ C$	5	-4
Pulsed Drain Current ^B	I_{DM}	20	-20	A
Power Dissipation	P_D	$T_A=25^\circ C$	2	2
		$T_A=70^\circ C$	1.28	1.28
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	-55 to 150	$^\circ C$

Thermal Characteristics: n-channel and p-channel

Parameter	Symbol	Device	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	n-ch	48	62.5	$^\circ C/W$
Maximum Junction-to-Ambient ^A		n-ch	74	110	$^\circ C/W$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	n-ch	35	50	$^\circ C/W$
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	p-ch	48	62.5	$^\circ C/W$
Maximum Junction-to-Ambient ^A		p-ch	74	110	$^\circ C/W$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	p-ch	35	50	$^\circ C/W$

N Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=10\text{mA}, V_{GS}=0\text{V}$	40			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=32\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1	μA
					5	
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1	2.3	3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}, V_{DS}=5\text{V}$	20			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=6\text{A}$ $T_J=125^\circ\text{C}$		23.2	31	m Ω
				36	48	
		$V_{GS}=4.5\text{V}, I_D=5\text{A}$		32.6	45	m Ω
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=6\text{A}$		22		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.77	1	V
I_S	Maximum Body-Diode Continuous Current				2	A
DYNAMIC PARAMETERS						
C_{ISS}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=20\text{V}, f=1\text{MHz}$		404		pF
C_{OSS}	Output Capacitance			95		pF
C_{RSS}	Reverse Transfer Capacitance			37		pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$		2.7		Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=20\text{V}, I_D=6\text{A}$		8.3		nC
$Q_g(4.5\text{V})$	Total Gate Charge			4.2		nC
Q_{gs}	Gate Source Charge			1.3		nC
Q_{gd}	Gate Drain Charge			2.3		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}, V_{DS}=20\text{V}, R_L=3.3\Omega,$ $R_{GEN}=3\Omega$		4.2		ns
t_r	Turn-On Rise Time			3.3		ns
$t_{D(off)}$	Turn-Off DelayTime			15.6		ns
t_f	Turn-Off Fall Time			3		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=6\text{A}, dI/dt=100\text{A}/\mu\text{s}$		20.5		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=6\text{A}, dI/dt=100\text{A}/\mu\text{s}$		14.5		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $t_s \leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using 80 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CANNEL

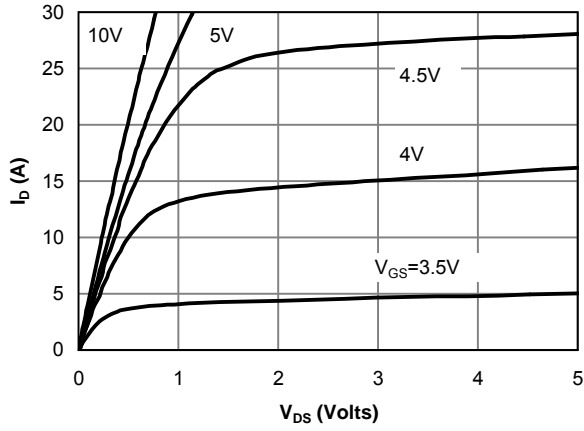


Figure 1: On-Region Characteristics

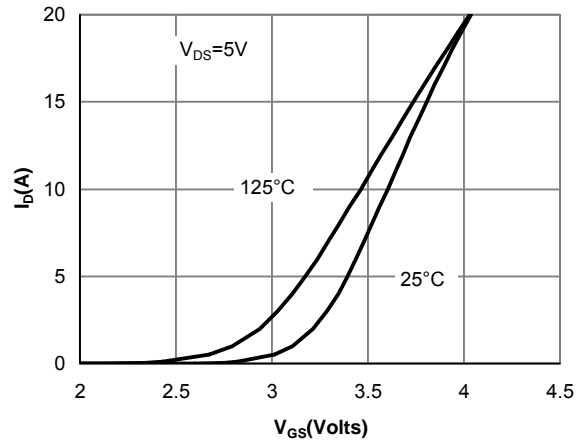


Figure 2: Transfer Characteristics

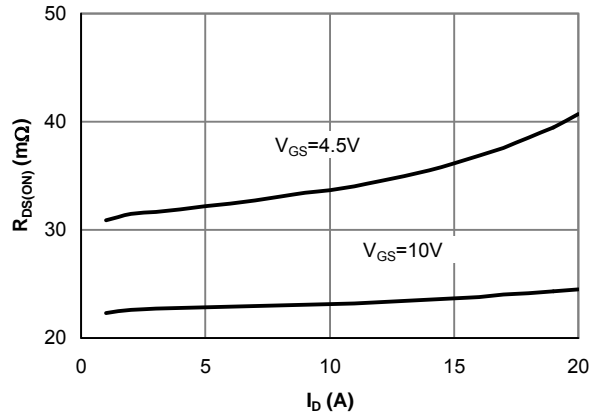


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

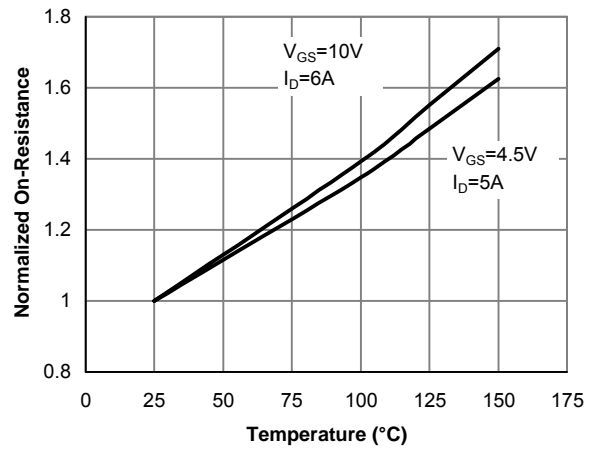


Figure 4: On-Resistance vs. Junction Temperature

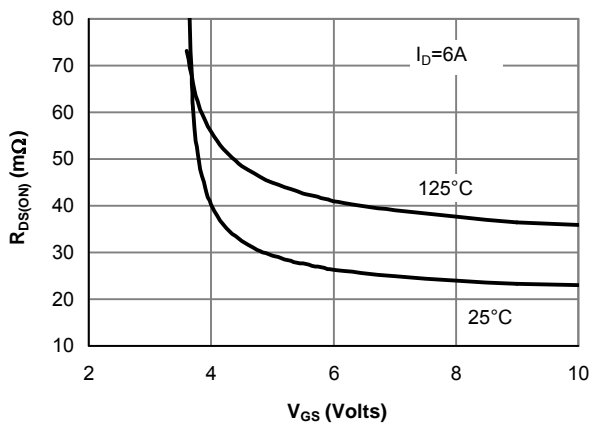


Figure 5: On-Resistance vs. Gate-Source Voltage

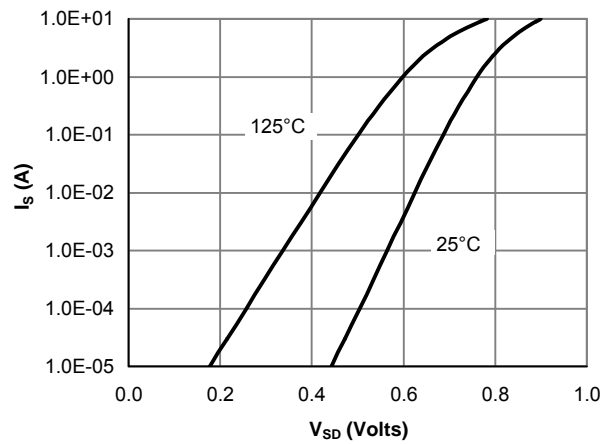


Figure 6: Body-Diode Characteristics

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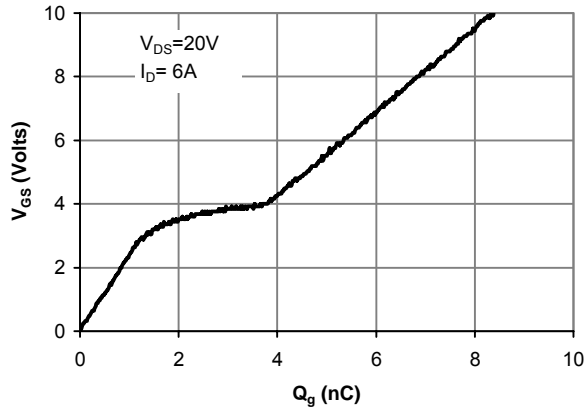


Figure 7: Gate-Charge Characteristics

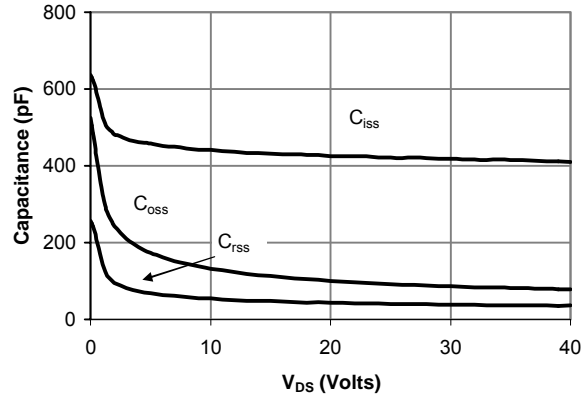


Figure 8: Capacitance Characteristics

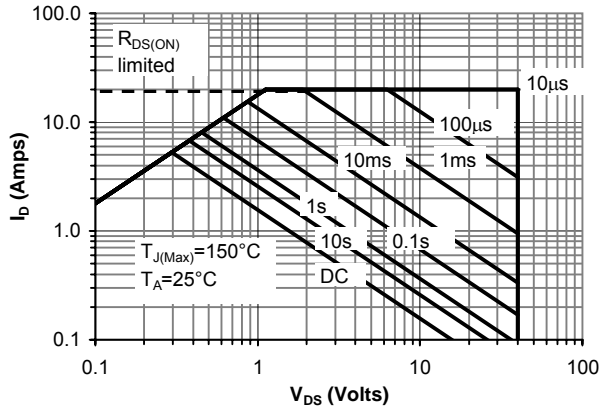


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

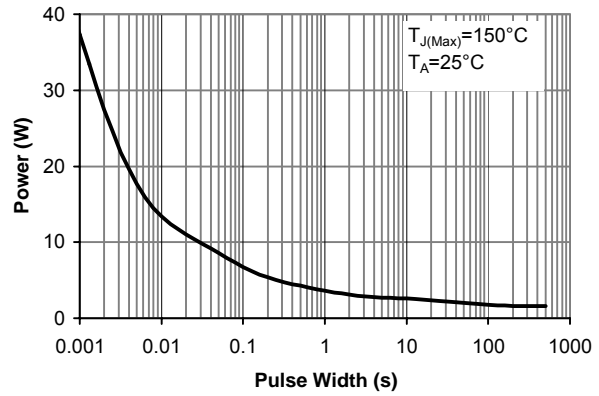


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

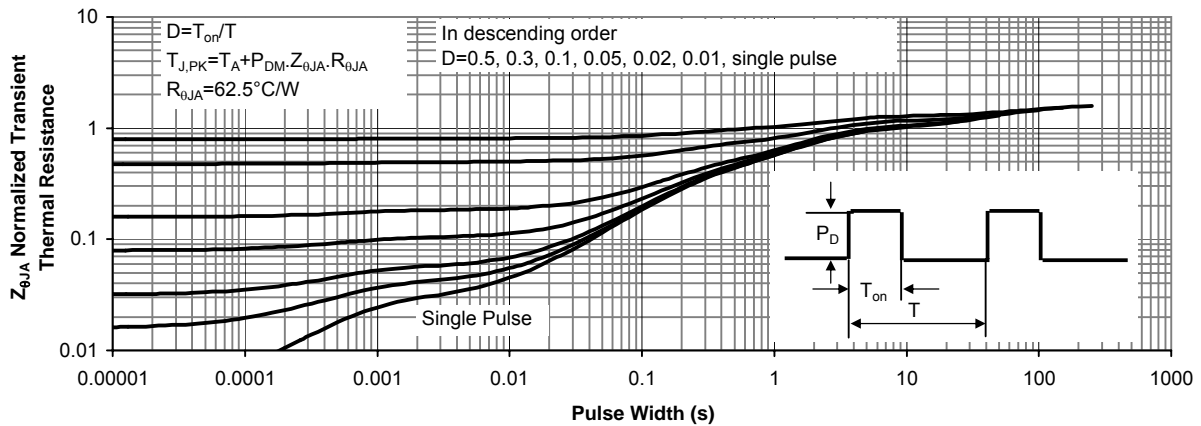


Figure 11: Normalized Maximum Transient Thermal Impedance

P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-10\text{mA}$, $V_{GS}=0\text{V}$	-40			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-32\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			-1	μA
					-5	
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-1	-1.9	-3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-10\text{V}$, $V_{DS}=-5\text{V}$	-20			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}$, $I_D=-5\text{A}$ $T_J=125^\circ\text{C}$		32.5	45	m Ω
				52	65	
		$V_{GS}=-4.5\text{V}$, $I_D=-2\text{A}$		51.4	63	m Ω
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}$, $I_D=-4.8\text{A}$		12		S
V_{SD}	Diode Forward Voltage	$I_S=-1\text{A}$, $V_{GS}=0\text{V}$		-0.75	-1	V
I_S	Maximum Body-Diode Continuous Current				-2.6	A
DYNAMIC PARAMETERS						
C_{ISS}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=-20\text{V}$, $f=1\text{MHz}$		657		pF
C_{OSS}	Output Capacitance			143		pF
C_{RSS}	Reverse Transfer Capacitance			63		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		6.5		Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge (10V)	$V_{GS}=-10\text{V}$, $V_{DS}=-20\text{V}$, $I_D=-5\text{A}$		13.6		nC
$Q_g(4.5\text{V})$	Total Gate Charge (4.5V)			6.8		nC
Q_{gs}	Gate Source Charge			1.8		nC
Q_{gd}	Gate Drain Charge			3.9		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=-10\text{V}$, $V_{DS}=-20\text{V}$, $R_L=4\Omega$, $R_{GEN}=3\Omega$		7.5		ns
t_r	Turn-On Rise Time			6.7		ns
$t_{D(off)}$	Turn-Off DelayTime			26		ns
t_f	Turn-Off Fall Time			11.2		ns
t_{rr}	Body Diode Reverse Recovery Time		$I_F=-5\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		22.3	
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-5\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		15.2		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $\leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using 80 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

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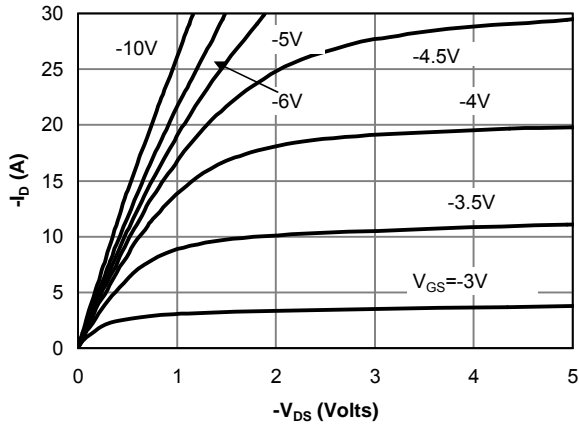


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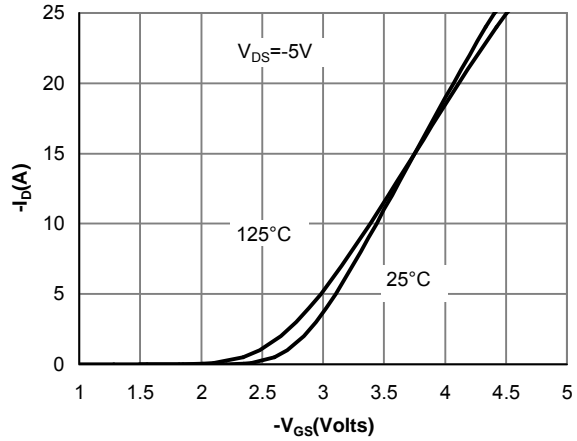


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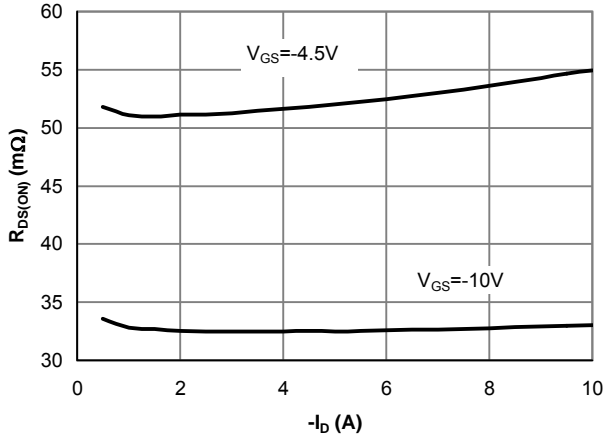


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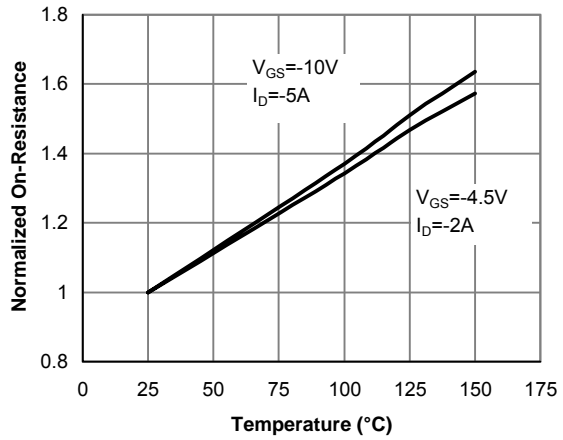


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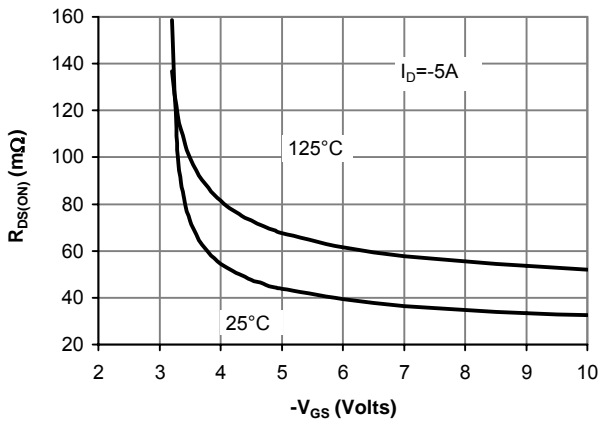


Figure 5: On-Resistance vs. Gate-Source Voltage

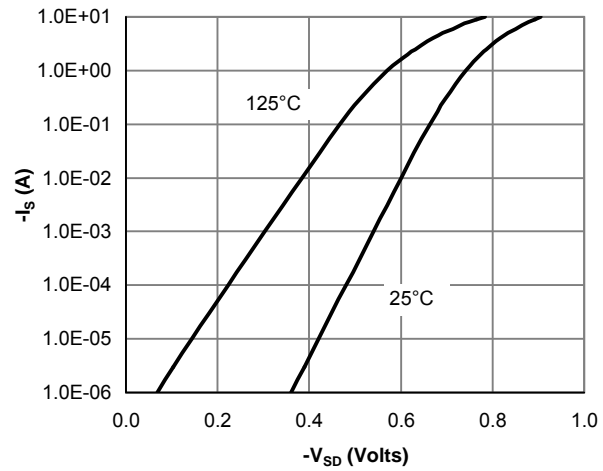


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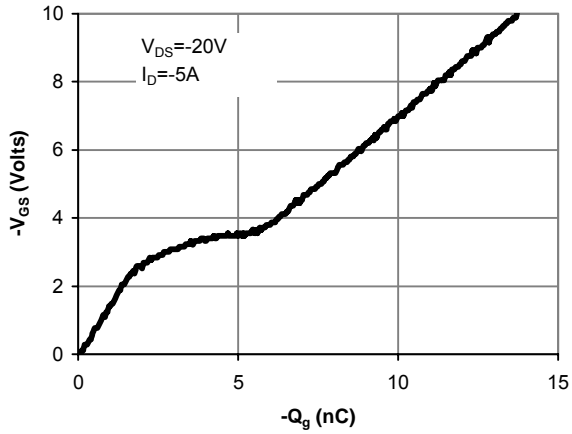


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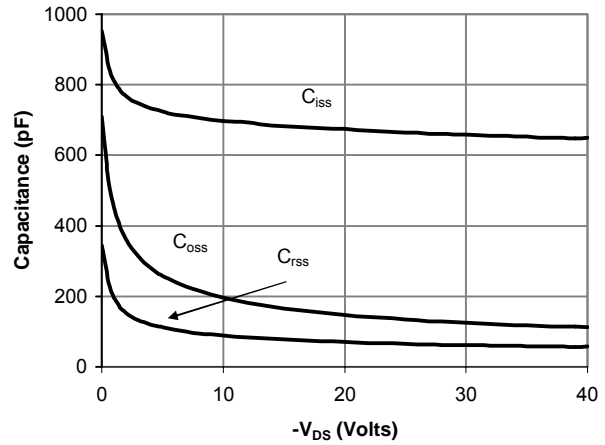


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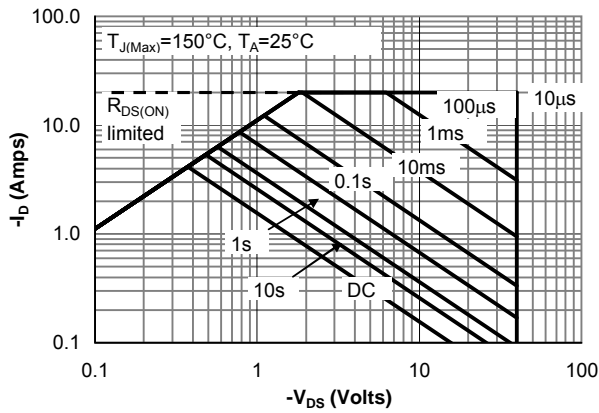


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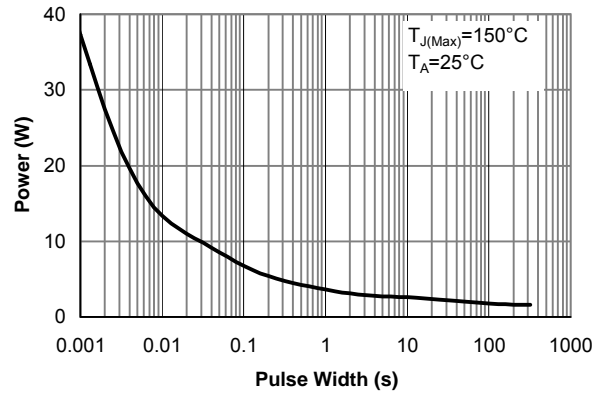


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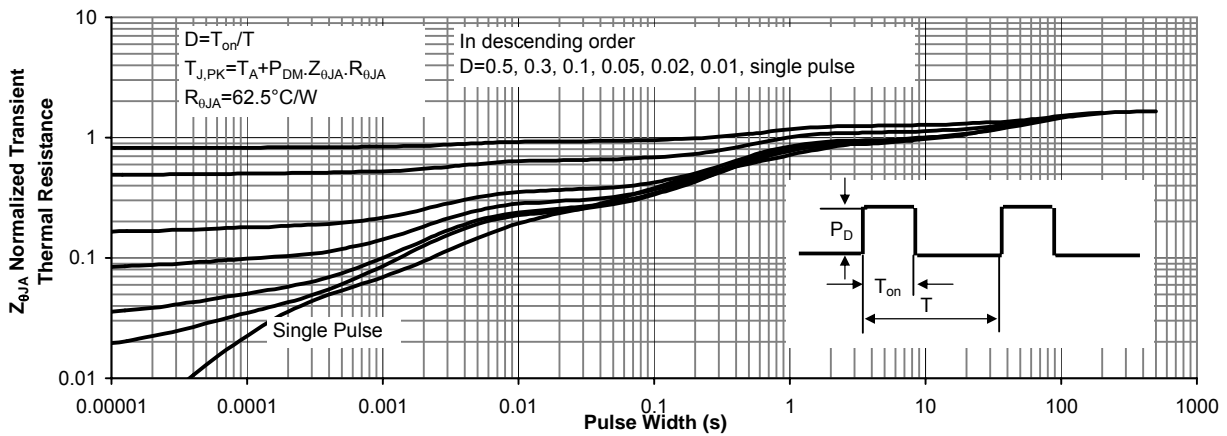


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