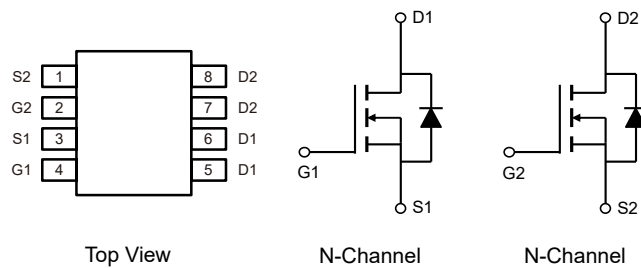


1.Features

- $V_{DS(V)}=40V$
- $I_D=7A(V_{GS}=10V)$
- $R_{DS(ON)}<0.028\Omega(V_{GS}=10V)$
- $R_{DS(ON)}<0.03\Omega(V_{GS}=4.5V)$
- TrenchFET® power MOSFET
- 100 % R_g and UIS tested

2.Pinning information

Pin	Symbol	Description
1,3	S2,S1	SOURCE
2,4	G2,G1	GATE
5,6,7,8	D2,D1	DRAIN



3.Absolute Maximum Ratings $T_c=25^{\circ}C$

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	$T_c=25^{\circ}C$	I_D	7	A
	$T_c=125^{\circ}C$		4	
Continuous Source Current (Diode Conduction) ^a		I_S	3.6	
Pulsed Drain Current ^b		I_{DM}	28	
Single Pulse Avalanche Current	L=0.1mH	I_{AS}	18	
Single Pulse Avalanche Energy		E_{AS}	16.2	mJ
Maximum Power Dissipation ^b	$T_c=25^{\circ}C$	P_D	4	W
	$T_c=125^{\circ}C$		1.3	W
Storage Temperature		T_J, T_{STG}	-55 to 150	$^{\circ}C$



4.Thermal Resistance Rating

Parameter		Symbol	Typ	Max	Units
Junction-to-Ambient	PCB Mount ^c	R _{thJA}	90	110	°C/W
Junction-to-Foot (Drain)		R _{thJF}	60	34	°C/W

Notes

- a. Package limited.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- c. When mounted on 1" square PCB (FR4 material).



5. Electrical Characteristic ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} =0V, I _D =250μA	40			V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.5	2	2.5	V
Gate-source leakage	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero gate voltage drain current	I _{DSS}	V _{GS} =0V, V _{DS} =60V			1	μA
		V _{GS} =0V,V _{DS} =60V,T _J =125°C			50	μA
		V _{GS} =0V,V _{DS} =60V,T _J =175°C			150	μA
On-State Drain Current ^a	I _{D(ON)}	V _{GS} =10V, V _{DS} ≥5V	20			A
Drain-Source On-State Resistance ^a	R _{DS(ON)}	V _{GS} =10V, I _D =4.5A		0.028		Ω
		V _{GS} =4.5V, I _D =4A		0.03		Ω
Forward transconductance ^f	g _{FS}	V _{DS} =15V, I _D =4.5A		15		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1MHz		600	750	pF
Output Capacitance	C _{oss}			110	140	pF
Reverse Transfer Capacitance	C _{rss}			50	62	pF
Total gate charge ^c	Q _g	V _{DS} =30V, V _{GS} =10V, I _D =5.3A		11.7	18	nC
Gate-source charge ^c	Q _{gs}			1.8	2.7	nC
Gate-drain charge ^c	Q _{gd}			2.8	4.2	nC
Gate resistance	R _g	f=1MHz	1.3		6	Ω
Turn-On Delay Time ^c	t _{D(on)}	V _{DS} =30V R _L =6.8Ω, I _D ≈4.4A V _{GEN} =10V, R _G =1Ω		7	11	ns
Rise Time ^c	t _r			3.3	5	ns
Turn-Off Delay Time ^c	t _{D(off)}			22.4	33.5	ns
Fall time ^c	t _f			2.1	3.2	ns
Source-Drain Diode Ratings and Characteristics ^b						
Pulsed Current ^a	I _{SM}	I _F =2A, V _{GS} =0V			28	A
Forward Voltage	V _{SD}	I _F =2A, V _{GS} =0V		0.75	1.1	V

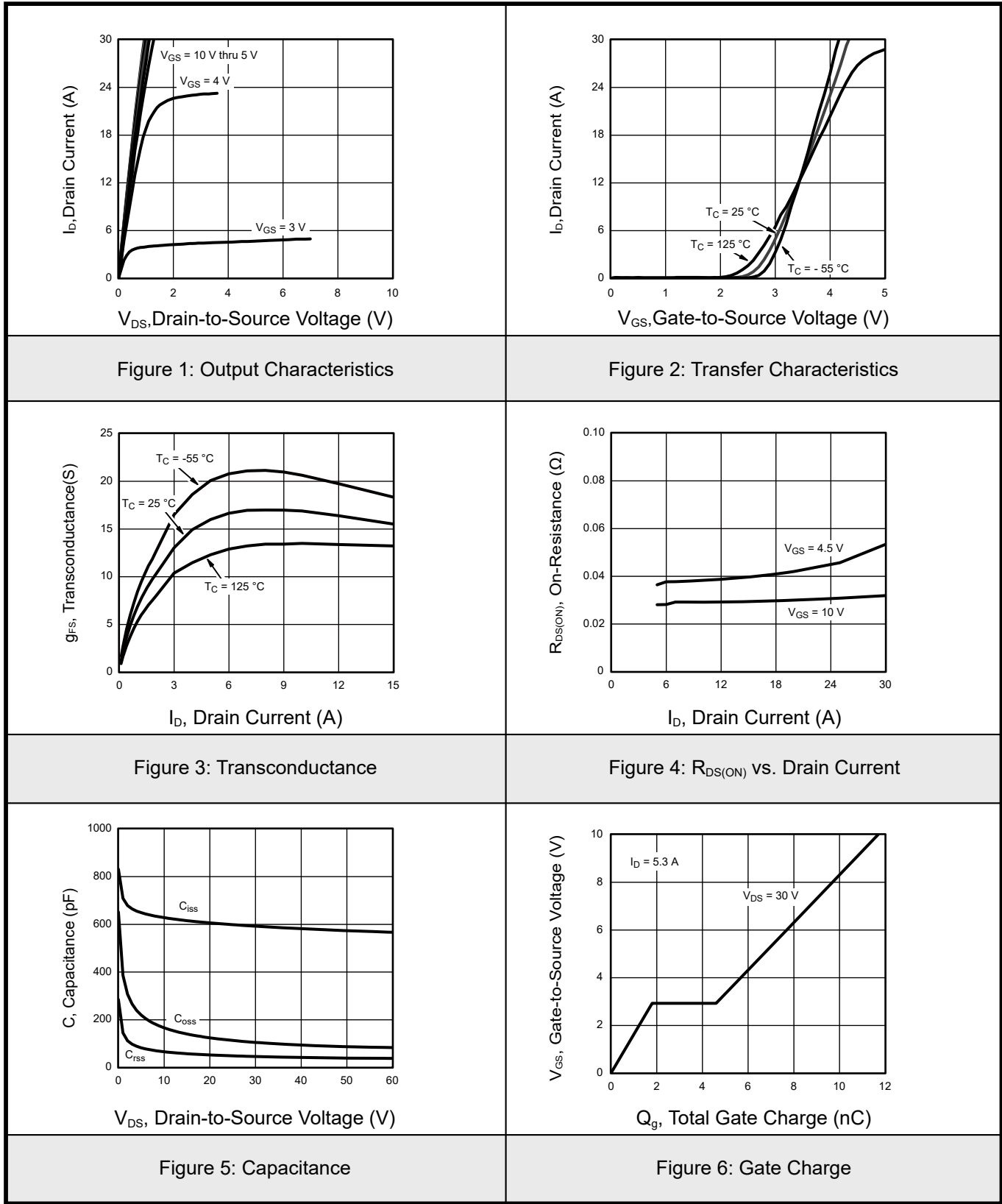
a. Pulse test; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

c. Independent of operating temperature.

b. Guaranteed by design, not subject to production testing.



6.1 Typical characteristic





6.2Typical characteristic

Figure 7: On-Resistance vs. Junction Temperature	Figure 8: Drain Source Breakdown vs. Junction Temperature
Figure 9: Source Drain Diode Forward Voltage	Figure 10: On-Resistance vs. Gate-to-Source Voltage
Figure 11: Threshold Voltage	Figure 12: Safe Operating Area



6.3Typical characteristic

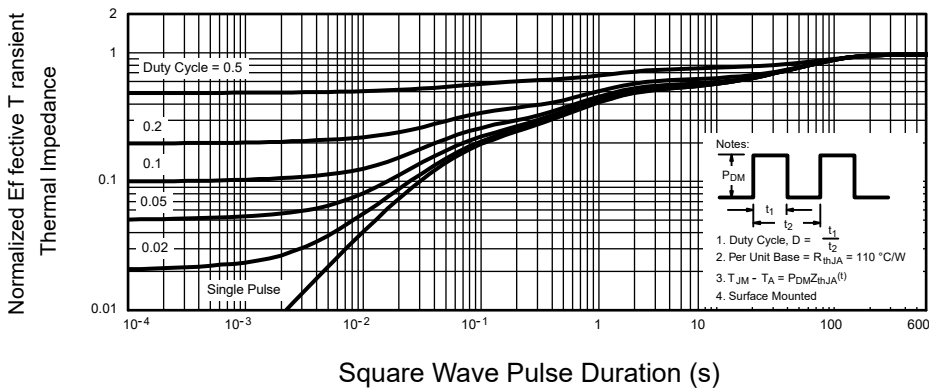


Figure 13: Normalized Thermal Transient Impedance, Junction-to-Ambient

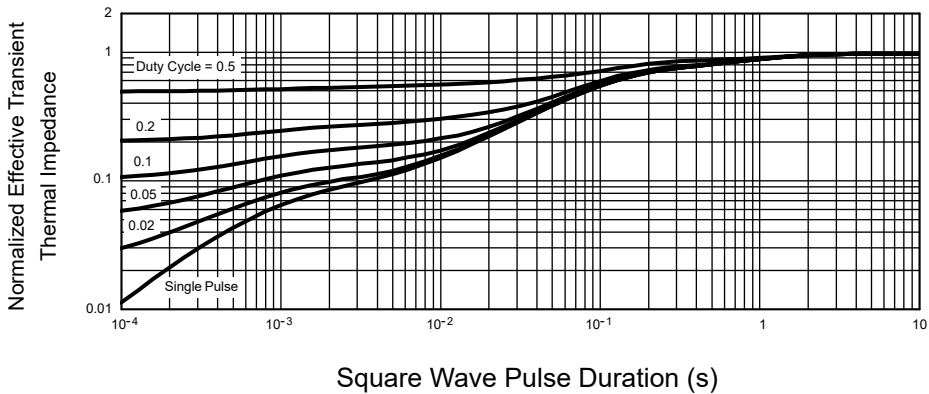
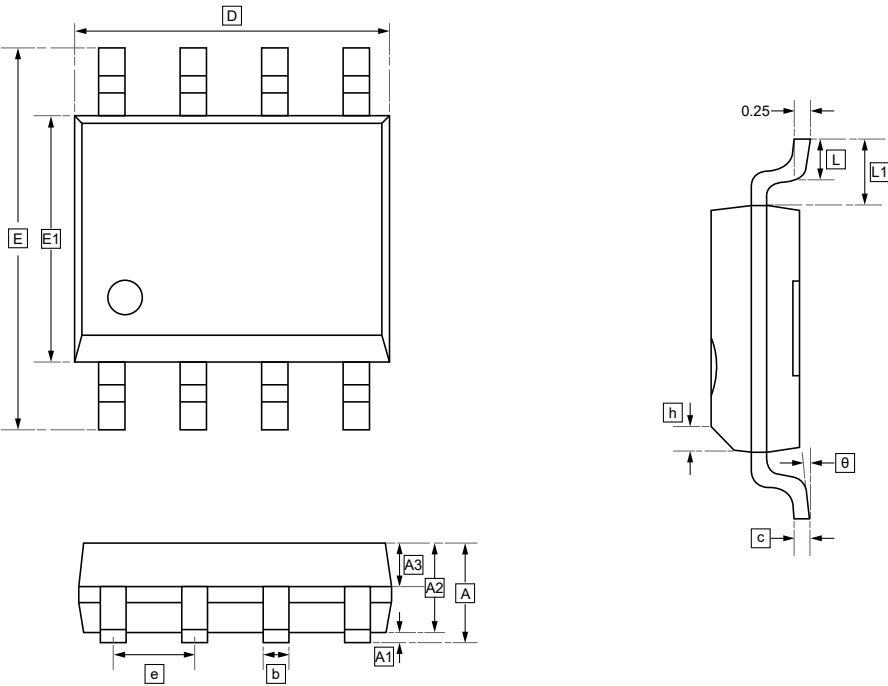


Figure 14: Normalized Thermal Transient Impedance, Junction-to-Foot



7.SOP-8 Package Outline Dimensions



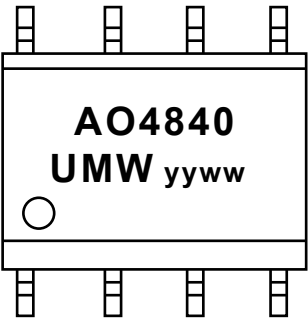
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.80	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.00	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°



8.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW AO4840	SOP-8	3000	Tape and reel



9.Disclaimer

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