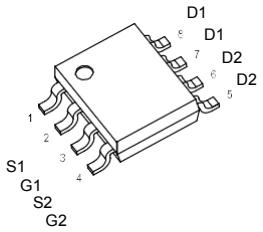
Product Summary

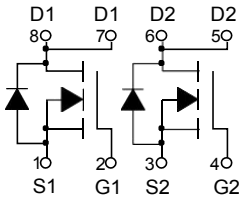
V_{DS}	30V
I_D (at V_{GS}=10V)	6A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 30mΩ
$R_{DS(ON)}$ (at V_{GS} =4.5V)	< 42mΩ



SOP-8

General Description

The AO4842-MSuses advanced trench technology to provide excellent RDS(ON) and low gate charge. This device is suitable for use as a load switch or in PWM applications.



N-Channel MOSFET

Absolute Maximum Ratings T_A=25°C unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A=25°C	I_D	6	A
	T_A=70°C		5	
Pulsed Drain Current [C]		I_{DM}	30	
Avalanche Current [C]		I_{AS}, I_{AR}	10	A
Avalanche energy L=0.1mH [C]		E_{AS}, E_{AR}	5	mJ
Power Dissipation [B]	T_A=25°C	P_D	2	W
	T_A=70°C		1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	48	62.5	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		74	90	°C/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	32	40	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250μA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250μA	1.2	1.8	2.4	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=6A		25	30	mΩ
		T_J=125°C		40	48	
		V_{GS}=4.5V, I_D=5A		33	42	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=6A		15		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.76	1	V
I_S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		255	310	pF
C_{oss}	Output Capacitance			45		pF
C_{rss}	Reverse Transfer Capacitance			35	50	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	1.6	3.25	4.9	Ω
SWITCHING PARAMETERS						
$Q_{g(10V)}$	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=6A		5.2	6.3	nC
$Qg_{(4.5V)}$				2.55	3.2	nC
Q_{gs}	Gate Source Charge			0.85		nC
Q_{gd}	Gate Drain Charge			1.3		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=2.5Ω, R_{GEN}=3Ω		4.5		ns
t_r	Turn-On Rise Time			2.5		ns
$t_{D(off)}$	Turn-Off DelayTime			14.5		ns
t_f	Turn-Off Fall Time			3.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=6A, dI/dt=100A/μs		8.5		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=6A, dI/dt=100A/μs		2.2		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using ≤ 10s junction-to-ambient thermal resistance.

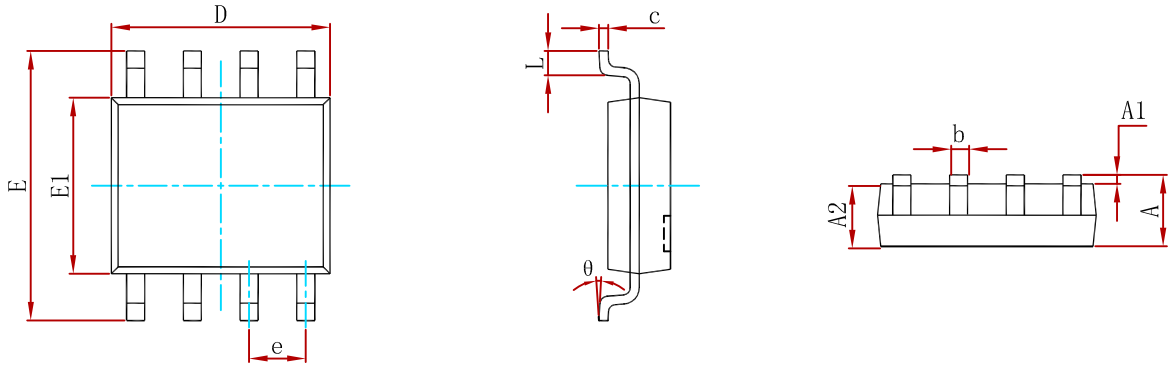
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initialT_J=25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

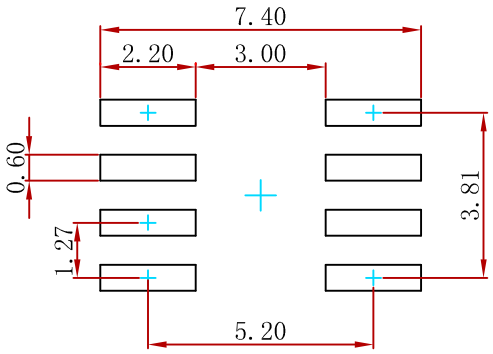
F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse ratin g.

PACKAGE MECHANICAL DATA



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

REEL SPECIFICATION

P/N	PKG	QTY
AO4842-MS	SOP-8	3000

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