

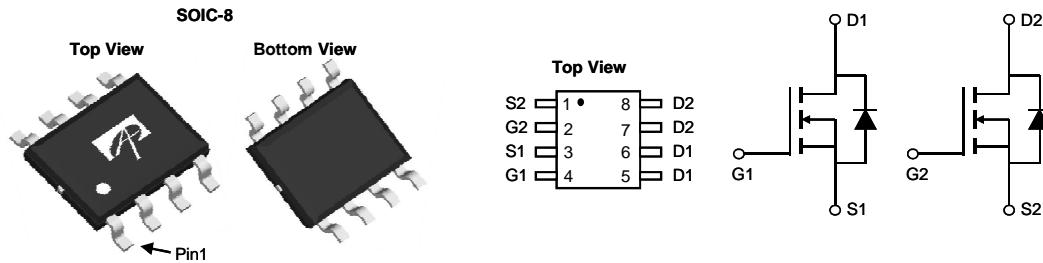
**General Description**

The AO4886 combines advanced trench MOSFET technology with a low resistance package to provide extremely low  $R_{DS(ON)}$ . This device is ideal for boost converters and synchronous rectifiers for consumer, telecom, industrial power supplies and LED backlighting.

**Product Summary**

$V_{DS}$	100V
$I_D$ (at $V_{GS}=10V$ )	3.3A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 80m $\Omega$
$R_{DS(ON)}$ (at $V_{GS} = 4.5V$ )	< 91m $\Omega$

100% UIS Tested  
 100%  $R_g$  Tested


**Absolute Maximum Ratings  $T_A=25^\circ C$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_A=25^\circ C$	3.3
		$T_A=70^\circ C$	2.7
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	17	A
Avalanche Current <sup>C</sup>	$I_{AS}, I_{AR}$	14	A
Avalanche energy $L=0.1mH$ <sup>C</sup>	$E_{AS}, E_{AR}$	10	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_A=25^\circ C$	2.00
		$T_A=70^\circ C$	1.28
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ C$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	48	62.5	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A D</sup>		74	90	$^\circ C/W$
Maximum Junction-to-Lead	$R_{\theta JL}$	32	40	$^\circ C/W$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	100			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.6	2.2	2.7	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	17			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =3A T <sub>J</sub> =125°C		63.5 122	80 152	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =3A		70	91	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =3A		20		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.74	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				2.5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =50V, f=1MHz	620	778	942	pF
C <sub>oss</sub>	Output Capacitance		38	55	81	pF
C <sub>riss</sub>	Reverse Transfer Capacitance		13	24	35	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.7	1.45	2.2	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>D</sub> =3A	13	16.3	20	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge		6.4	8.1	10	nC
Q <sub>gs</sub>	Gate Source Charge		2.2	2.8	3.4	nC
Q <sub>gd</sub>	Gate Drain Charge		2.4	4.1	5.8	nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, R <sub>L</sub> =16.7Ω, R <sub>GEN</sub> =3Ω		6		ns
t <sub>r</sub>	Turn-On Rise Time			2.5		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			21		ns
t <sub>f</sub>	Turn-Off Fall Time			2.4		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =3A, dI/dt=500A/μs	14	21	28	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =3A, dI/dt=500A/μs	65	94	123	nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

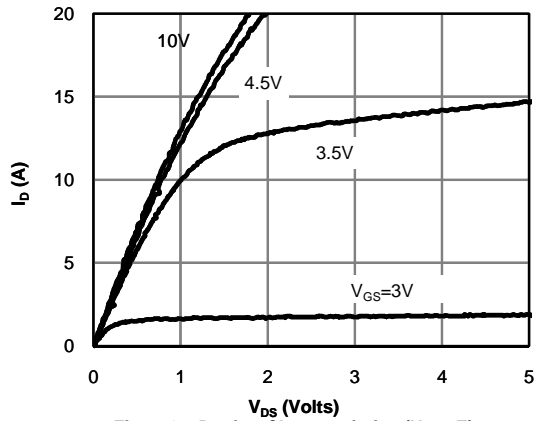


Figure 1: On-Region Characteristics (Note E)

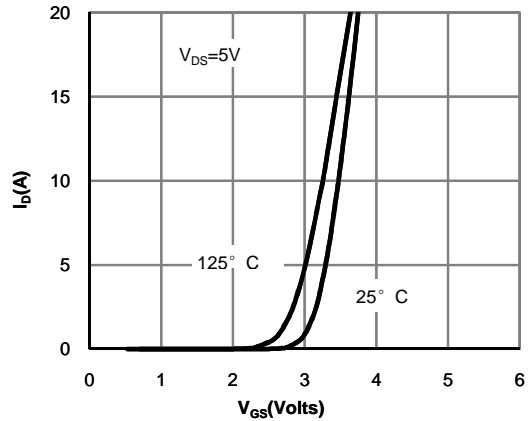


Figure 2: Transfer Characteristics (Note E)

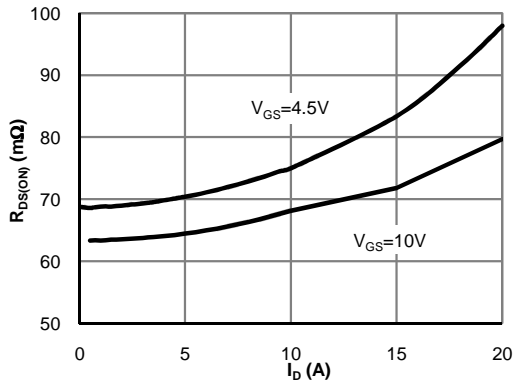


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

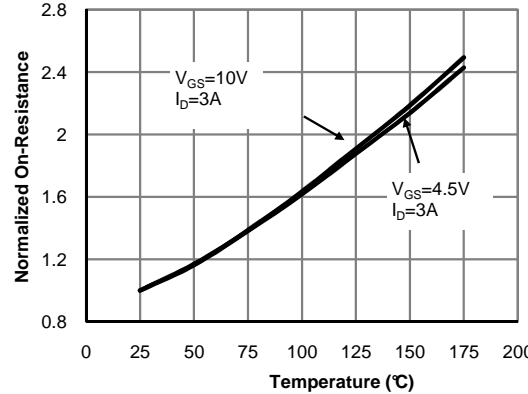


Figure 4: On-Resistance vs. Junction Temperature (Note E)

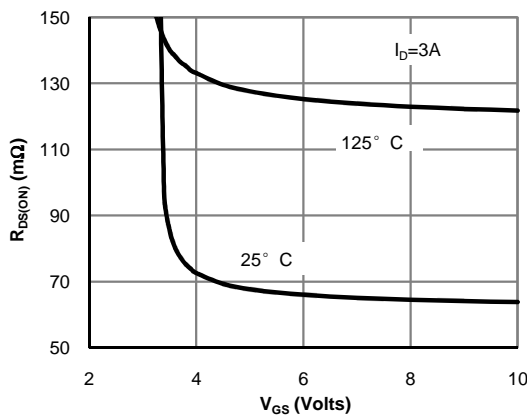


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

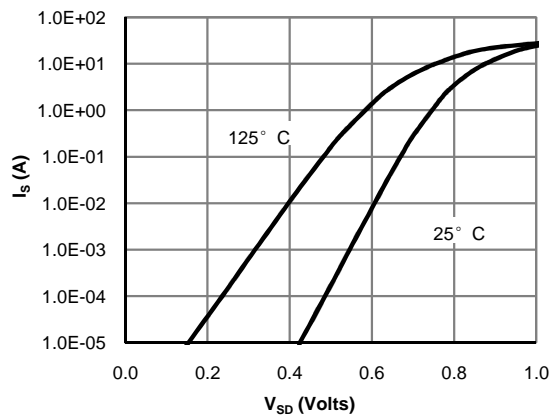
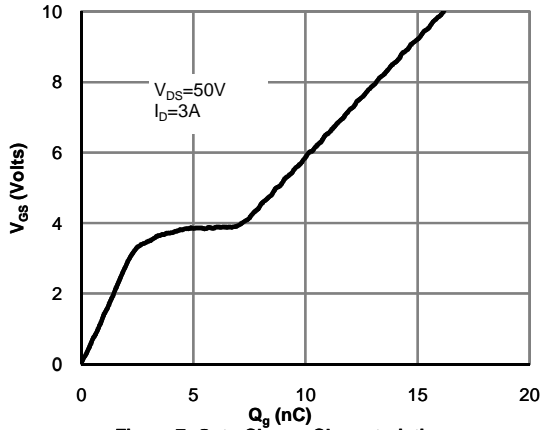
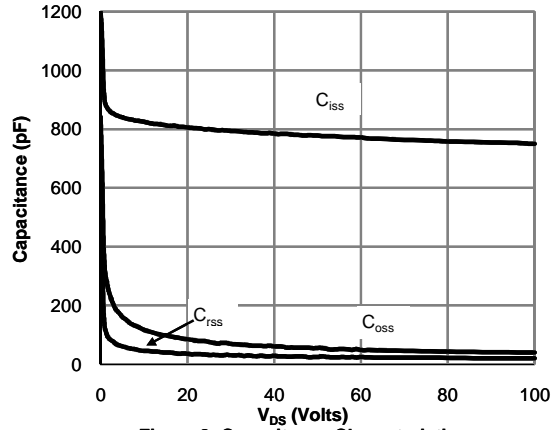


Figure 6: Body-Diode Characteristics (Note E)

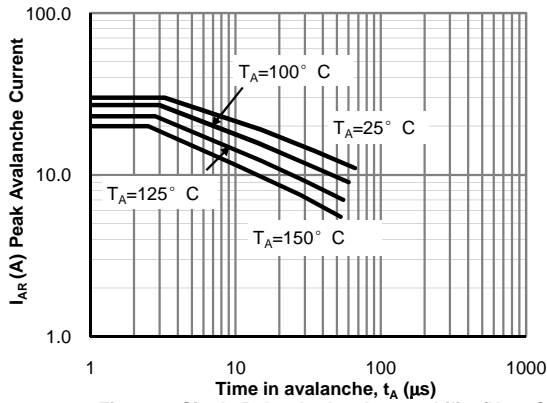
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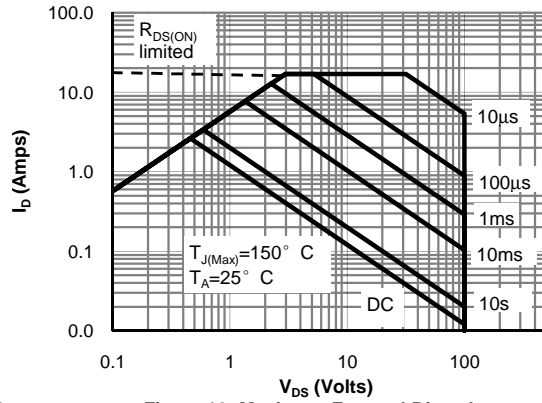
**Figure 7: Gate-Charge Characteristics**



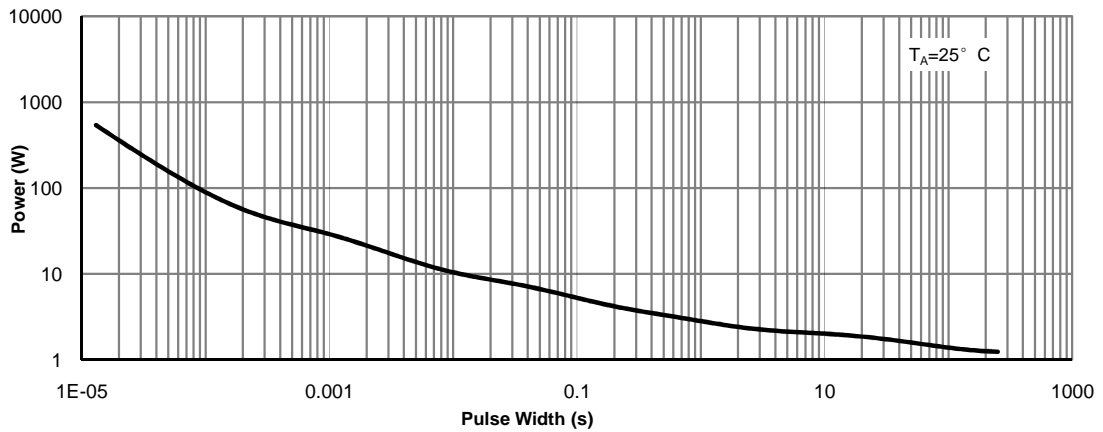
**Figure 8: Capacitance Characteristics**



**Figure 9: Single Pulse Avalanche capability (Note C)**



**Figure 10: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)**

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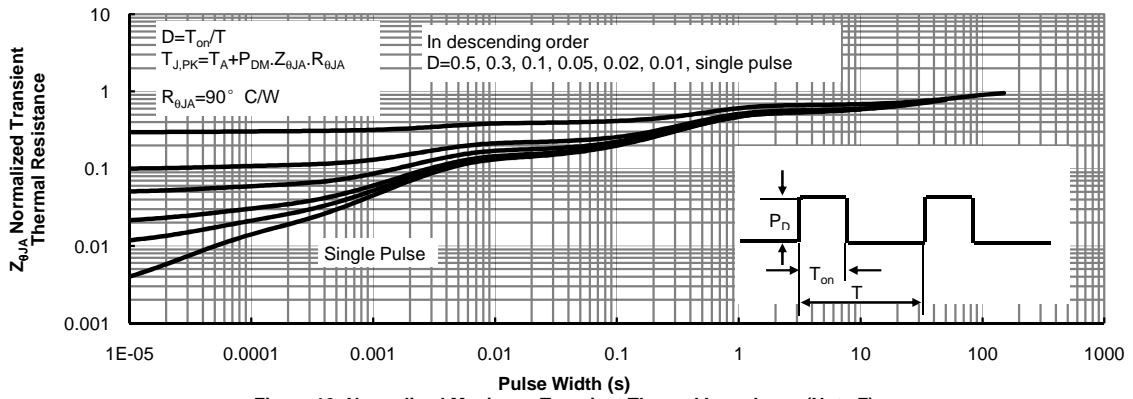
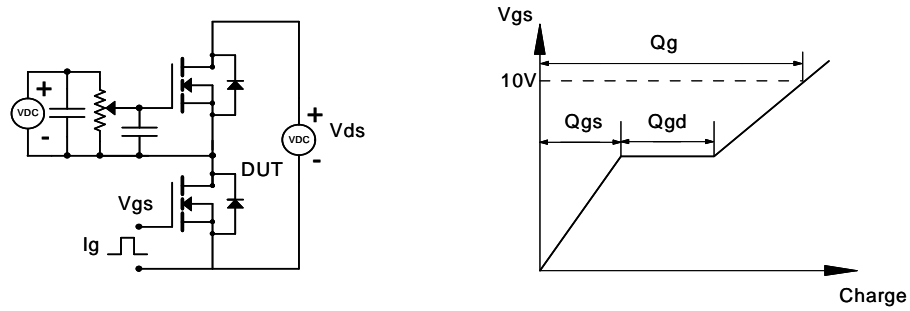


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

**Gate Charge Test Circuit & Waveform**



**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**

