

Dual N-Channel MOSFET

AO4912 (KO4912)

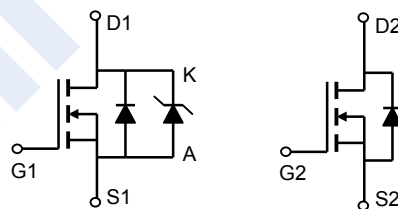
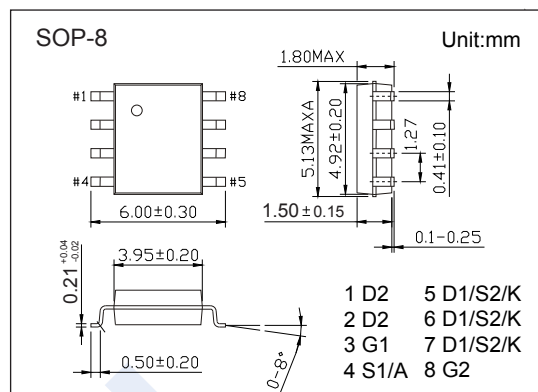
■ Features

N-Channel 1

- $V_{DS} (V) = 30V$
- $I_D = 8.5 A$ ($V_{GS} = 10V$)
- $R_{DS(ON)} < 17m\Omega$ ($V_{GS} = 10V$)
- $R_{DS(ON)} < 25m\Omega$ ($V_{GS} = 4.5V$)
- $V_{DS} (V) = 30V$, $I_F = 3A$, $V_F < 0.5V@1A$

N-Channel 2

- $V_{DS} (V) = 30V$
- $I_D = 7 A$ ($V_{GS} = 10V$)
- $R_{DS(ON)} < 26m\Omega$ ($V_{GS} = 10V$)
- $R_{DS(ON)} < 31m\Omega$ ($V_{GS} = 4.5V$)

■ Absolute Maximum Ratings $T_a = 25^\circ C$

Parameter		Symbol	N-Channel 1	Schottky	N-Channel 2	Unit
Drain-Source Voltage		V _{DS}	30		30	V
Gate-Source Voltage		V _{GS}	± 20		± 12	
Schottky Reverse Voltage		V _{KA}		30		
Continuous Drain Current	T _A =25°C	I _D	8.5		7	A
	T _A =70°C		6.8		6.4	
Pulsed Drain Current		I _{DM}	40		30	
Continuous Forward Current	T _A =25°C	I _F		3		A
	T _A =70°C			2.2		
Pulsed Diode Forward Current		I _{FM}		20		
Avalanche Current		I _{AR}	17		15	
Repetitive Avalanche Energy	L=0.3mH	E _{AR}	43		34	mJ
Power Dissipation	T _A =25°C	P _D	2			W
	T _A =70°C		1.28			
Thermal Resistance.Junction- to-Ambient	t ≤ 10s	R _{thJA}	62.5			°C/W
	Steady-State		110			
Thermal Resistance.Junction- to-Lead		R _{thJL}	40			
Junction Temperature		T _J	150			°C
Storage Temperature Range		T _{stg}	-55 to 150			

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■ N-Channel 1 Electrical Characteristics Ta = 25°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V _{DSS}	I _D =250 μA, V _{GS} =0V	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			0.05	mA
		V _{DS} =30V, V _{GS} =0V, T _J =125°C			10	
		V _{DS} =30V, V _{GS} =0V, T _J =150°C			20	
Gate-Body Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250 μA	1		3	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =8.5A			17	mΩ
		V _{GS} =10V, I _D =8.5A, T _J =125°C			24	
		V _{GS} =4.5V, I _D =7A			25	
On State Drain Current	I _{D(on)}	V _{GS} =4.5V, V _{DS} =5V	30			A
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =8.5A		23		S
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =15V, f=1MHz		971	1165	pF
Output Capacitance (FET + Schottky)	C _{oss}			190		
Reverse Transfer Capacitance	C _{rss}			110	154	
Gate Resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.35		0.85	Ω
Total Gate Charge (10V)	Q _g	V _{GS} =10V, V _{DS} =15V, I _D =8.5A		19.2	23	nC
Total Gate Charge (4.5V)				9.36	11.2	
Gate Source Charge				2.6		
Gate Drain Charge				4.2		
Turn-On DelayTime	t _{d(on)}	V _{GS} =10V, V _{DS} =15V, R _L =1.8Ω, R _{GEN} =3Ω		5.2	7.5	ns
Turn-On Rise Time	t _r			4.4	6.5	
Turn-Off DelayTime	t _{d(off)}			17.3	25	
Turn-Off Fall Time	t _f			3.3	5	
Body Diode Reverse Recovery Time	t _{rr}	I _F =8.5A, di/dt=100A/us		19.3	23	nC
Body Diode Reverse Recovery Charge	Q _{rr}			9.4	11	
Body-Diode + Schottky Continuous Current	I _S				3.5	A
Diode + Schottky Forward Voltage	V _{SD}	I _S =1A, V _{GS} =0V			0.5	V

Note. The static characteristics in Figures 1 to 6 are obtained using 300 μs pulses, duty cycle 0.5% max.

■ Marking

Marking	4912 KA****
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■ N-Channel 2 Electrical Characteristics Ta = 25°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V _{DSS}	I _D =250 μA, V _{GS} =0V	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
		V _{DS} =30V, V _{GS} =0V, T _J =55°C			5	
Gate-Body Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±12V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250 μA	1		2	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =7A			26	mΩ
		V _{GS} =10V, I _D =7A, T _J =125°C			38	
		V _{GS} =4.5V, I _D =6A			31	
On State Drain Current	I _{D(on)}	V _{GS} =4.5V, V _{DS} =5V	25			A
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =7A		22		S
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =15V, f=1MHz		590	710	pF
Output Capacitance	C _{oss}			162		
Reverse Transfer Capacitance	C _{rss}			40	56	
Gate Resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.2		0.6	Ω
Total Gate Charge	Q _g	V _{GS} =4.5V, V _{DS} =15V, I _D =7A		6.04	7.3	nC
Gate Source Charge	Q _{gs}			1.46		
Gate Drain Charge	Q _{gd}			2.56		
Turn-On DelayTime	t _{d(on)}	V _{GS} =10V, V _{DS} =15V, R _L =2.2Ω, R _{GEN} =3Ω		3.7	5.5	ns
Turn-On Rise Time	t _r			3.5	5.5	
Turn-Off DelayTime	t _{d(off)}			14.9	22	
Turn-Off Fall Time	t _f			2.5	4	
Body Diode Reverse Recovery Time	t _{rr}	I _F =7A, di/dt=100A/μs		21.2	26	nC
Body Diode Reverse Recovery Charge	Q _{rr}			14.2	21	
Body-Diode + Schottky Continuous Current	I _S				3	A
Diode Forward Voltage	V _{SD}	I _S =1A, V _{GS} =0V			1	V

Note. The static characteristics in Figures 1 to 6 are obtained using 300 μs pulses, duty cycle 0.5% max.

Dual N-Channel MOSFET

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■ N-Channel 1 Typical Characteristics

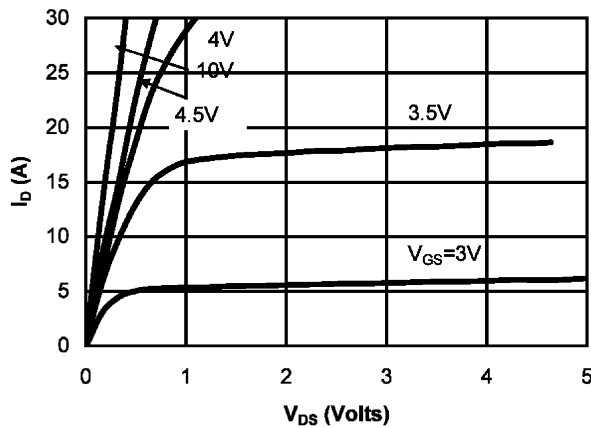


Fig 1: On-Region Characteristics

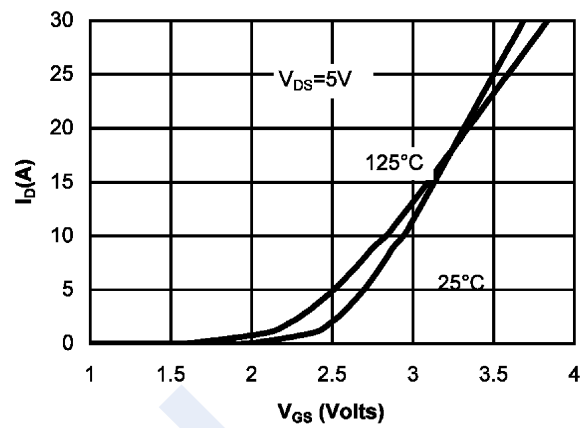


Figure 2: Transfer Characteristics

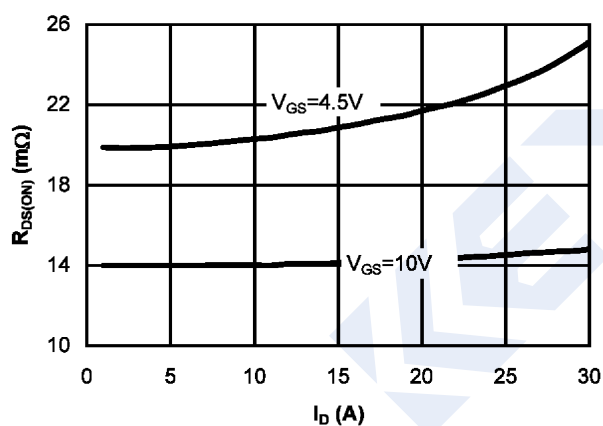


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

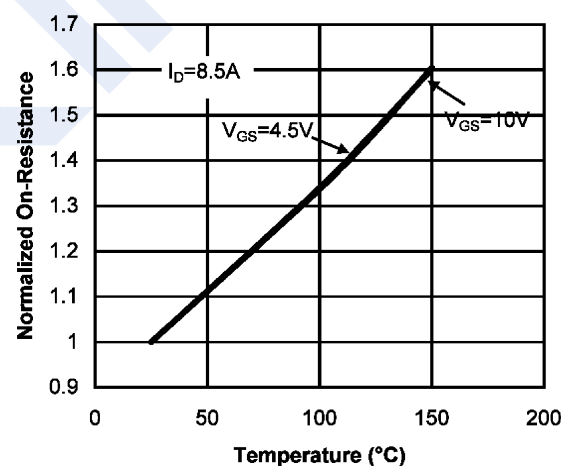


Figure 4: On resistance vs. Junction Temperature

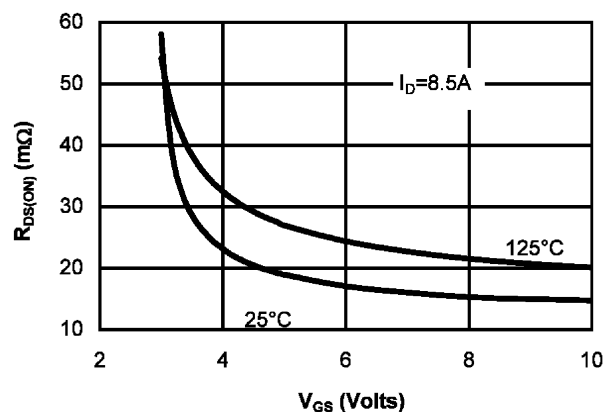
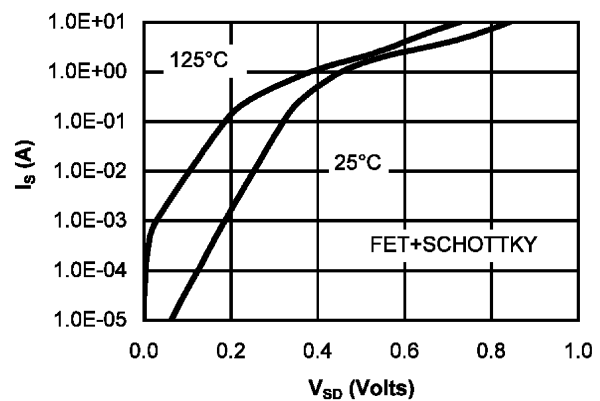


Figure 5: On resistance vs. Gate-Source Voltage

Figure 6: Body-Diode Characteristics
(Note F)

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■ N-Channel 1 Typical Characteristics

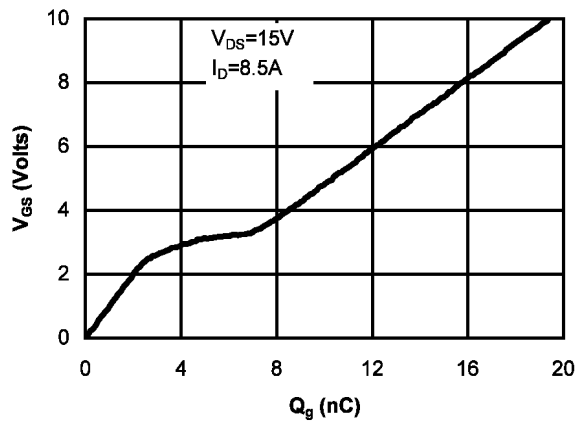


Figure 7: Gate-Charge Characteristics

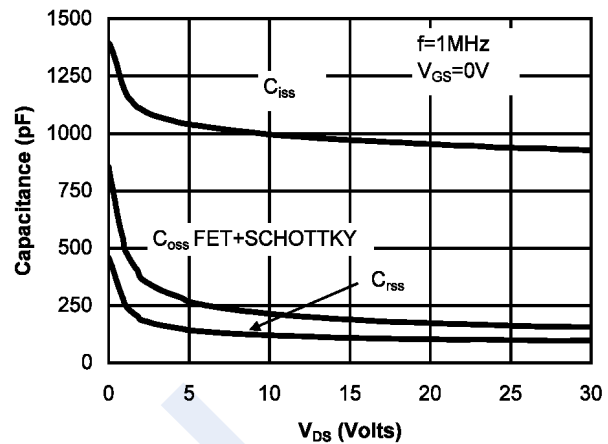


Figure 8: Capacitance Characteristics

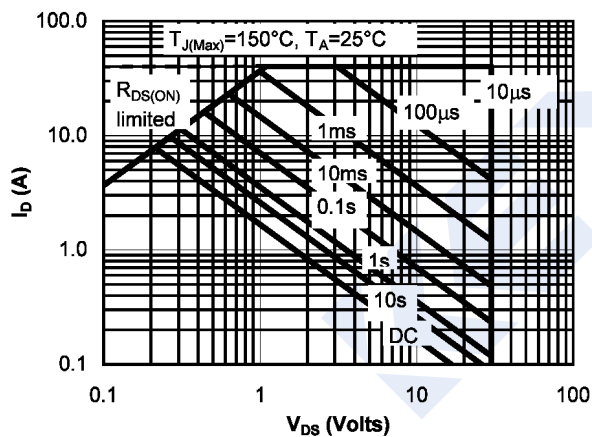


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

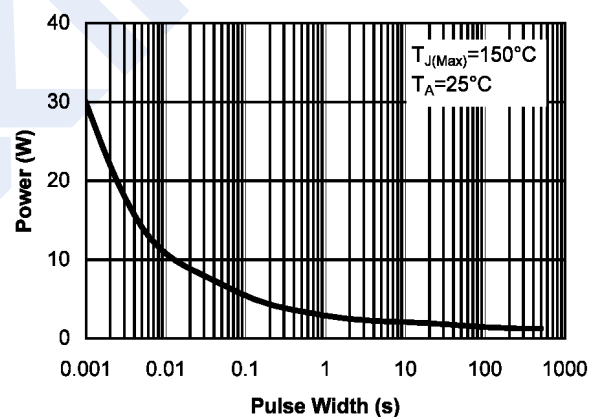


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

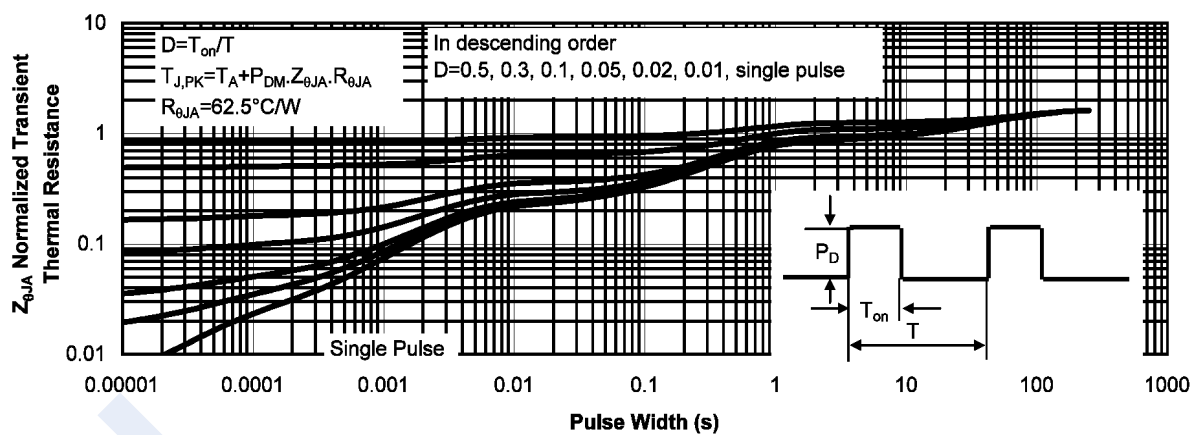


Figure 11: Normalized Maximum Transient Thermal Impedance

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■ N-Channel 2 Typical Characteristics

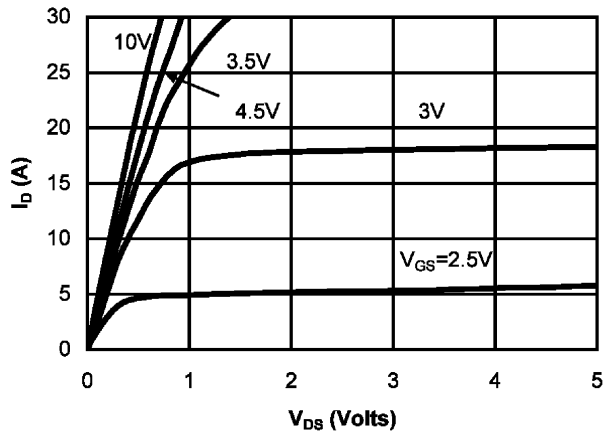


Fig 1: On-Region Characteristics

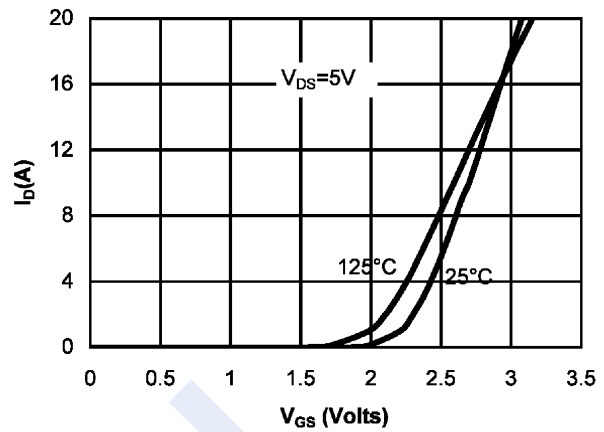


Figure 2: Transfer Characteristics

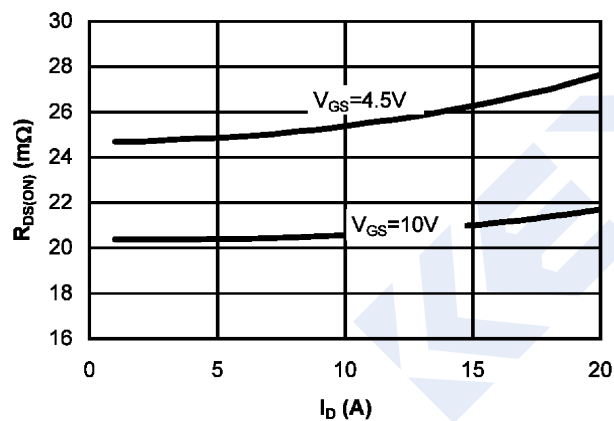


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

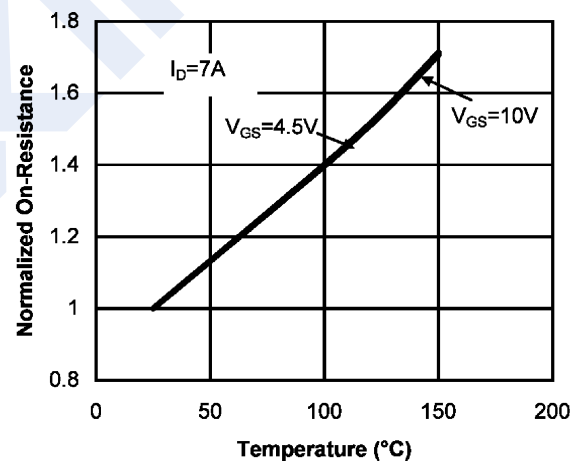


Figure 4: On resistance vs. Junction Temperature

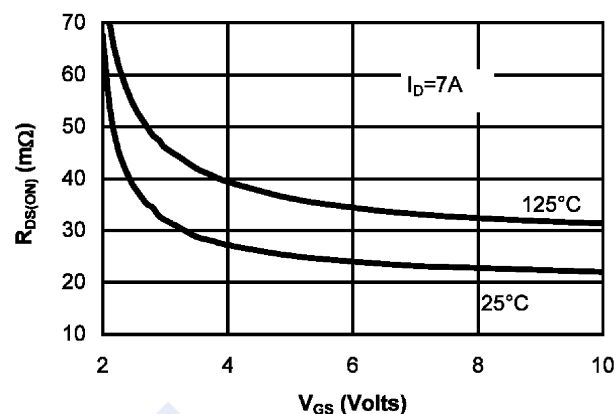


Figure 5: On resistance vs. Gate-Source Voltage

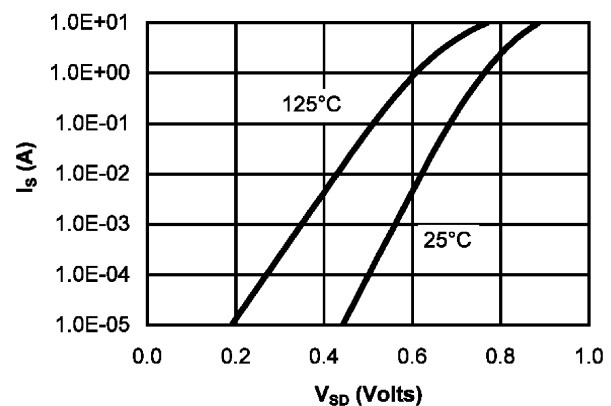


Figure 6: Body-Diode Characteristics

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■ N-Channel 2 Typical Characteristics

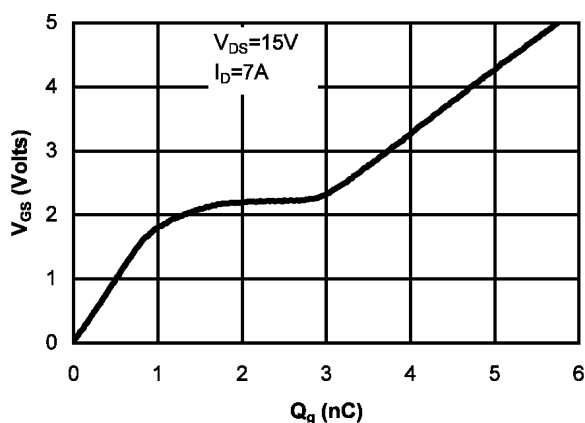


Figure 7: Gate-Charge Characteristics

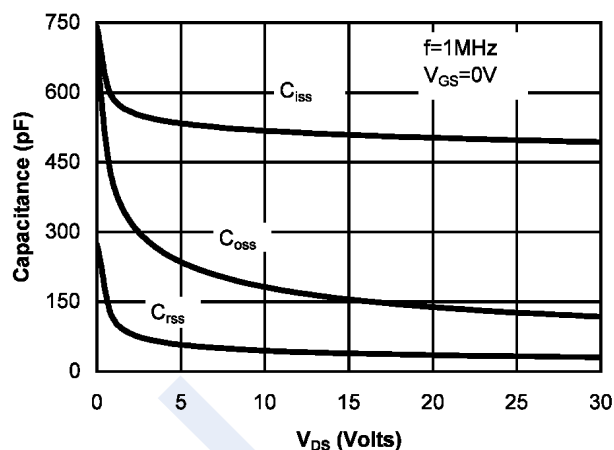


Figure 8: Capacitance Characteristics

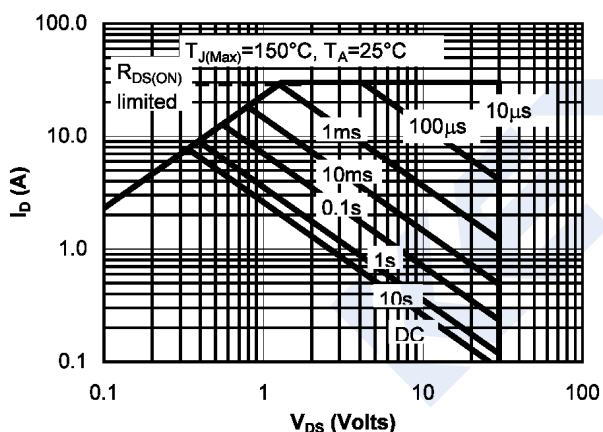


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

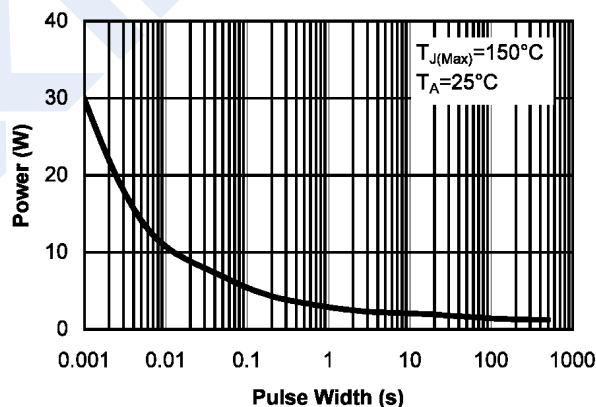


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

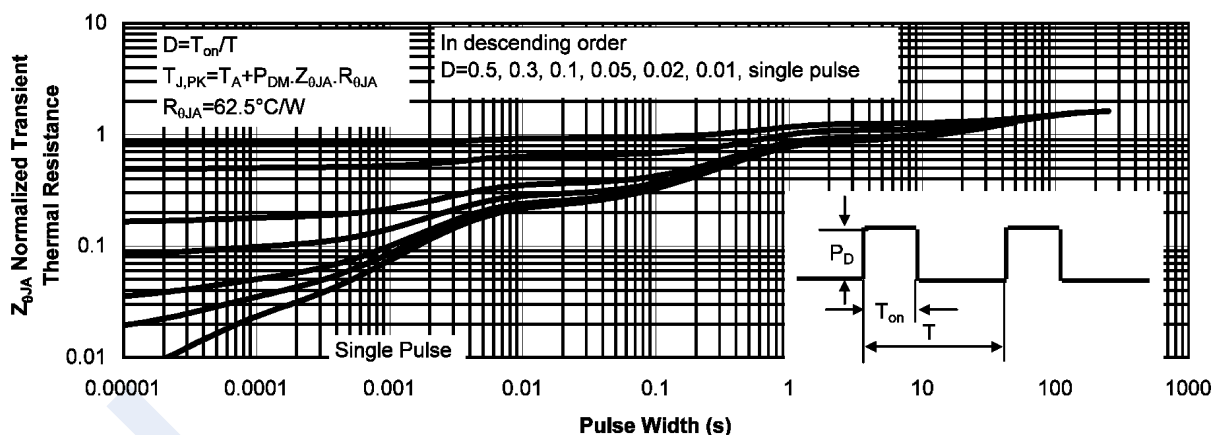


Figure 11: Normalized Maximum Transient Thermal Impedance