AO6402A

30V N-Channel MOSFET

General Description

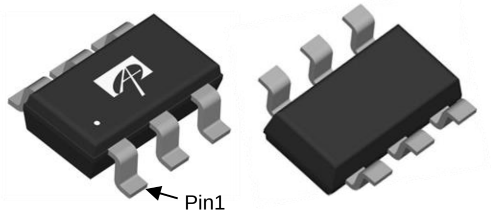
The AO6402A uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications. The source leads are separated to allow a Kelvin connection to the source, which may be used to bypass the source inductance.

Product Summary

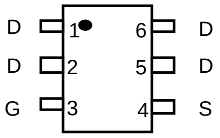
V_{DS} (V) = 30V
I_D = 7.5A (${V_{GS}}$ = 10V)
$R_{DS(ON)} < 24m\Omega$ (V_{GS} = 10V)
$R_{DS(ON)} < 35m\Omega$ (V_{GS} = 4.5V)

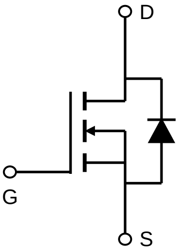
TSOP6

Top View **Bottom View**



Top View





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current ^{A,F}	T_A=25°C	I_D	7.5	A
	T_A=70°C		6.0	
Pulsed Drain Current ^{B}		I_{DM}	64	
Power Dissipation	T_A=25°C	P_D	2.0	W
	T_A=70°C		1.28	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^{A}	t ≤ 10s	$R_{\theta JA}$	48	62.5	°C/W
Maximum Junction-to-Ambient ^{A}	Steady-State		74	110	°C/W
Maximum Junction-to-Lead ^{C}	Steady-State	$R_{\theta JL}$	54	68	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250μA	1.5	2.1	2.6	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	64			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=7.5A		17.3	24	mΩ
		T_J=125°C		25	34	
		V_{GS}=4.5V, I_D=5.6A		25	35	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=7.5A		20		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.75	1	V
I_S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		373	448	pF
C_{oss}	Output Capacitance			67		pF
C_{rss}	Reverse Transfer Capacitance			41		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		2	2.8	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=7.5A		7.2	11	nC
Q_g(4.5V)	Total Gate Charge			3.5	5	nC
Q_{gs}	Gate Source Charge			1.3		nC
Q_{gd}	Gate Drain Charge			1.7		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=2Ω, R_{GEN}=3Ω		4.5	6.5	ns
t_r	Turn-On Rise Time			2.7	4.5	ns
$t_{D(off)}$	Turn-Off DelayTime			14.9	23	ns
t_f	Turn-Off Fall Time			2.9	5.5	ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=7.5A, dI/dt=100A/μs		10.5	12.6	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=7.5A, dI/dt=100A/μs		4.5	5.4	nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on $1in^2$ FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leqslant 10s$ thermal resistance rating.
B: Repetitive rating, pulse width limited by junction temperature.
C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
D. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.
E. These tests are performed with the device mounted on $1 in^2$ FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The SOA curve provides a single pulse rating.
F.The current rating is based on the $t \leqslant 10s$ thermal resistance rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

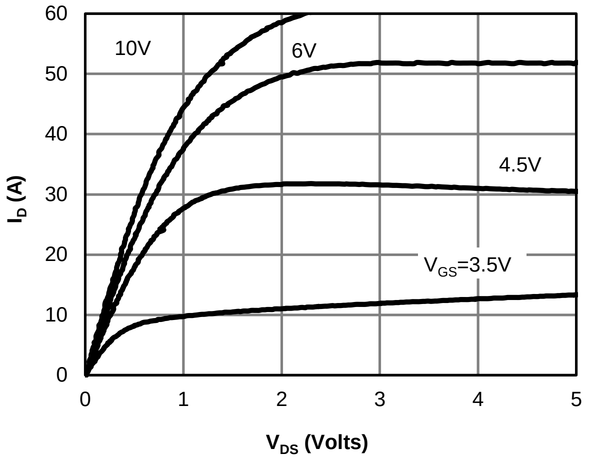


Fig 1: On-Region Characteristics

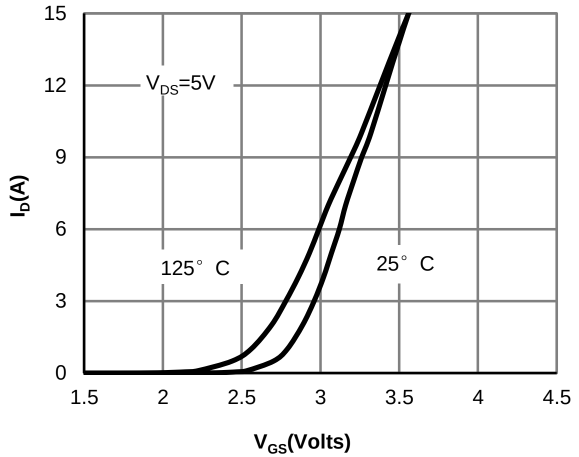


Figure 2: Transfer Characteristics

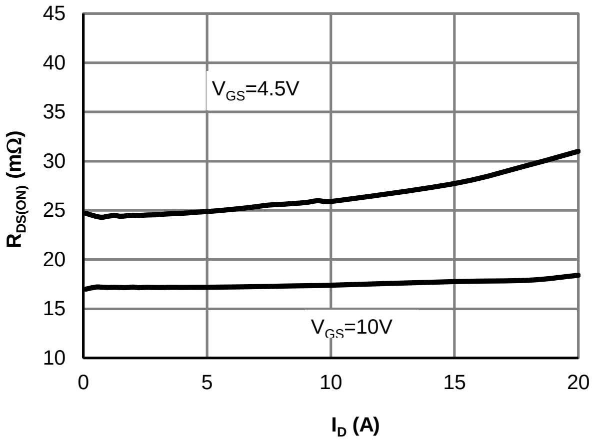


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

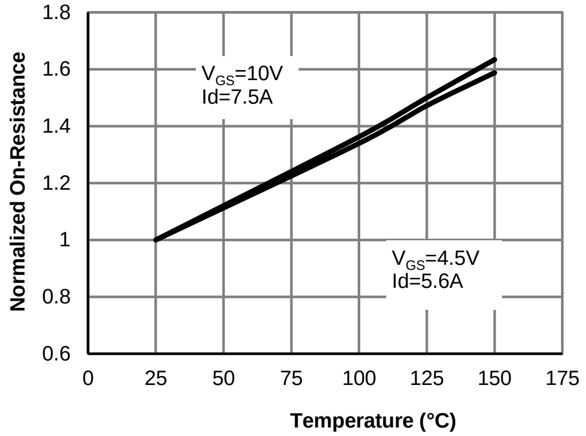


Figure 4: On-Resistance vs. Junction Temperature

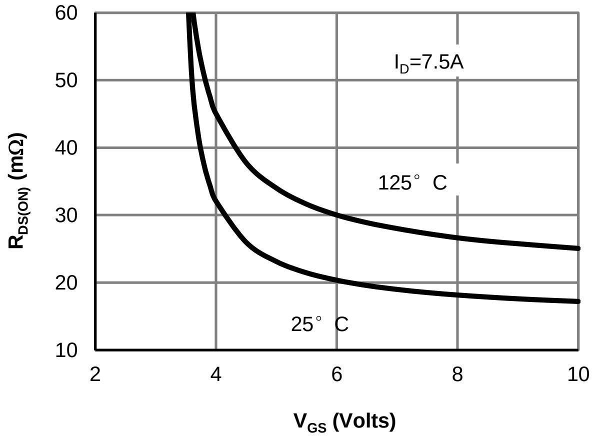


Figure 5: On-Resistance vs. Gate-Source Voltage

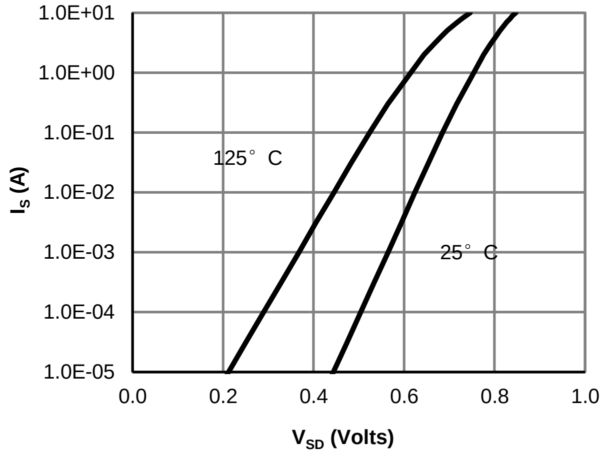


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

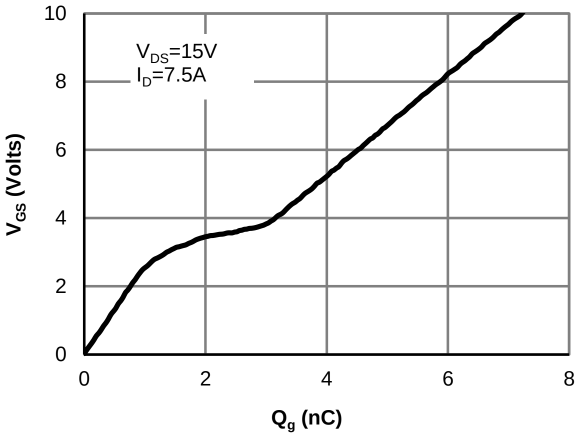


Figure 7: Gate-Charge Characteristics

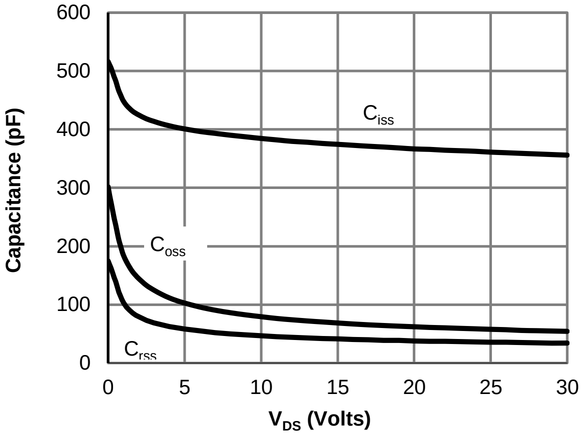


Figure 8: Capacitance Characteristics

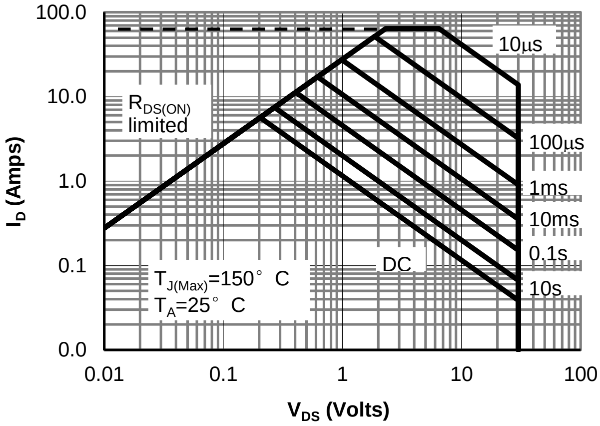


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

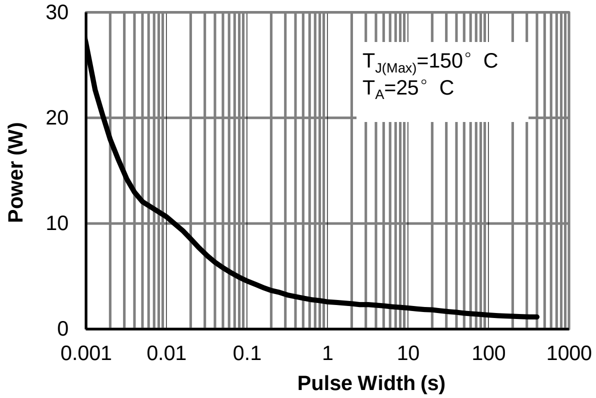


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

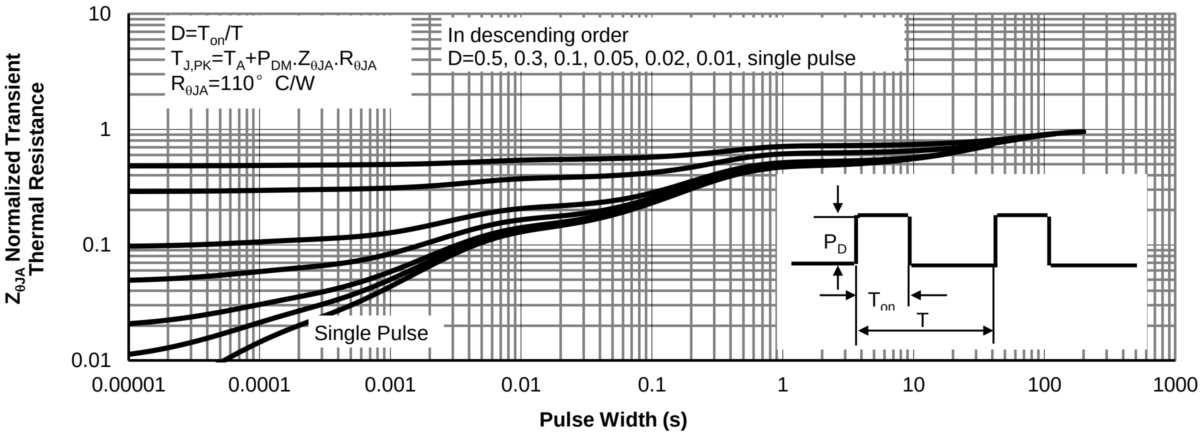
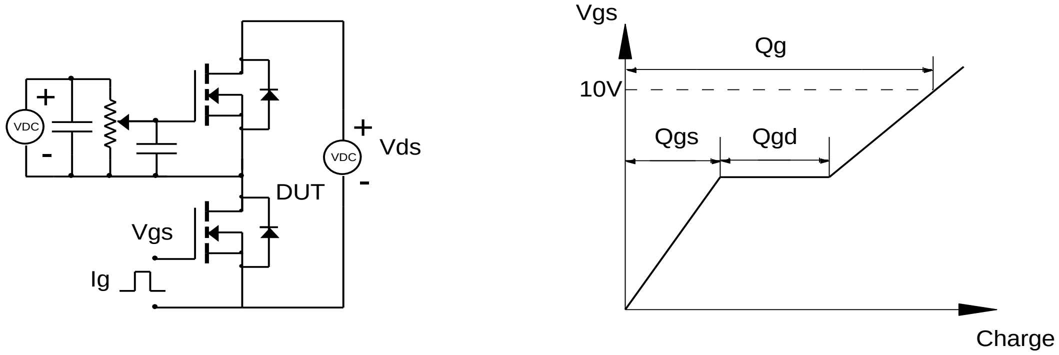
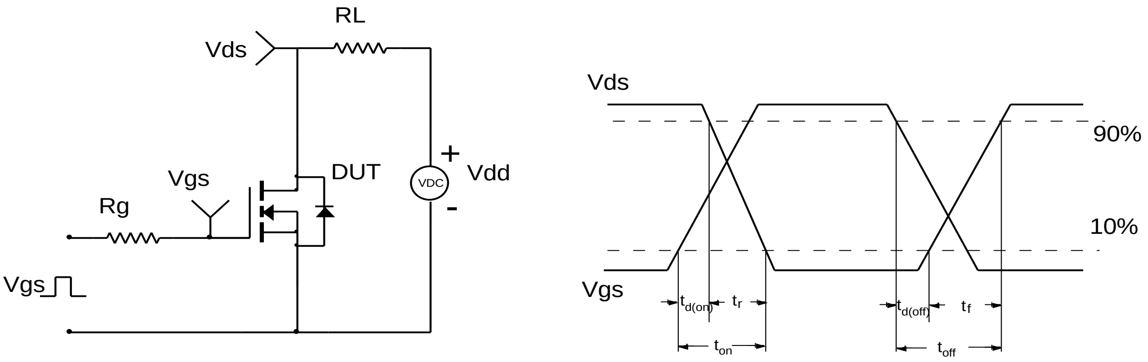


Figure 11: Normalized Maximum Transient Thermal Impedance

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms