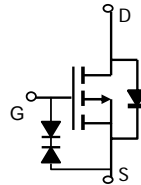
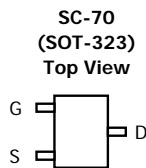



AO7403
P-Channel Enhancement Mode Field Effect Transistor
General Description

The AO7403 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge, and operation with gate voltages as low as 1.8V, in the small SOT323 footprint. It can be used for a wide variety of applications, including load switching, low current inverters and low current DC-DC converters. It is ESD protected to 2KV HBM. *Standard Product AO7403 is Pb-free (meets ROHS & Sony 259 specifications). AO7403L is a Green Product ordering option. AO7403 and AO7403L are electrically identical.*

Features

$V_{DS} (V) = -20V$
 $I_D = -0.7A (V_{GS} = -4.5V)$
 $R_{DS(ON)} < 470m\Omega (V_{GS} = -4.5V)$
 $R_{DS(ON)} < 625m\Omega (V_{GS} = -2.5V)$
 $R_{DS(ON)} < 900m\Omega (V_{GS} = -1.8V)$


Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

| Parameter | Symbol | Maximum | Units |
|--|----------------|------------------|------------|
| Drain-Source Voltage | V_{DS} | -20 | V |
| Gate-Source Voltage | V_{GS} | ± 8 | V |
| Continuous Drain Current ^A | I_D | $T_A=25^\circ C$ | A |
| | | $T_A=70^\circ C$ | |
| Pulsed Drain Current ^B | I_{DM} | -3 | |
| Power Dissipation ^A | P_D | $T_A=25^\circ C$ | 0.35 |
| | | $T_A=70^\circ C$ | 0.22 |
| Junction and Storage Temperature Range | T_J, T_{STG} | -55 to 150 | $^\circ C$ |

Thermal Characteristics

| Parameter | Symbol | Typ | Max | Units |
|--|-----------------|--------------|-----|--------------|
| Maximum Junction-to-Ambient ^A | $R_{\theta JA}$ | $t \leq 10s$ | 300 | $^\circ C/W$ |
| Maximum Junction-to-Ambient ^A | | Steady-State | 350 | $^\circ C/W$ |
| Maximum Junction-to-Lead ^C | $R_{\theta JL}$ | 280 | 320 | $^\circ C/W$ |

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------|---------------------------------------|--|------|------------|------------|------------------|
| STATIC PARAMETERS | | | | | | |
| BV_{DSS} | Drain-Source Breakdown Voltage | $I_D=-250\mu\text{A}$, $V_{GS}=0\text{V}$ | -20 | | | V |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS}=-16\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$ | | | -1 -5 | μA |
| I_{GSS} | Gate-Body leakage current | $V_{DS}=0\text{V}$, $V_{GS}=\pm 8\text{V}$ | | | ± 10 | μA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$ | -0.5 | -0.6 | -0.9 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}=-4.5\text{V}$, $V_{DS}=-5\text{V}$ | -3 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}=-4.5\text{V}$, $I_D=-0.7\text{A}$ $T_J=125^\circ\text{C}$ | | 388 542 | 470 660 | $\text{m}\Omega$ |
| | | $V_{GS}=-2.5\text{V}$, $I_D=-0.6\text{A}$ | | 519 | 625 | $\text{m}\Omega$ |
| | | $V_{GS}=-1.8\text{V}$, $I_D=-0.5\text{A}$ | | 666 | 900 | $\text{m}\Omega$ |
| g_{FS} | Forward Transconductance | $V_{DS}=-5\text{V}$, $I_D=-0.7\text{A}$ | | 1.7 | | S |
| V_{SD} | Diode Forward Voltage | $I_S=-0.5\text{A}$, $V_{GS}=0\text{V}$ | | -0.86 | -1 | V |
| I_S | Maximum Body-Diode Continuous Current | | | | -0.4 | A |
| DYNAMIC PARAMETERS | | | | | | |
| C_{iss} | Input Capacitance | $V_{GS}=0\text{V}$, $V_{DS}=-10\text{V}$, $f=1\text{MHz}$ | | 114 | | pF |
| C_{oss} | Output Capacitance | | | 17 | | pF |
| C_{riss} | Reverse Transfer Capacitance | | | 14 | | pF |
| R_g | Gate resistance | $V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$ | | 12 | | Ω |
| SWITCHING PARAMETERS | | | | | | |
| Q_g | Total Gate Charge | $V_{GS}=-4.5\text{V}$, $V_{DS}=-10\text{V}$, $I_D=-0.7\text{A}$ | | 1.44 | | nC |
| Q_{gs} | Gate Source Charge | | | 0.14 | | nC |
| Q_{gd} | Gate Drain Charge | | | 0.35 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}=-4.5\text{V}$, $V_{DS}=-10\text{V}$, $R_L=14.3\Omega$, $R_{GEN}=3\Omega$ | | 6.5 | | ns |
| t_r | Turn-On Rise Time | | | 6.5 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 18.2 | | ns |
| t_f | Turn-Off Fall Time | | | 5.5 | | ns |
| t_{rr} | Body Diode Reverse Recovery Time | $I_F=-0.7\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$ | | 10 | | ns |
| Q_{rr} | Body Diode Reverse Recovery Charge | $I_F=-0.7\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$ | | 3 | | nC |

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D: The static characteristics in Figures 1 to 6, 12, 14 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

Rev4: Aug 2008

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

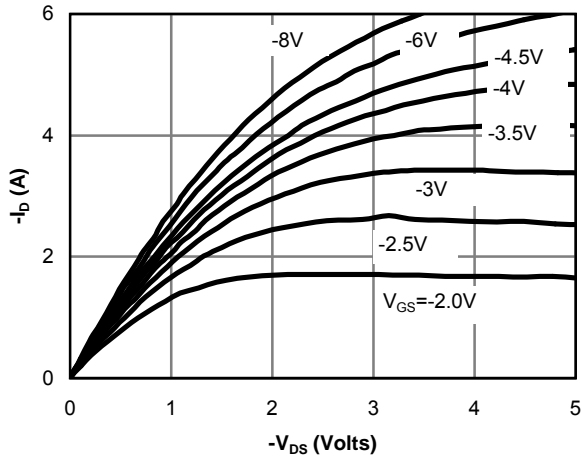


Fig 1: On-Region Characteristics

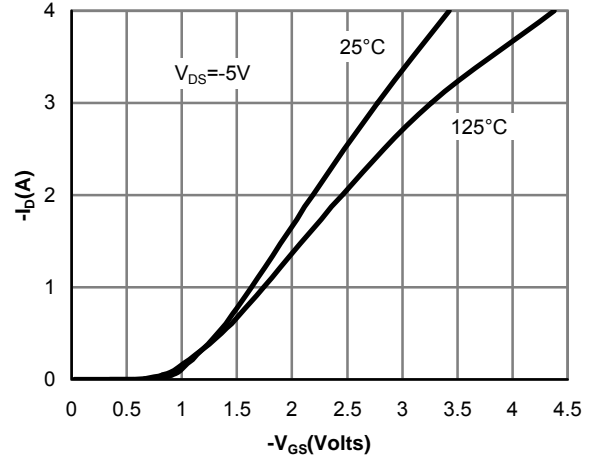


Figure 2: Transfer Characteristics

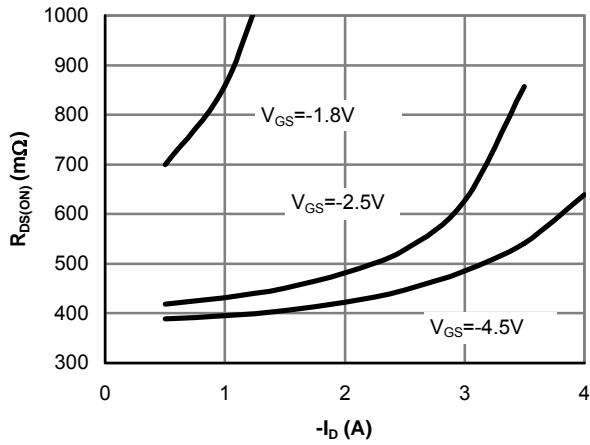


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

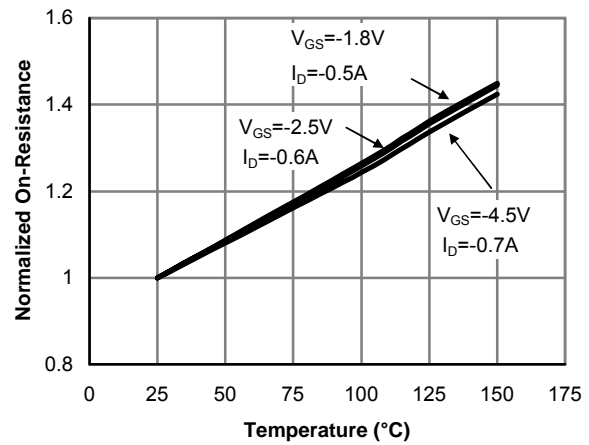


Figure 4: On-Resistance vs. Junction Temperature

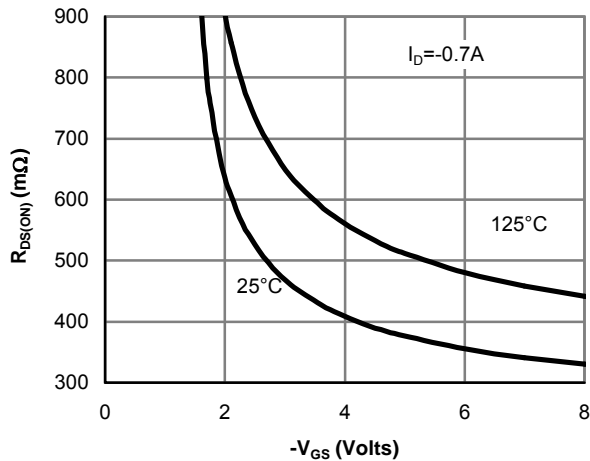


Figure 5: On-Resistance vs. Gate-Source Voltage

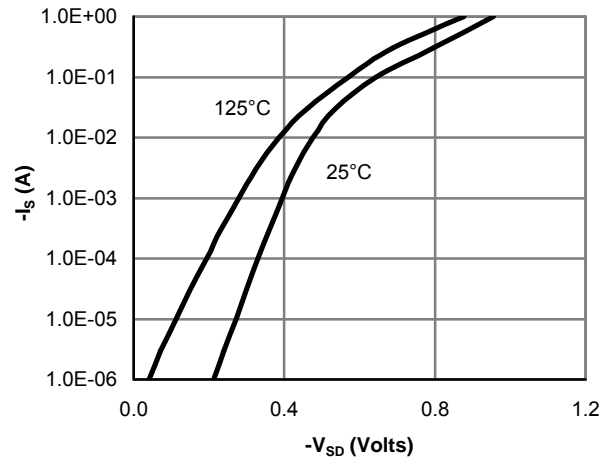


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

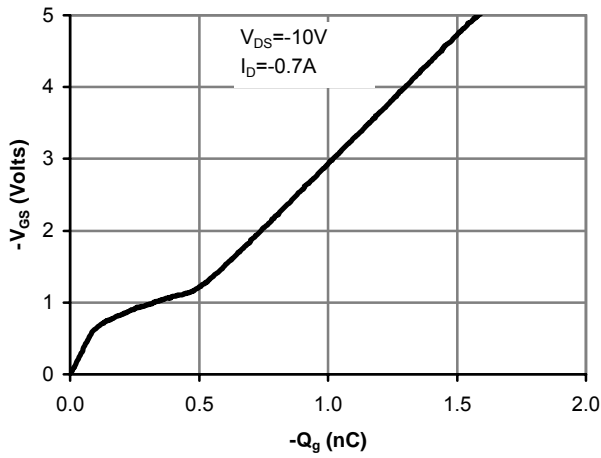


Figure 7: Gate-Charge Characteristics

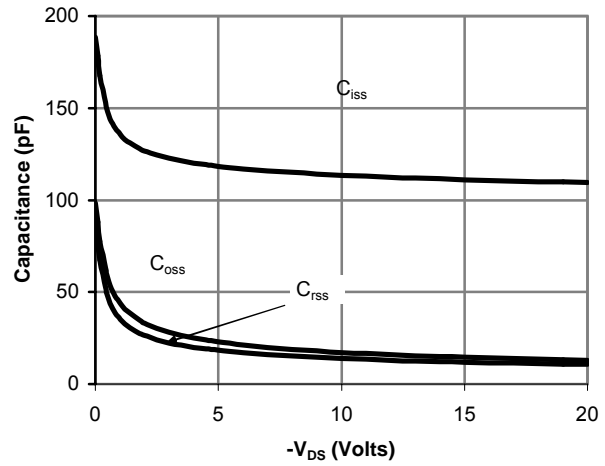


Figure 8: Capacitance Characteristics

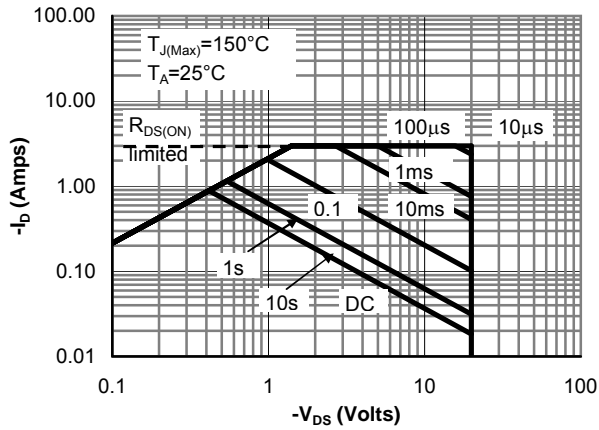


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

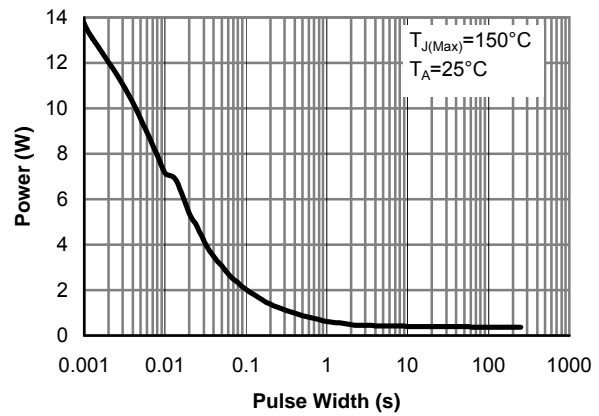


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

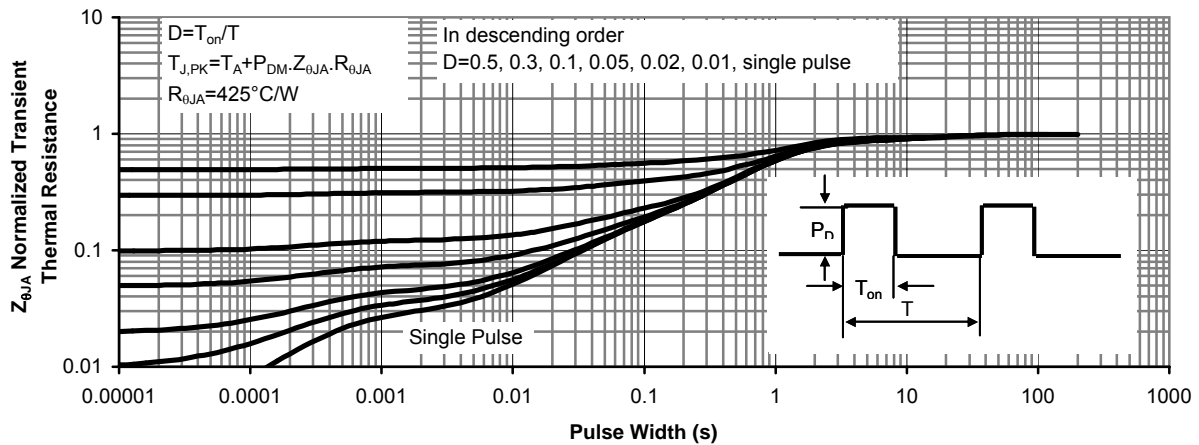


Figure 11: Normalized Maximum Transient Thermal Impedance