

AOD4104

N-Channel Enhancement Mode Field Effect Transistor

General Description

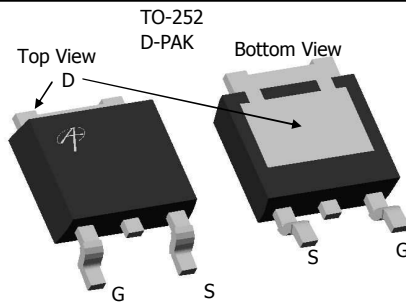
The AOD4104 uses advanced trench technology to provide excellent $R_{DS(ON)}$, shoot-through immunity and body diode characteristics. This device is ideally suited for use as a low side switch in CPU core power conversion.

- RoHS Compliant
- Halogen Free*

Features

$V_{DS} (V) = 25V$
 $I_D = 75A (V_{GS} = 10V)$
 $R_{DS(ON)} < 3.6m\Omega (V_{GS} = 20V)$
 $R_{DS(ON)} < 4.5m\Omega (V_{GS} = 12V)$
 $R_{DS(ON)} < 5.4m\Omega (V_{GS} = 10V)$

100% UIS Tested!
100% Rg Tested!



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	25	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current ^{B,G,I}	I_D	$T_C=25^\circ C$ ^G	75
		$T_C=100^\circ C$	75
Pulsed Drain Current ^C	I_{DM}	200	A
Avalanche Current ^C	I_{AR}	30	A
Repetitive avalanche energy $L=0.3mH$ ^C	E_{AR}	135	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ C$	100
		$T_C=100^\circ C$	50
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ C$	2.5
		$T_A=70^\circ C$	1.6
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	16	20	$^\circ C/W$
Maximum Junction-to-Ambient ^A		Steady-State	40	50
Maximum Junction-to-Case ^B	$R_{\theta JC}$	1	1.5	$^\circ C/W$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	25			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V T _J =55°C		0.005	1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±30V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2	3	4	V
I _{D(ON)}	On state drain current	V _{GS} =12V, V _{DS} =5V	200			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =20V, I _D =20A T _J =125°C		3 4.2	3.6 5	mΩ
		V _{GS} =12V, I _D =20A		3.7	4.5	
		V _{GS} =10V, I _D =20A		4.5	5.4	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		75		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current				55	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =12.5V, f=1MHz		2100	2400	pF
C _{oss}	Output Capacitance		850		pF	
C _{rss}	Reverse Transfer Capacitance		400		pF	
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		0.35	1	Ω
SWITCHING PARAMETERS						
Q _g (12V)	Total Gate Charge	V _{GS} =10V, V _{DS} =12.5V, I _D =20A		40	50	nC
Q _g (10V)	Total Gate Charge		33		nC	
Q _{gs}	Gate Source Charge		11		nC	
Q _{gd}	Gate Drain Charge		14		nC	
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =12.5V, R _L =0.68Ω, R _{GEN} =3Ω		12		ns
t _r	Turn-On Rise Time		19		ns	
t _{D(off)}	Turn-Off DelayTime		15		ns	
t _f	Turn-Off Fall Time		8.5		ns	
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, di/dt=100A/μs		42		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, di/dt=100A/μs		34		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C.

D: The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

I: The maximum current rating is limited by bond-wires.

*This device is guaranteed green after data code 8X11 (Sep 8th 2008).

Rev1:Oct 2008

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

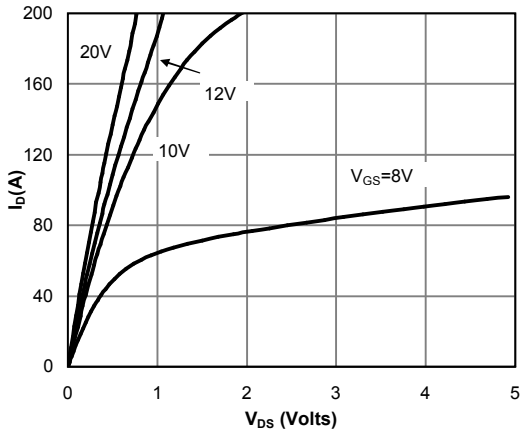


Figure 1: On-Region Characteristics

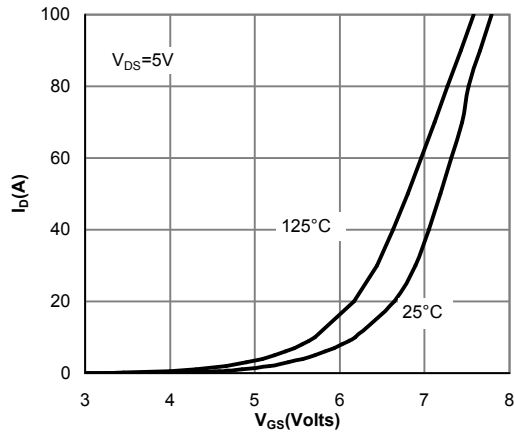


Figure 2: Transfer Characteristics

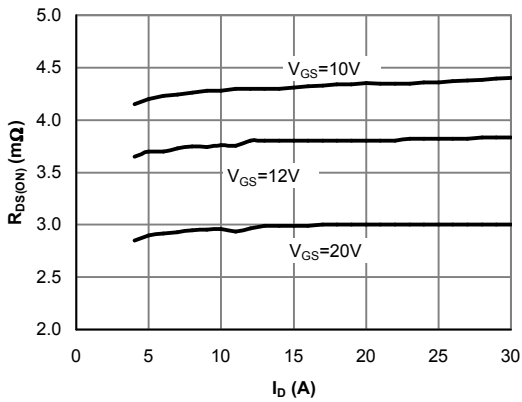


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

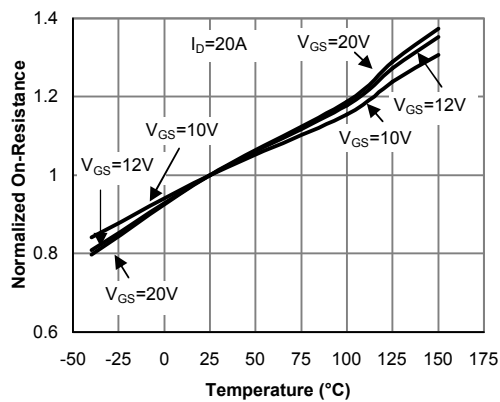


Figure 4: On-Resistance vs. Junction Temperature

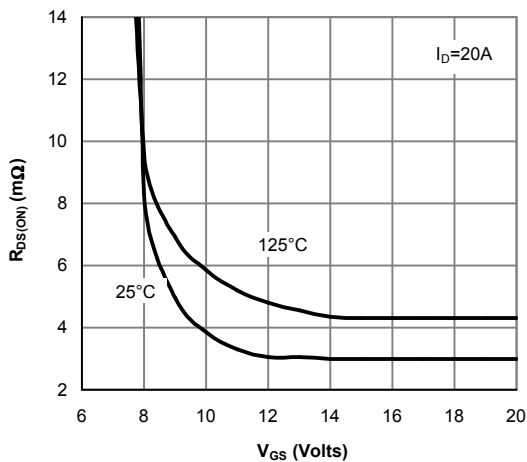


Figure 5: On-Resistance vs. Gate-Source Voltage

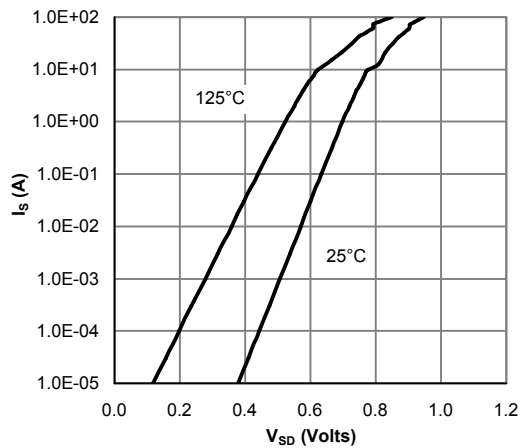


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

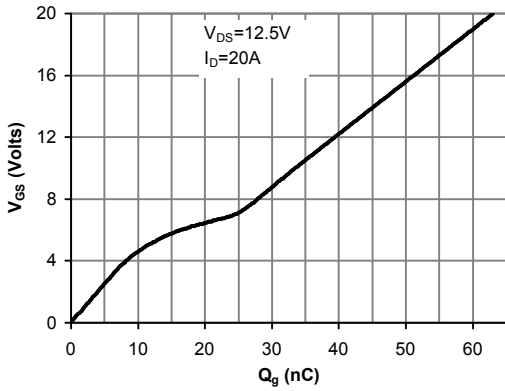


Figure 7: Gate-Charge Characteristics

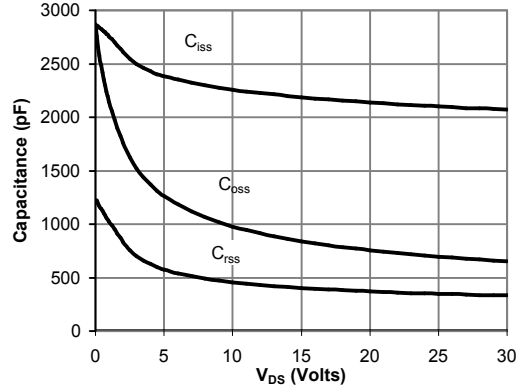


Figure 8: Capacitance Characteristics

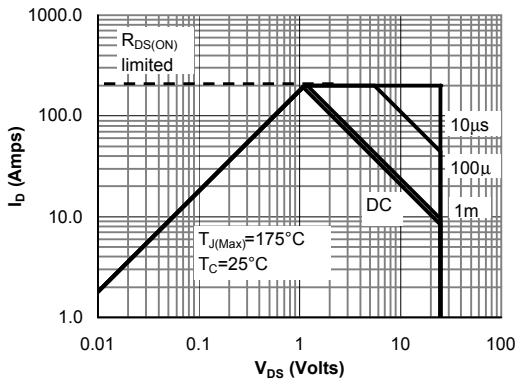


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

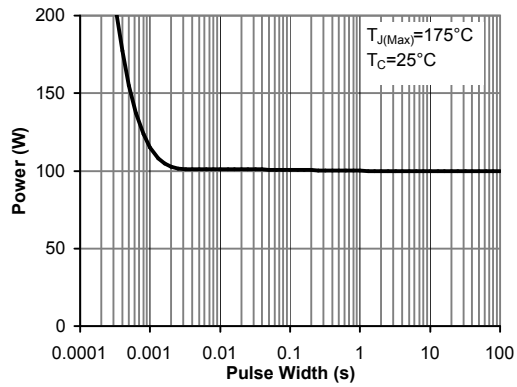


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

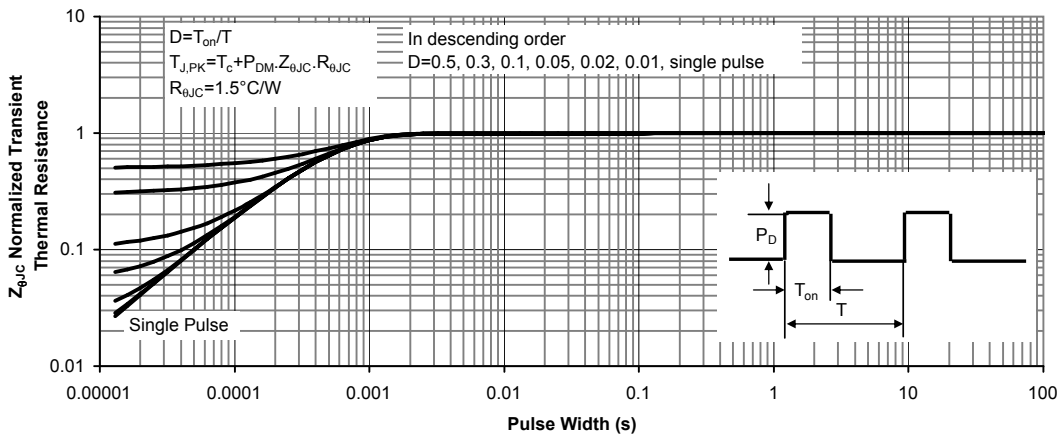


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

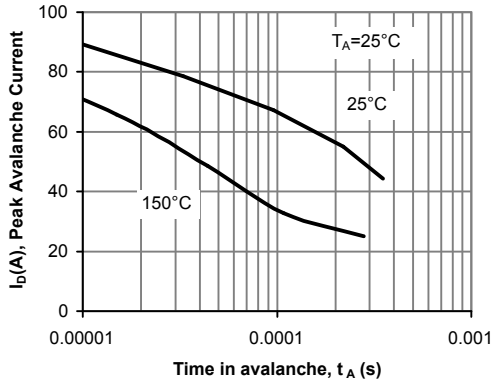


Figure 12: Single Pulse Avalanche capability

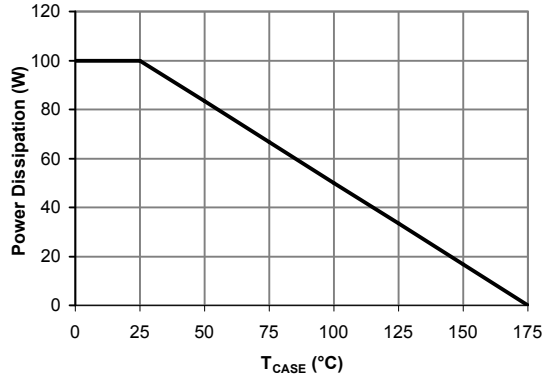


Figure 13: Power De-rating (Note B)

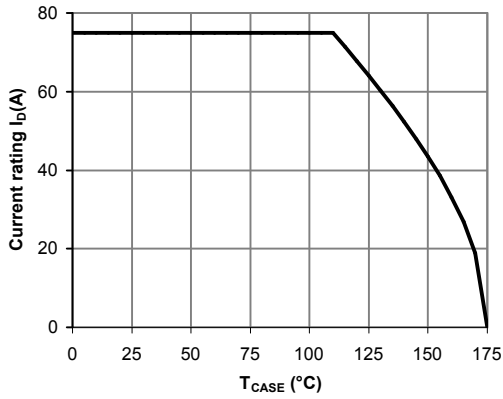


Figure 14: Current De-rating (Note B)

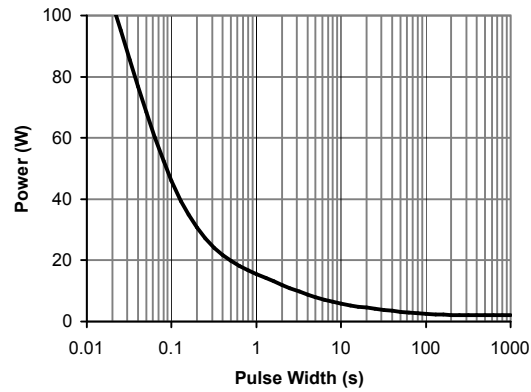


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

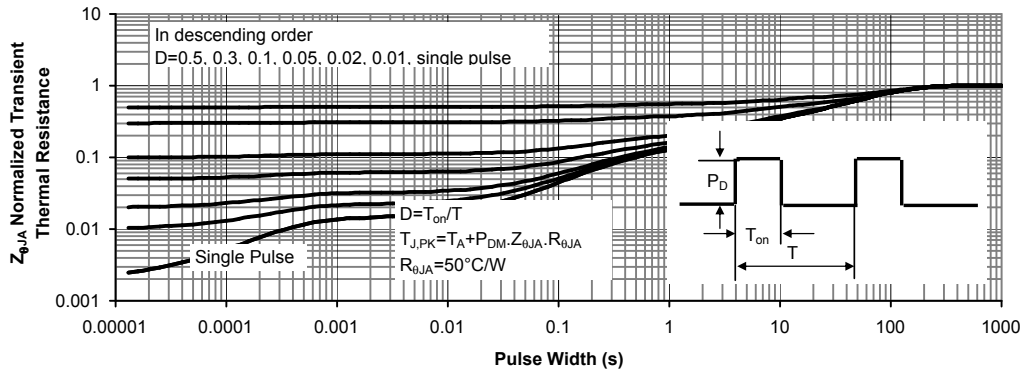
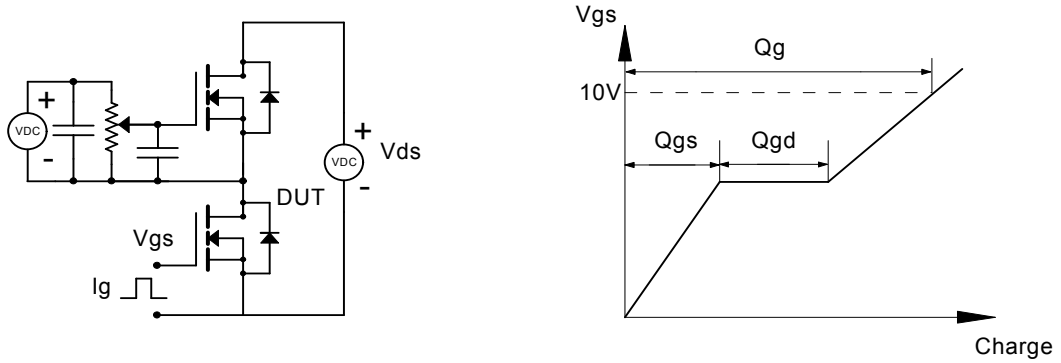
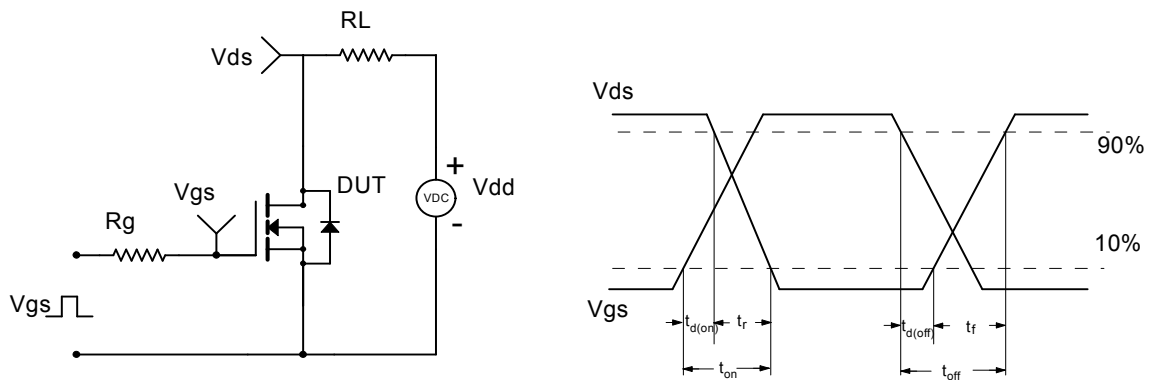


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

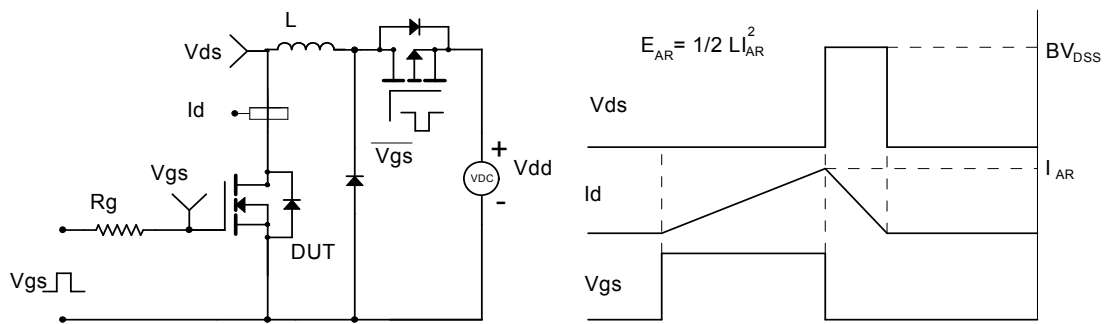
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

