

AOD4110
N-Channel Enhancement Mode Field Effect Transistor
SRFET™

General Description

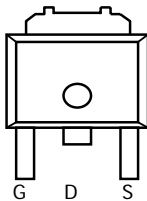
The AOD4110 uses advanced trench technology with a monolithically integrated Schottky diode to provide excellent $R_{DS(ON)}$, and low gate charge. This device is suitable for use as a low side FET in SMPS, load switching and general purpose applications. *Standard Product AOD4110 is Pb-free (meets ROHS & Sony 259 specifications).*

Features

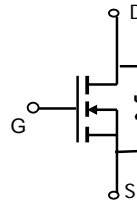
V_{DS} (V) = 30V
 $I_D = 40A$ ($V_{GS} = 10V$)
 $R_{DS(ON)} < 7.2m\Omega$ ($V_{GS} = 10V$)
 $R_{DS(ON)} < 10.5m\Omega$ ($V_{GS} = 4.5V$)

UIS Tested!
Rg, Ciss, Coss, Crss Tested

TO-252 D-PAK



Top View
Drain Connected to Tab



SRFET™
Soft Recovery MOSFET:
Integrated Schottky Diode

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^B	I_D	$T_C=25^\circ\text{C}^G$	A
		$T_C=100^\circ\text{C}^G$	
Pulsed Drain Current ^C	I_{DM}	180	
Continuous Drain Current ^A	I_{DSM}	$T_A=25^\circ\text{C}$	A
		$T_A=70^\circ\text{C}$	
Avalanche Current ^C	I_{AR}	25	A
Repetitive avalanche energy $L=0.3mH^C$	E_{AR}	94	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	W
		$T_C=100^\circ\text{C}$	
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10s$	15	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		Steady-State	41	$^\circ\text{C/W}$
Maximum Junction-to-Case ^D	$R_{\theta JC}$	2	2.4	$^\circ\text{C/W}$

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}$, $V_{GS}=0\text{V}$ $T_J=125^\circ\text{C}$			0.1 20	mA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			0.1	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.3	1.6	2	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	180			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=20\text{A}$ $T_J=125^\circ\text{C}$		6 9.0	7.2 11.0	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=20\text{A}$		8.5	10.5	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=20\text{A}$		55		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.37	0.5	V
I_S	Maximum Body-Diode + Schottky Continuous Current [†]				40	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance			2154	2650	pF
C_{oss}	Output Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=15\text{V}$, $f=1\text{MHz}$		474		pF
C_{rss}	Reverse Transfer Capacitance			185		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		0.75	1.1	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge			37	45	
$Q_g(4.5\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $I_D=20\text{A}$		17.8		nC
Q_{gs}	Gate Source Charge			6.6		nC
Q_{gd}	Gate Drain Charge			7.6		nC
$t_{D(on)}$	Turn-On DelayTime			6.8		ns
t_r	Turn-On Rise Time	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $R_L=0.75\Omega$, $R_{GEN}=3\Omega$		7.2		ns
$t_{D(off)}$	Turn-Off DelayTime			25.2		ns
t_f	Turn-Off Fall Time			5.8		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20\text{A}$, $dI/dt=300\text{A}/\mu\text{s}$		12	18	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}$, $dI/dt=300\text{A}/\mu\text{s}$		10.5		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The power dissipation P_{DSM} and current rating I_{DSM} are based on $T_{J(MAX)}=150^\circ\text{C}$, using $t \leq 10\text{s}$ junction-to-ambient thermal resistance. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation P_D is based on $T_{J(MAX)}=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^\circ\text{C}$.

D: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=175^\circ\text{C}$.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

Rev0: Apr.2007

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

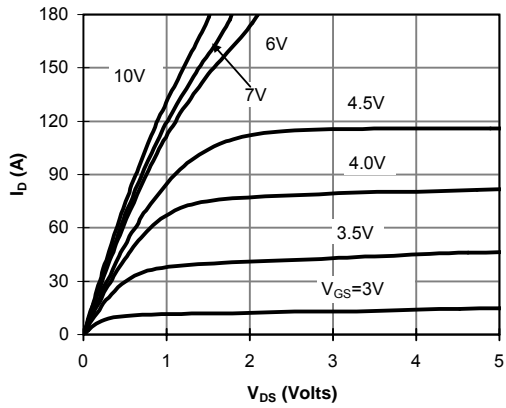


Figure 1: On-Region Characteristics

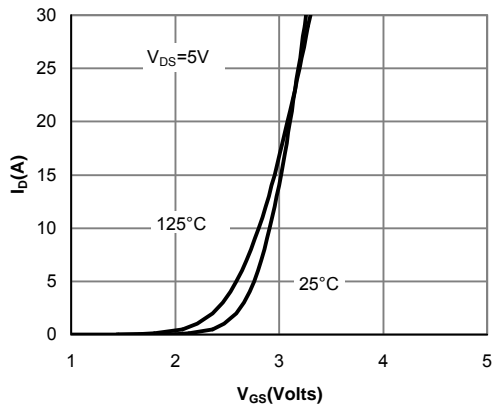


Figure 2: Transfer Characteristics

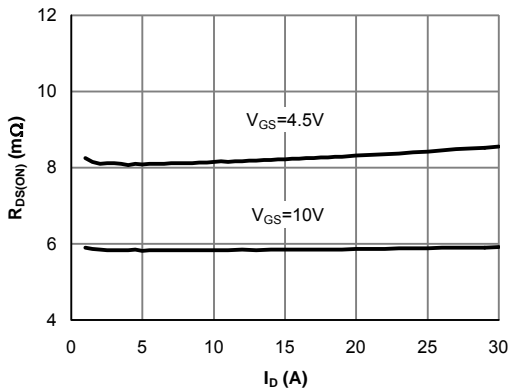


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

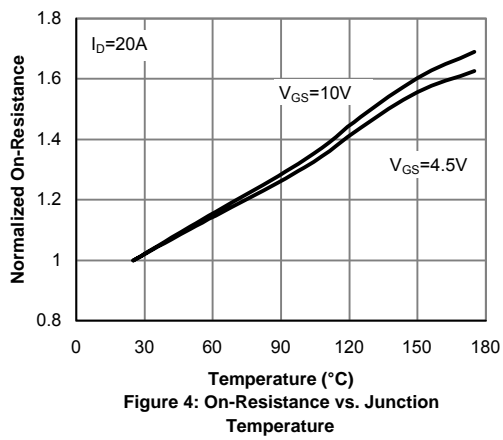


Figure 4: On-Resistance vs. Junction Temperature

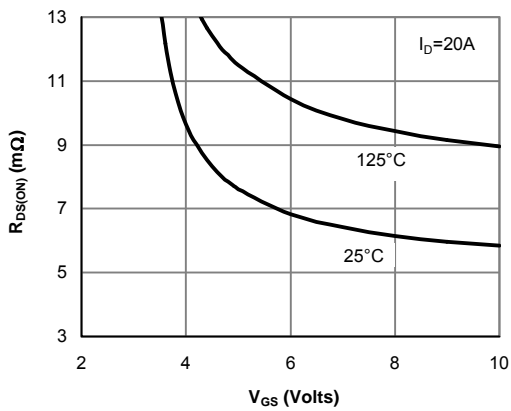


Figure 5: On-Resistance vs. Gate-Source Voltage

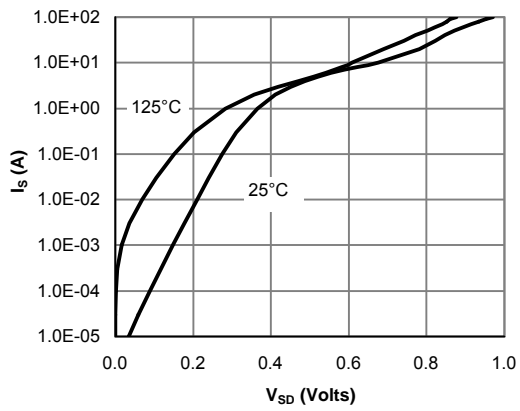


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

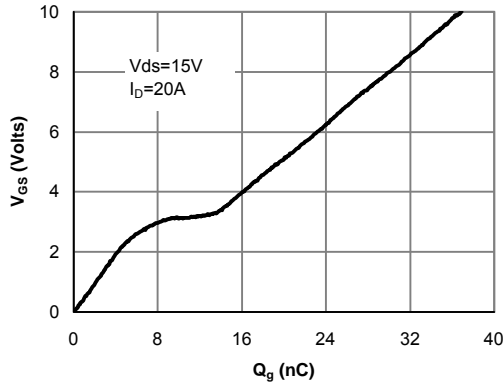


Figure 7: Gate-Charge Characteristics

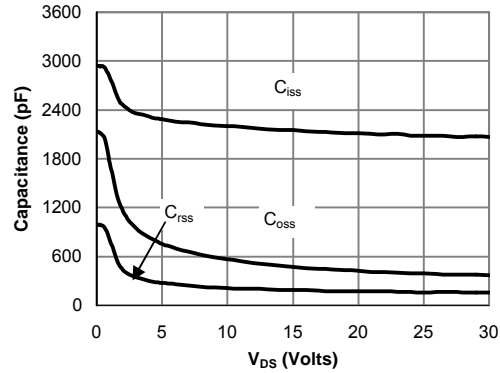


Figure 8: Capacitance Characteristics

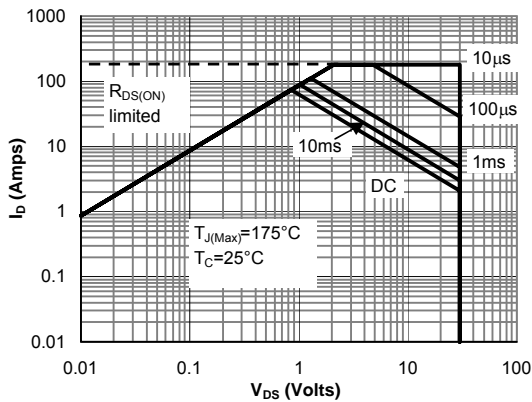


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

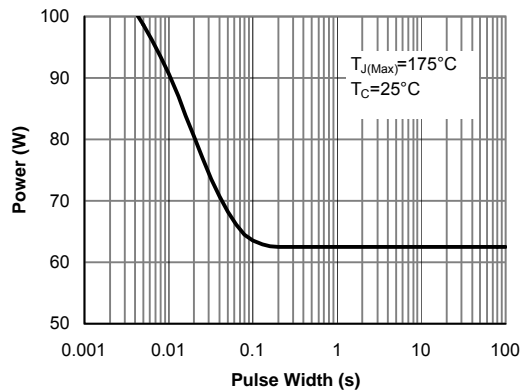


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

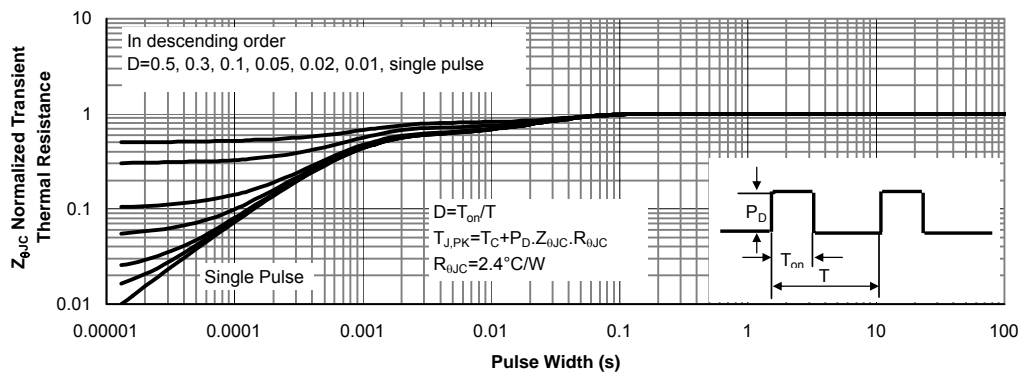


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

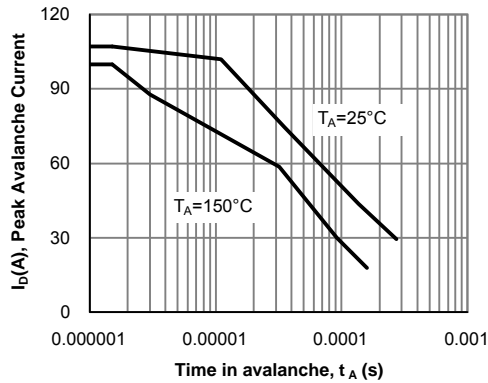


Figure 12: Single Pulse Avalanche capability

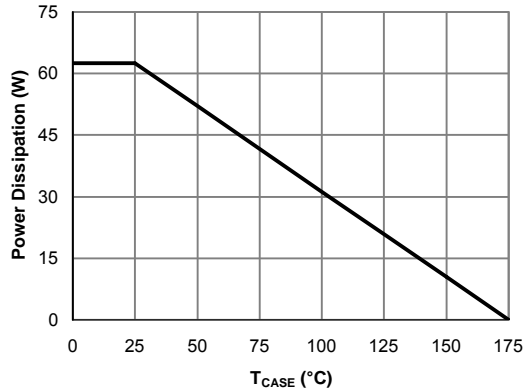


Figure 13: Power De-rating (Note B)

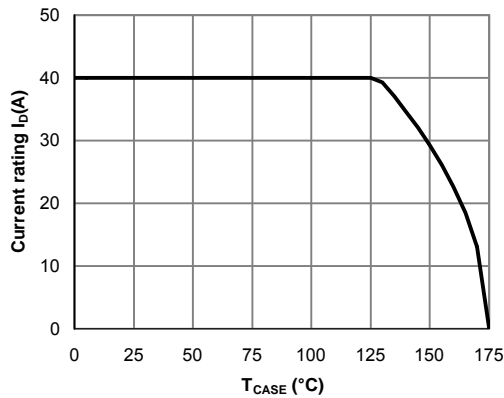


Figure 14: Current De-rating (Note B,G)

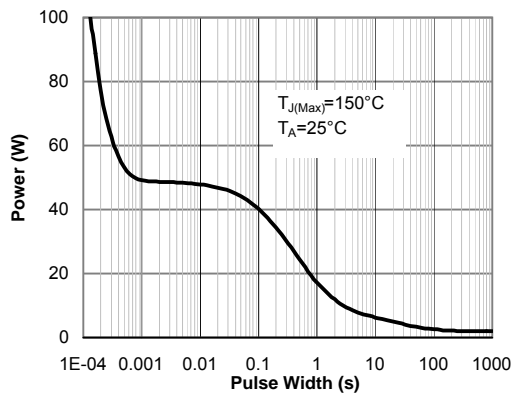


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

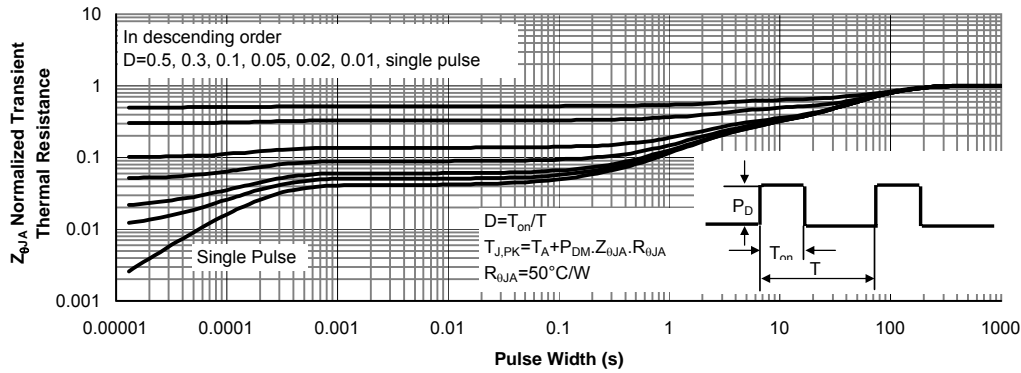


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)