



AOD420
N-Channel Enhancement Mode Field Effect Transistor

General Description

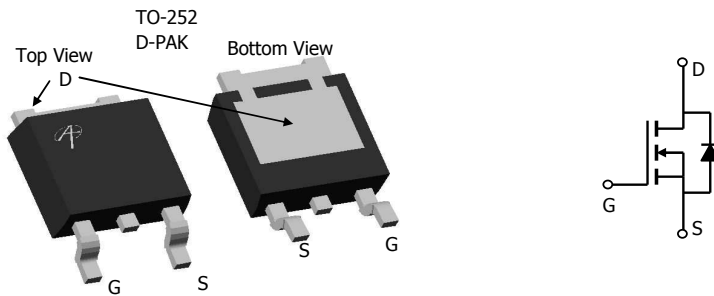
The AOD420 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications.

- RoHS Compliant
- Halogen Free*

Features

- $V_{DS} (V) = 30V$
- $I_D = 10A (V_{GS} = 10V)$
- $R_{DS(ON)} < 28m\Omega (V_{GS} = 10V)$
- $R_{DS(ON)} < 42m\Omega (V_{GS} = 4.5V)$

100% UIS Tested!
100% Rg Tested!



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	$T_C=25^\circ C$	10	A
	$T_C=100^\circ C$	10	
Pulsed Drain Current ^C	I_{DM}	30	
Avalanche Current ^C	I_{AR}	15	A
Repetitive avalanche energy $L=0.1mH$ ^C	E_{AR}	36	mJ
Power Dissipation ^B	$T_C=25^\circ C$	60	W
	$T_C=100^\circ C$	30	
Power Dissipation ^A	$T_A=25^\circ C$	2.5	W
	$T_A=70^\circ C$	1.6	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	16.7	25	$^\circ C/W$
Maximum Junction-to-Ambient ^A		Steady-State	40	50
Maximum Junction-to-Case ^B	$R_{\theta JC}$	1.9	2.5	$^\circ C/W$

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=24\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1	1.8	3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=4.5\text{V}$, $V_{DS}=5\text{V}$	40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=10\text{A}$ $T_J=125^\circ\text{C}$		21 31	28 40	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=7\text{A}$		32.5	42	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=10\text{A}$		15.6		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.75	1	V
I_S	Maximum Body-Diode Continuous Current				10	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=15\text{V}$, $f=1\text{MHz}$		710	850	pF
C_{oss}	Output Capacitance			120		pF
C_{riss}	Reverse Transfer Capacitance			72		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		1.1	3.6	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $I_D=10\text{A}$		14.4	18	nC
$Q_g(4.5\text{V})$	Total Gate Charge			7	8.4	nC
Q_{gs}	Gate Source Charge			2.6		nC
Q_{gd}	Gate Drain Charge			2.7		nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $R_L=1.5\Omega$, $R_{GEN}=3\Omega$		5.6		ns
t_r	Turn-On Rise Time			2.4		ns
$t_{D(off)}$	Turn-Off Delay Time			15.6		ns
t_f	Turn-Off Fall Time			2.2		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=10\text{A}$, $di/dt=100\text{A}/\mu\text{s}$		13.4	21	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=10\text{A}$, $di/dt=100\text{A}/\mu\text{s}$		4.4		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any a given application depends on the user's specific board design, and the maximum temperature fo 175°C may be used if the PCB allows it.

B: The power dissipation P_D is based on $T_{J(MAX)}=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^\circ\text{C}$.

D: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

G: The maximum current rating is limited by bond-wires.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

Rev5: Oct 2008

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

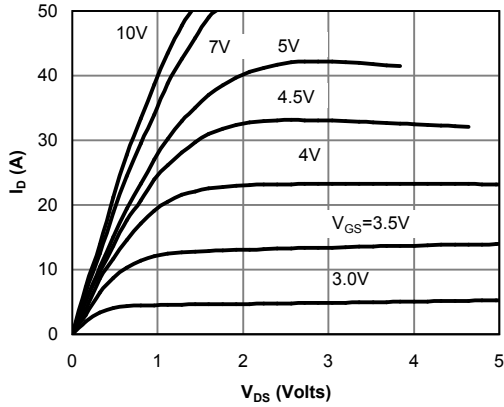


Fig 1: On-Region Characteristics

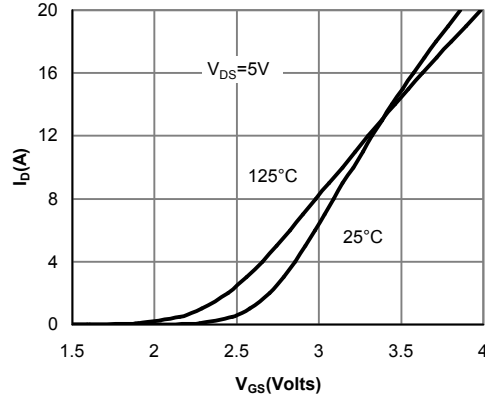


Figure 2: Transfer Characteristics

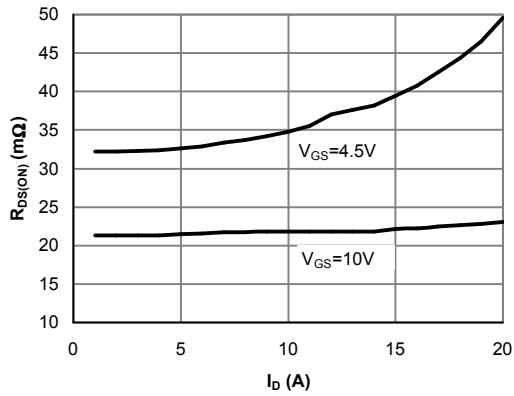


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

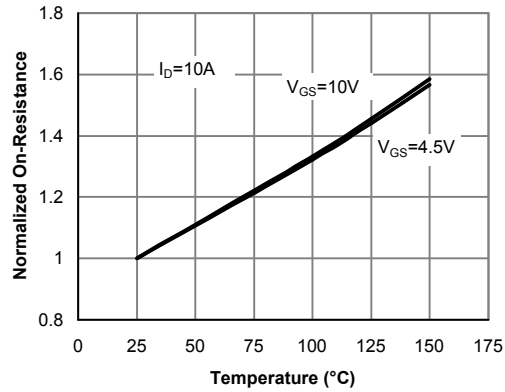


Figure 4: On-Resistance vs. Junction Temperature

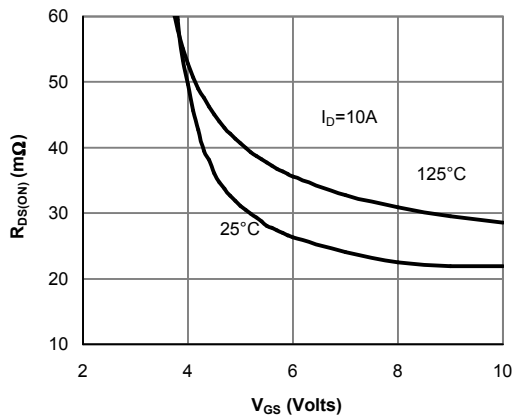


Figure 5: On-Resistance vs. Gate-Source Voltage

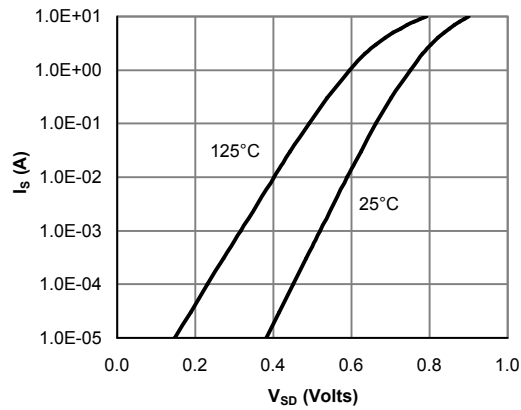


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

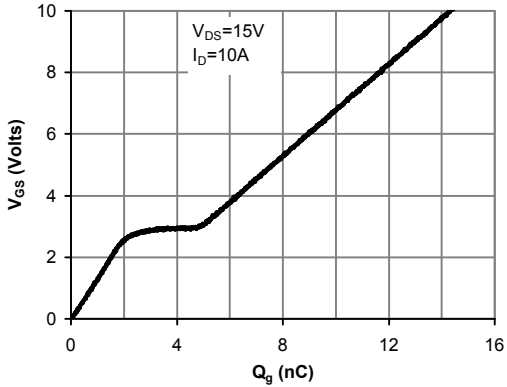


Figure 7: Gate-Charge Characteristics

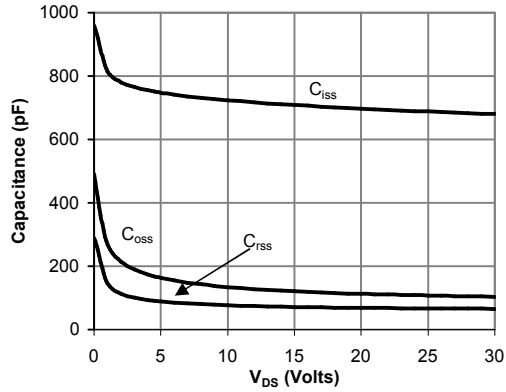


Figure 8: Capacitance Characteristics

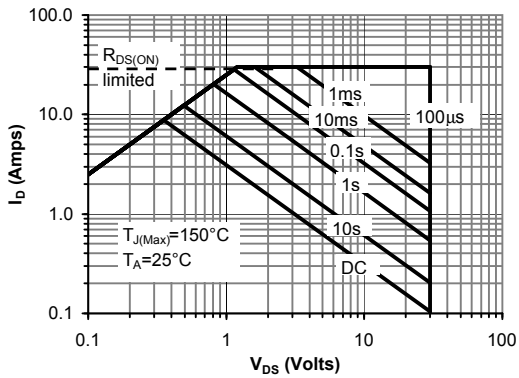


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

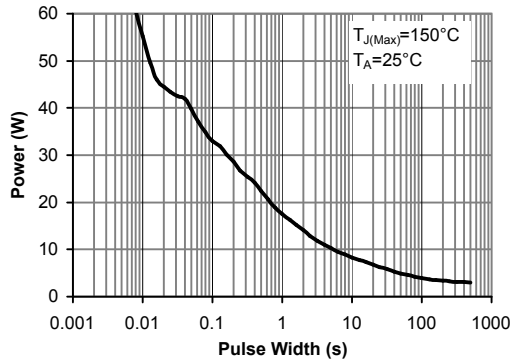


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

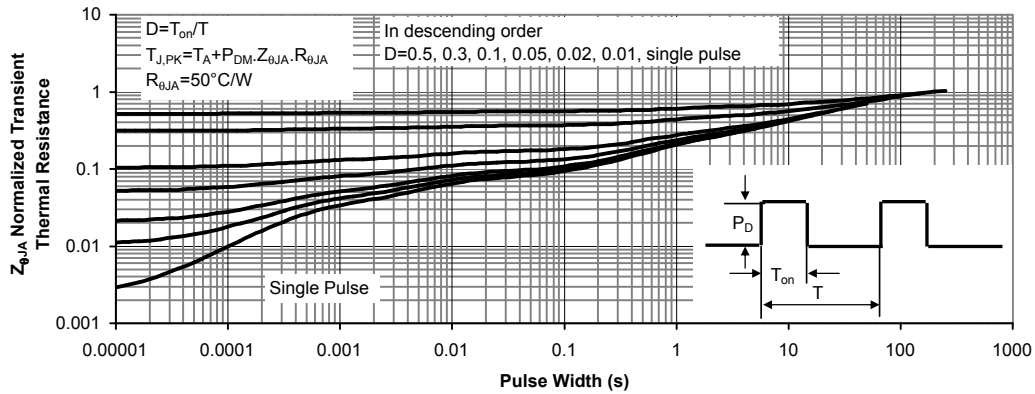
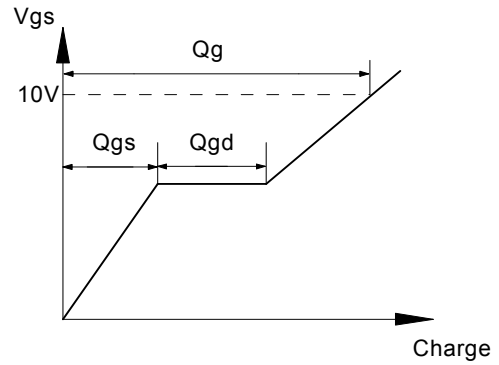
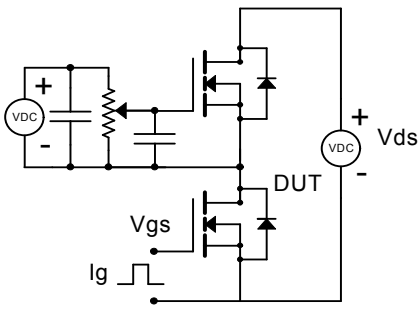
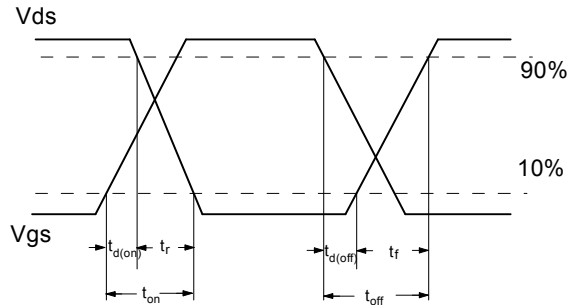
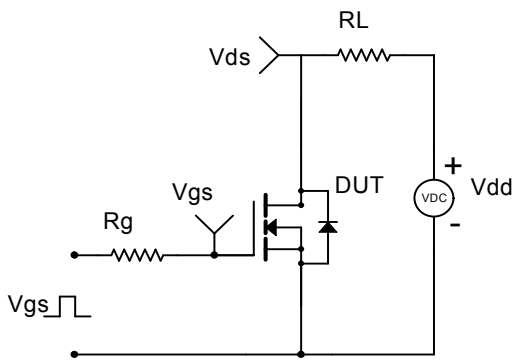


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

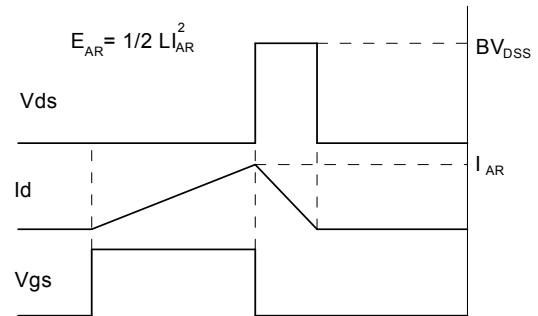
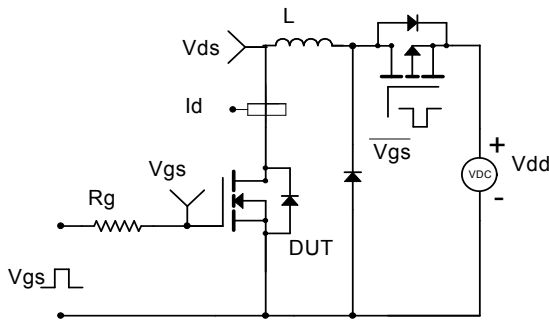
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

