ALPHA & OMEGA SEMICONDUCTOR

AOD490

N-Channel Enhancement Mode Field Effect Transistor

SRFET™

General Description

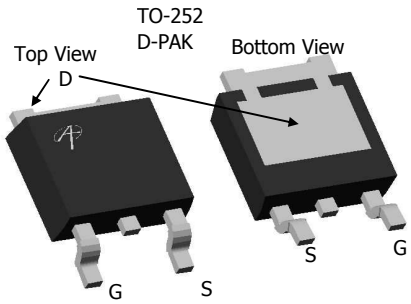
The AOD490 uses advanced trench technology with a monolithically integrated Schottky diode to provide excellent $R_{DS(ON)}$,and low gate charge. This device is suitable for use as a low side FET in SMPS, load switching and general purpose applications.

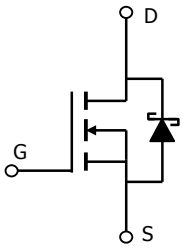
-RoHS Compliant
-Halogen Free*

Features

V_{DS} (V) = 30V
I_D =40A (V_{GS} = 10V)
$R_{DS(ON)}$ < 6.8mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 8.3mΩ (V_{GS} = 4.5V)

100% UIS Tested!
100% Rg Tested!





SRFET™
Soft Recovery MOSFET:
Integrated Schottky Diode

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current [B]	T_C=25°C [G]	I_D	40	A
	T_C=100°C [G]		31	
Pulsed Drain Current [C]		I_{DM}	100	
Continuous Drain Current[A]	T_A=25°C	I_{DSM}	15	A
	T_A=70°C		12	
Avalanche Current [C]		I_{AR}	30	A
Repetitive avalanche energy L=0.3mH [C]		E_{AR}	135	mJ
Power Dissipation [B]	T_C=25°C	P_D	63	W
	T_C=100°C		31	
Power Dissipation [A]	T_A=25°C	P_{DSM}	2.5	W
	T_A=70°C		1.6	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	15	20	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		41	50	°C/W
Maximum Junction-to-Case [D]	Steady-State	$R_{\theta JC}$	2	2.4	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250uA, V_{GS}=0V		30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=24V, V_{GS}=0V				0.1	mA
			T_J=125°C			20	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±12V				0.1	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA		1.5	1.85	2.4	V
$I_{D(ON)}$	On state drain current	V_{GS}=4.5V, V_{DS}=5V		100			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A			5.5	6.8	mΩ
			T_J=125°C		8.5	10.7	
		V_{GS}=4.5V, I_D=20A			6.7	8.3	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A			110		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V			0.37	0.5	V
I_S	Maximum Body-Diode + Schottky Continuous Current [G]					40	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz			4000	5000	pF
C_{oss}	Output Capacitance				520		pF
C_{rss}	Reverse Transfer Capacitance				217		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz			0.6	0.9	Ω
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=20A			59	77	
Q_g(4.5V)	Total Gate Charge				27		nC
Q_{gs}	Gate Source Charge				12		nC
Q_{gd}	Gate Drain Charge				11		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω			9		ns
t_r	Turn-On Rise Time				9		ns
$t_{D(off)}$	Turn-Off DelayTime				37		ns
t_f	Turn-Off Fall Time				8		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=300A/µs			16		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=300A/µs			22		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The power dissipation P_{DSM} and current rating IDSM are based on $T_{J(MAX)}$=150°C, using t ≤ 10s junction-to-ambient thermal resistance.The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

Rev1: Sep. 2008

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

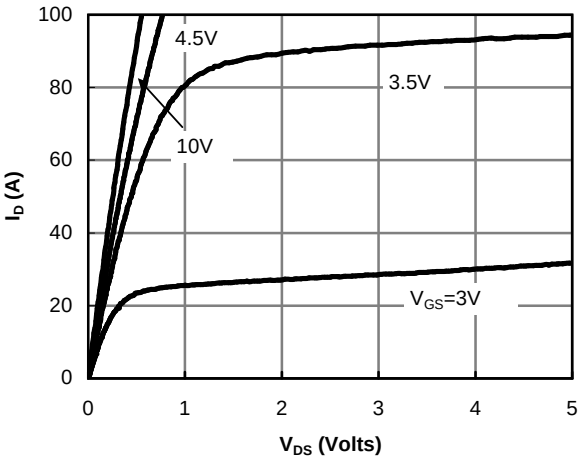


Figure 1: On-Region Characteristics

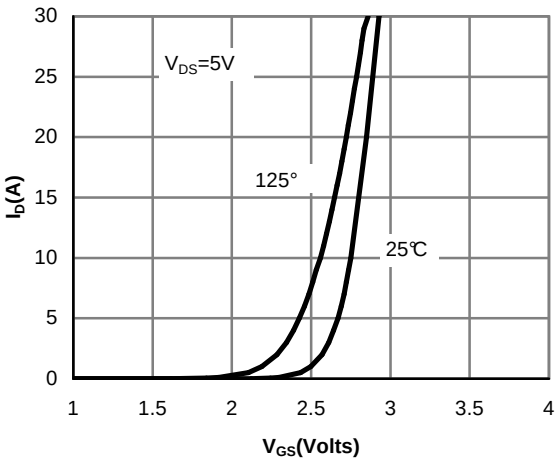


Figure 2: Transfer Characteristics

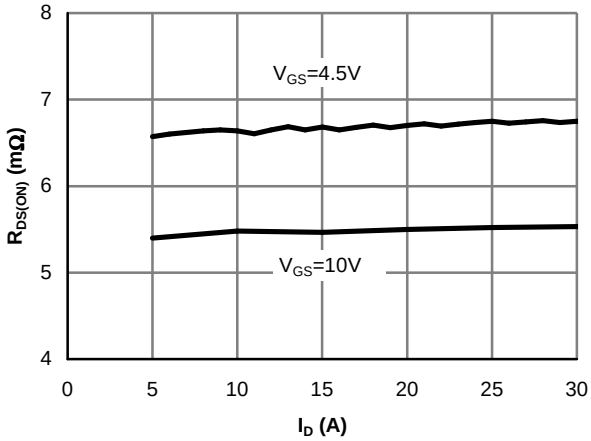


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

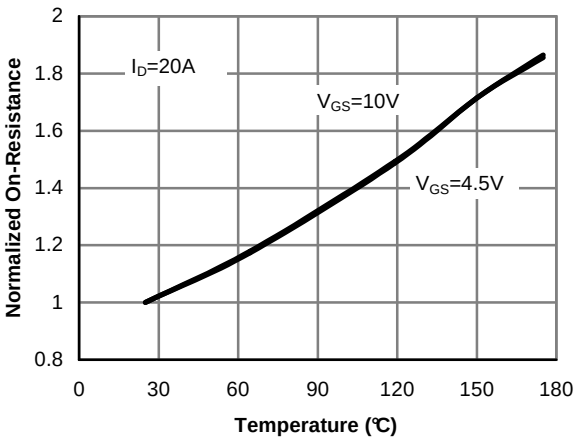


Figure 4: On-Resistance vs. Junction Temperature

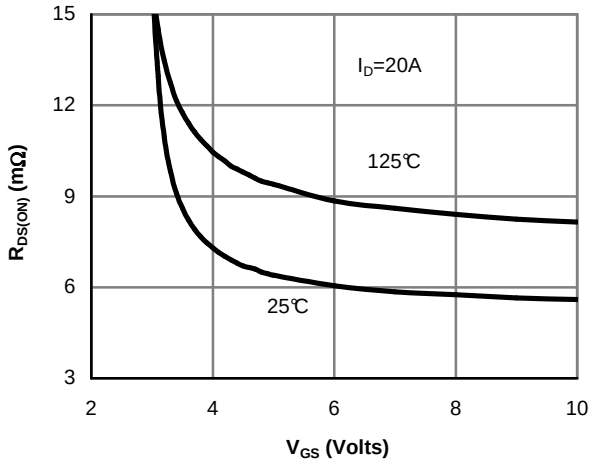


Figure 5: On-Resistance vs. Gate-Source Voltage

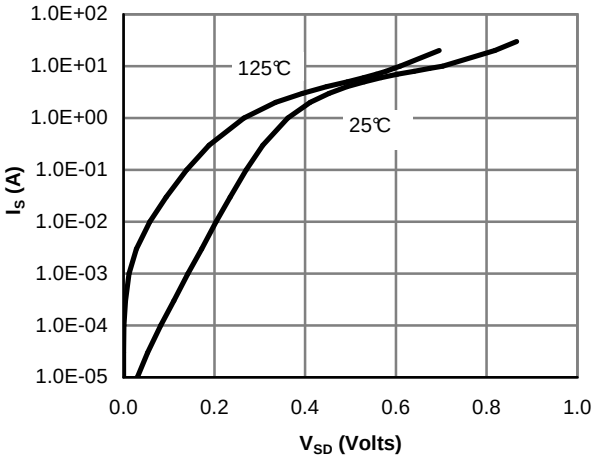


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

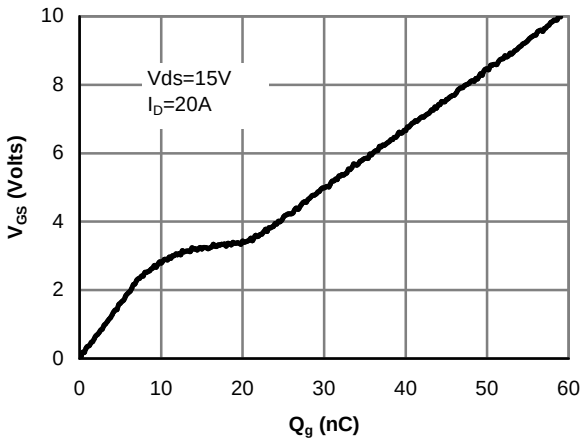


Figure 7: Gate-Charge Characteristics

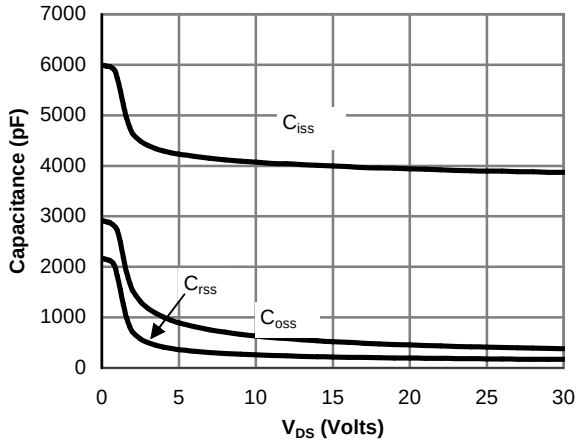


Figure 8: Capacitance Characteristics

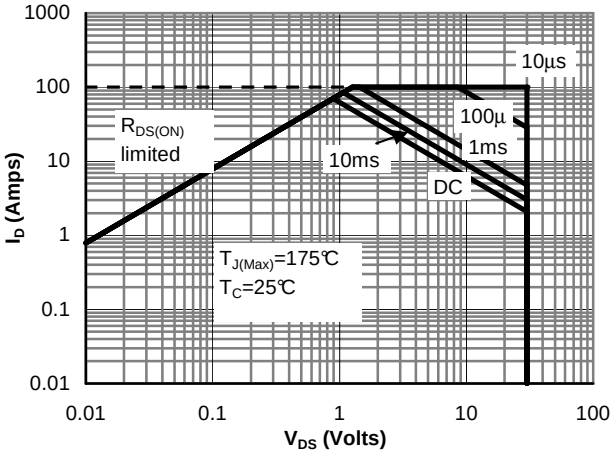


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

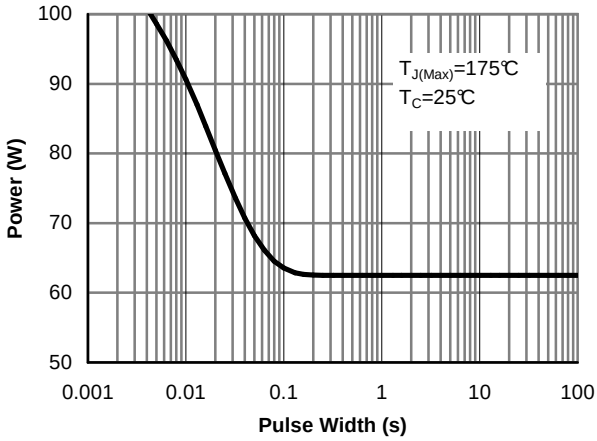


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

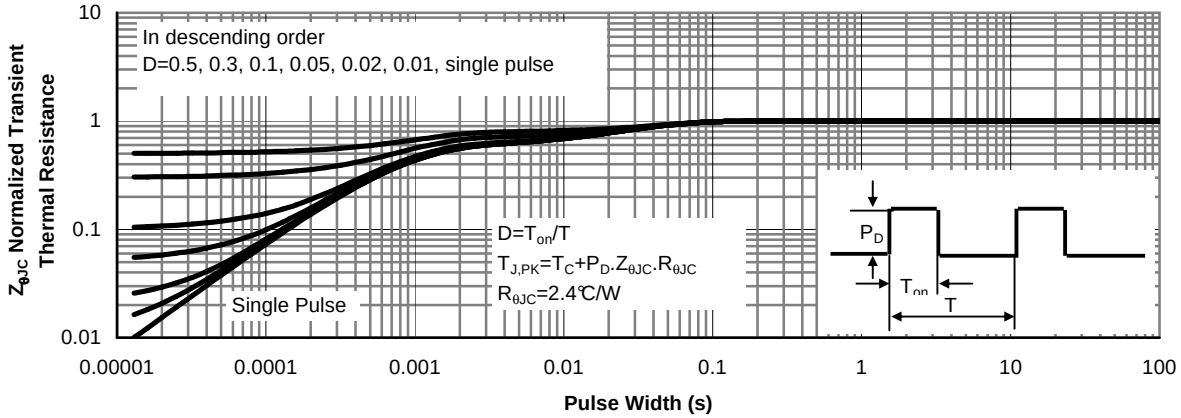


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

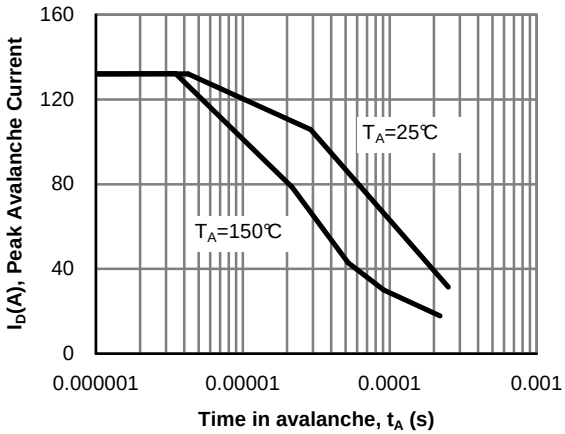


Figure 12: Single Pulse Avalanche capability

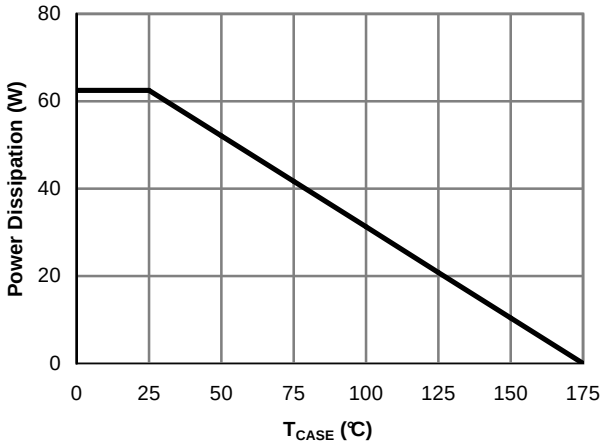


Figure 13: Power De-rating (Note B)

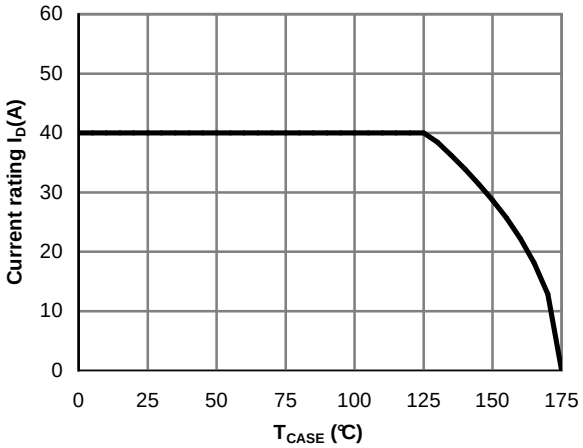


Figure 14: Current De-rating (Note B,G)

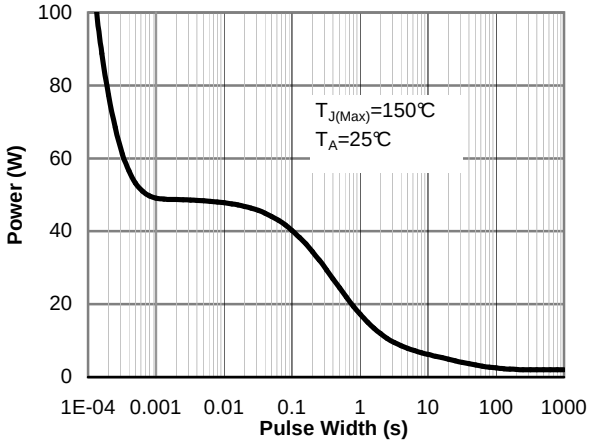


Figure15: Single Pulse Power Rating Junction-to-Ambient (Note H)

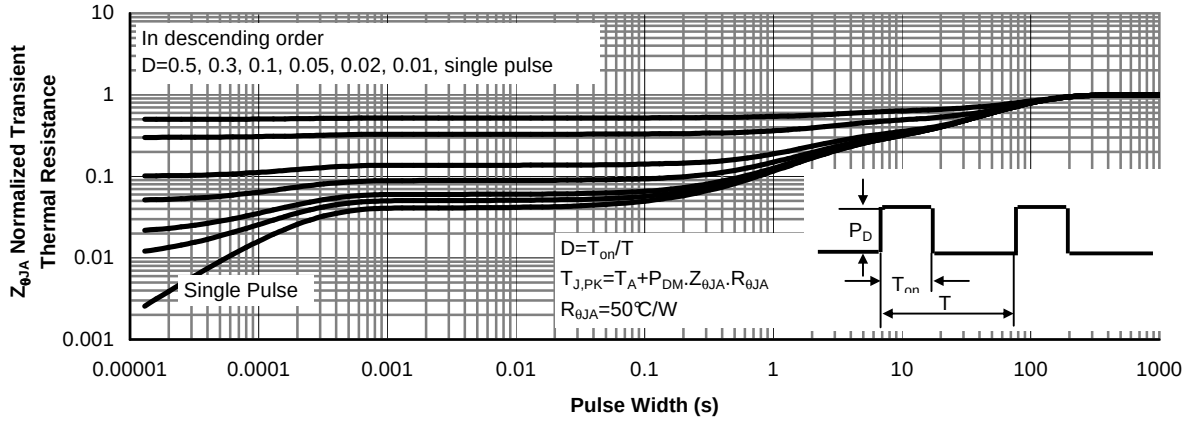


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

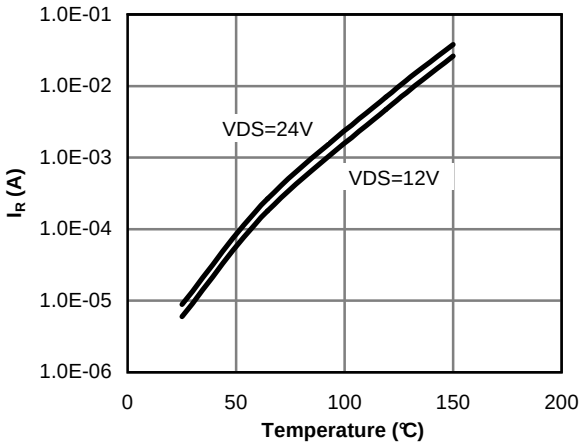


Figure 17: Diode Reverse Leakage Current vs. Junction Temperature

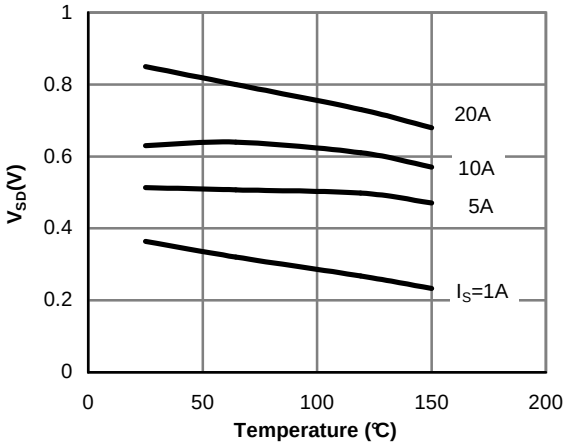


Figure 18: Diode Forward voltage vs. Junction Temperature

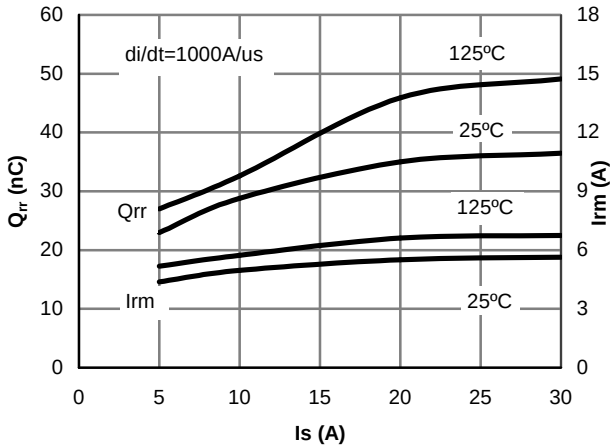


Figure 19: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

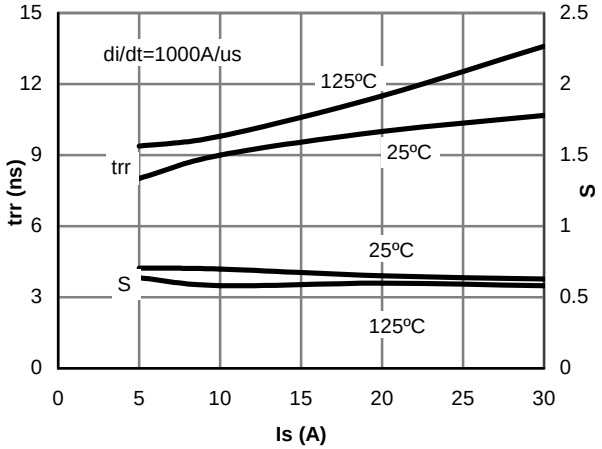


Figure 20: Diode Reverse Recovery Time and Soft Coefficient vs. Conduction Current

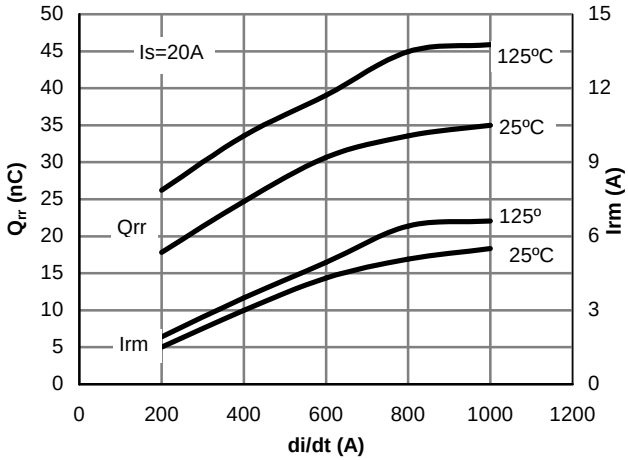


Figure 21: Diode Reverse Recovery Charge and Peak Current vs. di/dt

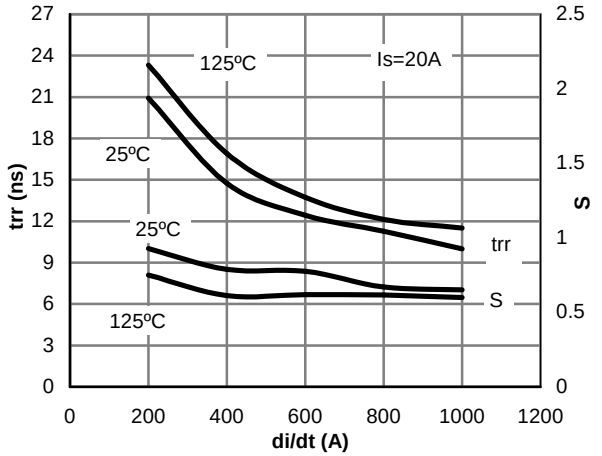
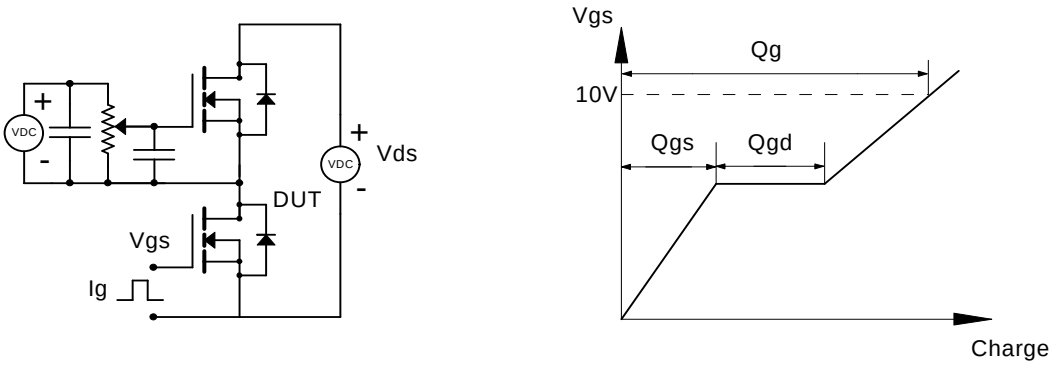
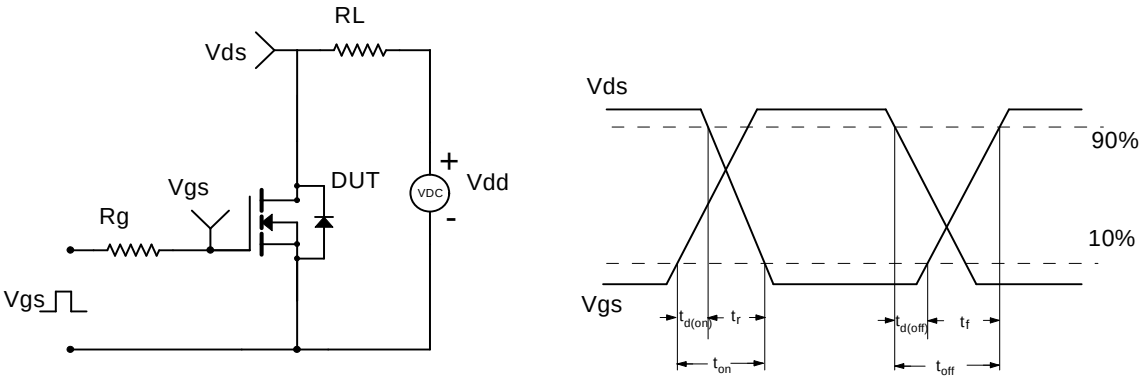


Figure 22: Diode Reverse Recovery Time and Soft Coefficient vs. di/dt

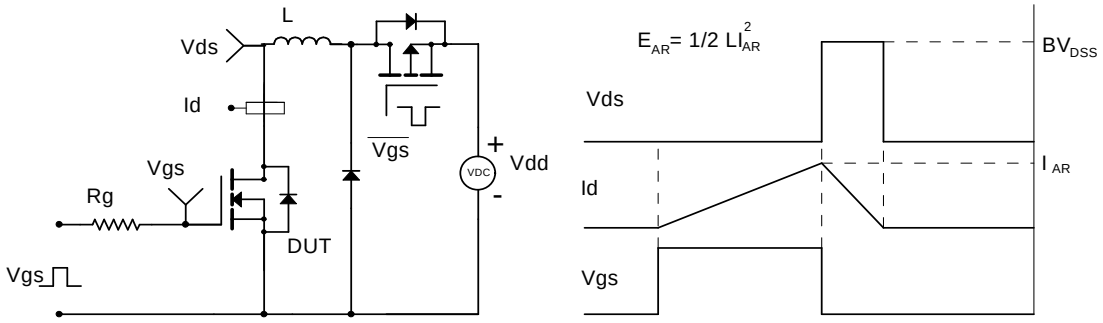
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms