



ALPHA & OMEGA
SEMICONDUCTOR



AOD603

Complementary Enhancement Mode Field Effect Transistor

General Description

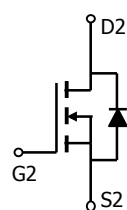
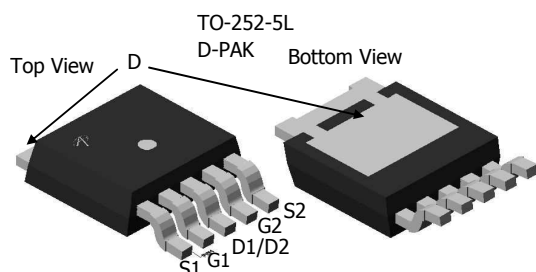
The AOD603 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications.

- RoHS Compliant
- Halogen Free*

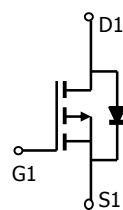
Features

n-channel	p-channel
V_{DS} (V) = 60V	-60V
I_D = 12A ($V_{GS}=10V$)	-12A
$R_{DS(ON)}$	$R_{DS(ON)}$
< 60m Ω ($V_{GS}=10V$)	< 115m Ω ($V_{GS} = -10V$)
< 85m Ω ($V_{GS}=4.5V$)	< 150m Ω ($V_{GS} = -4.5V$)

100% UIS Tested!



n-channel



p-channel

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	60	-60	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current ^G	$T_C=25^\circ\text{C}$	12	-12	A
	$T_C=100^\circ\text{C}$	9.4	-10	
Pulsed Drain Current ^C	I_{DM}	30	-30	
Avalanche Current ^C	I_{AR}	12	-12	A
Repetitive avalanche energy $L=0.1\text{mH}$ ^C	E_{AR}	23	23	mJ
Power Dissipation ^B	$T_C=25^\circ\text{C}$	20	37.5	W
	$T_C=100^\circ\text{C}$	10	18.8	
Power Dissipation ^A	$T_A=25^\circ\text{C}$	2	2.5	W
	$T_A=70^\circ\text{C}$	1.3	1.6	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	-55 to 175	$^\circ\text{C}$

Thermal Characteristics: n-channel and p-channel

Parameter	Symbol	Device	Typ	Max	
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	n-ch	17.4	30	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		n-ch	50	60	$^\circ\text{C/W}$
Maximum Junction-to-Case ^B	$R_{\theta JC}$	n-ch	4	7.5	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	p-ch	16.7	25	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		p-ch	40	50	$^\circ\text{C/W}$
Maximum Junction-to-Case ^B	$R_{\theta JC}$	p-ch	2.5	4	$^\circ\text{C/W}$

N-Channel MOSFET Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =10mA, V _{GS} =0V	60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =48V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1	2.4	3	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	30			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =12A		47	60	mΩ
		T _J =125°C		85		
		V _{GS} =4.5V, I _D =6A		67	85	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =12A		14		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.74	1	V
I _S	Maximum Body-Diode Continuous Current				12	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =30V, f=1MHz		450	540	pF
C _{oss}	Output Capacitance			61		pF
C _{rss}	Reverse Transfer Capacitance			27		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		1.35	2	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =30V, I _D =12A		7.5	10	nC
Q _g (4.5V)	Total Gate Charge			3.8	5	nC
Q _{gs}	Gate Source Charge			1.2		nC
Q _{gd}	Gate Drain Charge			1.9		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =30V, R _L =2.5Ω, R _{GEN} =3Ω		4.2		ns
t _r	Turn-On Rise Time			3.4		ns
t _{D(off)}	Turn-Off DelayTime			16		ns
t _f	Turn-Off Fall Time			2		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =12A, dI/dt=100A/μs		27.6	35	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =12A, dI/dt=100A/μs		30		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any a given application depends on the user's specific board design, and the maximum temperature fo 175°C may be used if the PCB allow s it.

B: The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C.

D: The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

Rev3: Sep. 2008

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N-Channel MOSFET TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

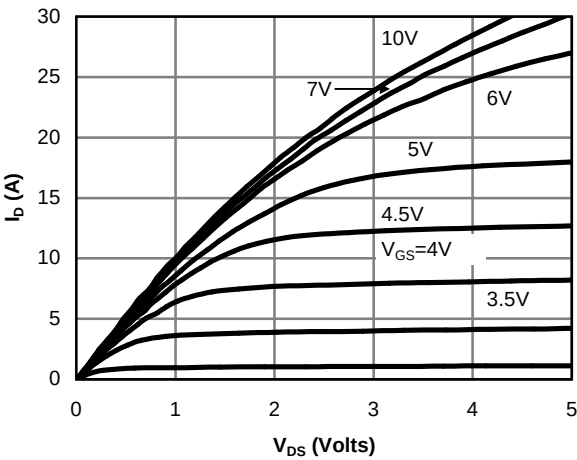


Fig 1: On-Region Characteristics

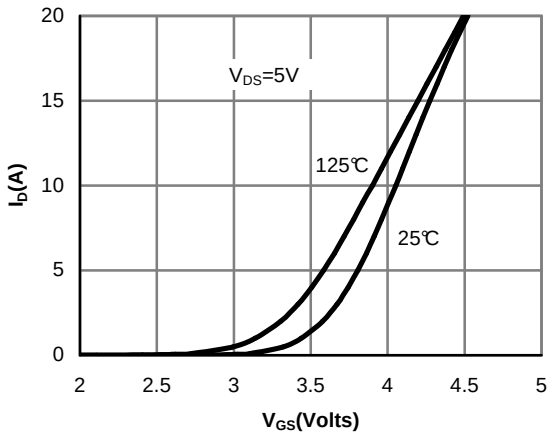


Figure 2: Transfer Characteristics

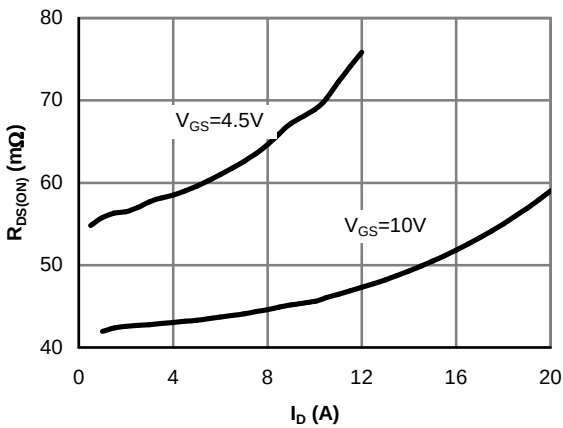


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

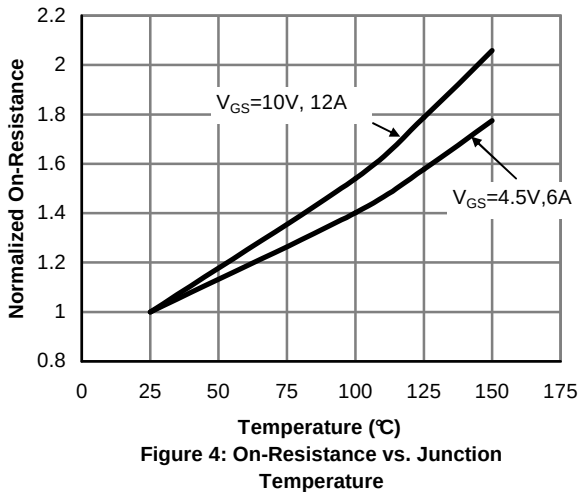


Figure 4: On-Resistance vs. Junction Temperature

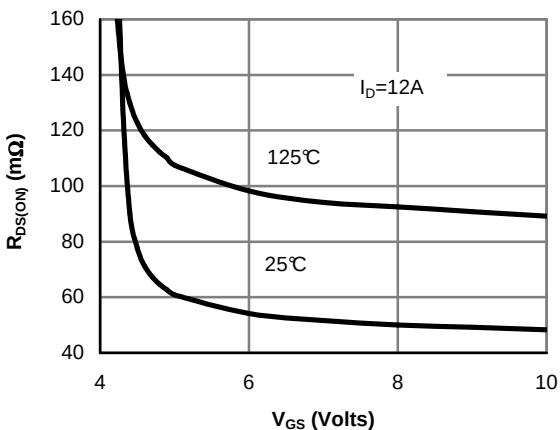


Figure 5: On-Resistance vs. Gate-Source Voltage

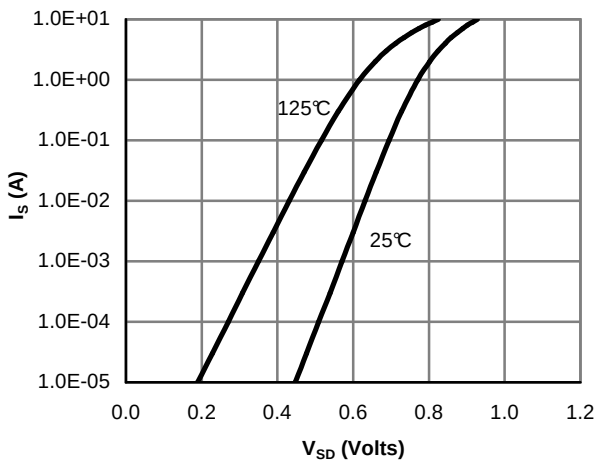


Figure 6: Body-Diode Characteristics

N-Channel MOSFET TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

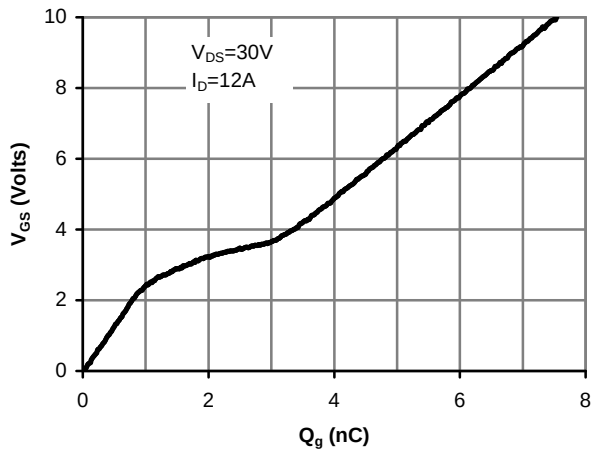


Figure 7: Gate-Charge Characteristics

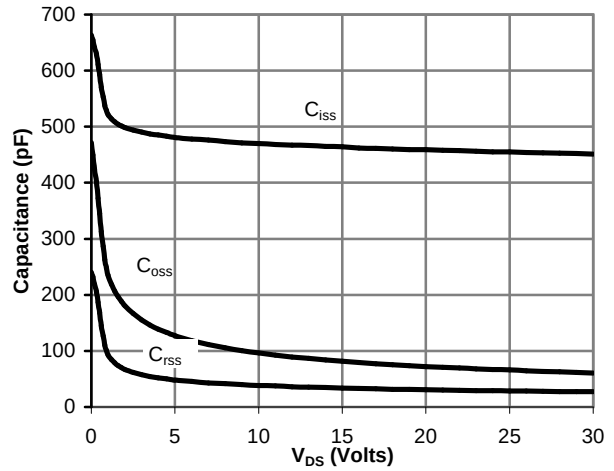


Figure 8: Capacitance Characteristics

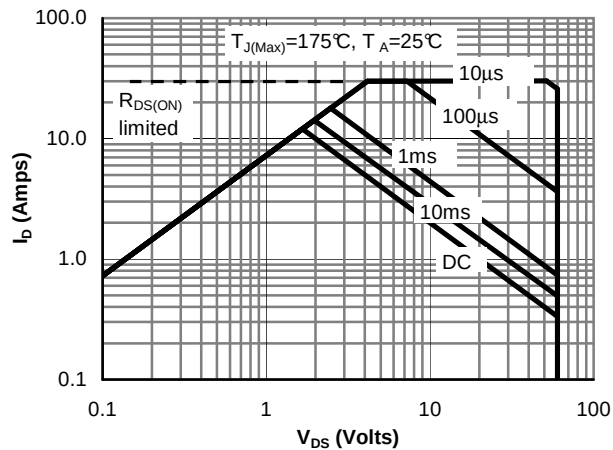


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

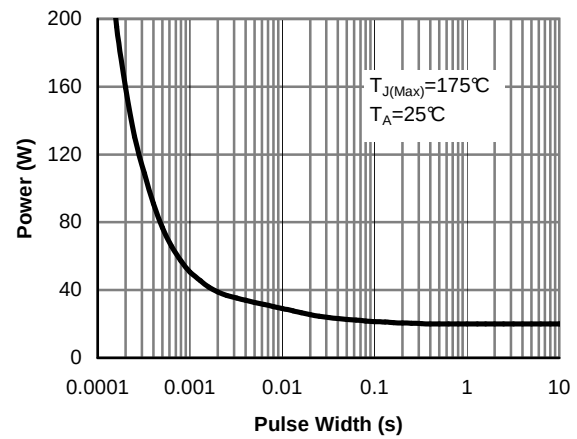


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

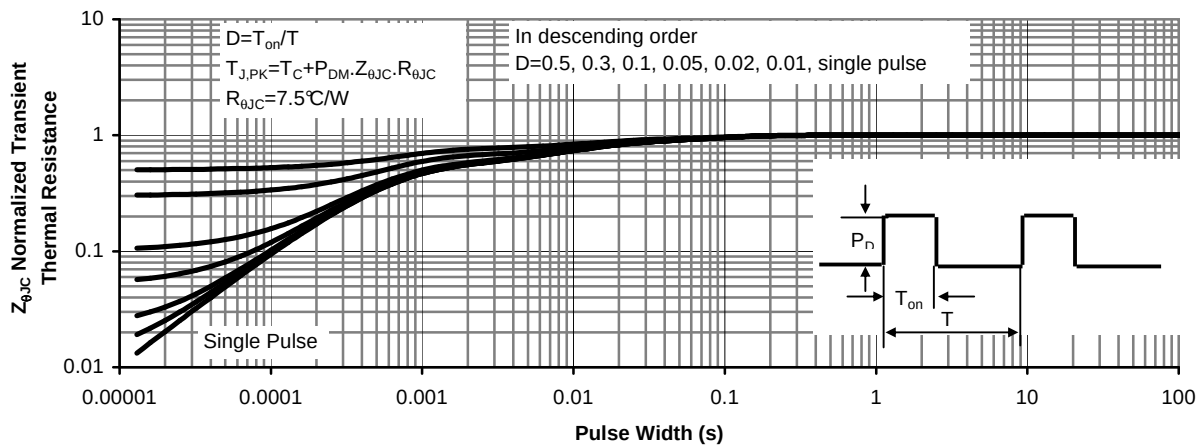


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

N-Channel MOSFET TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

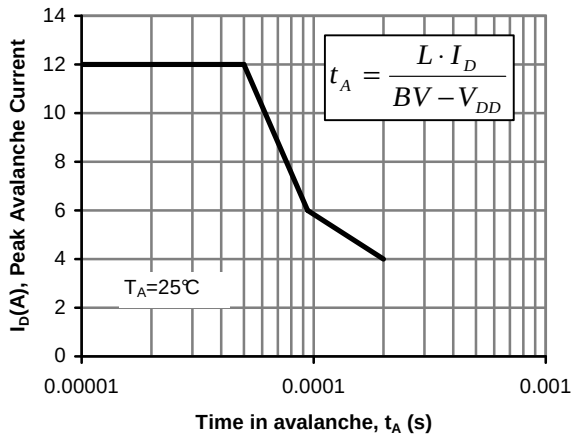


Figure 12: Single Pulse Avalanche capability

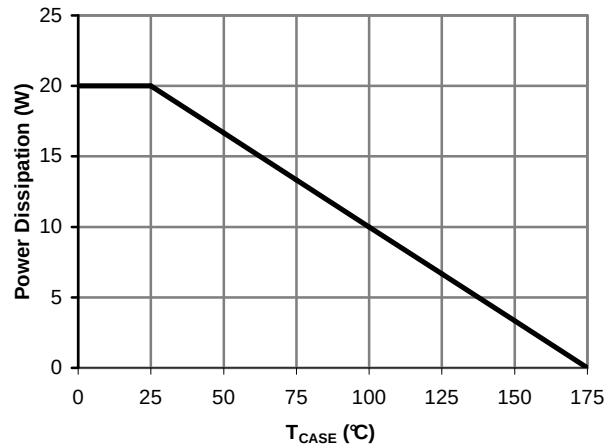


Figure 13: Power De-rating (Note B)

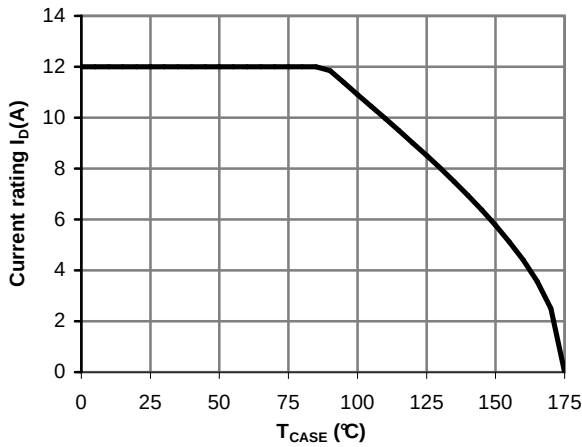


Figure 14: Current De-rating (Note B)

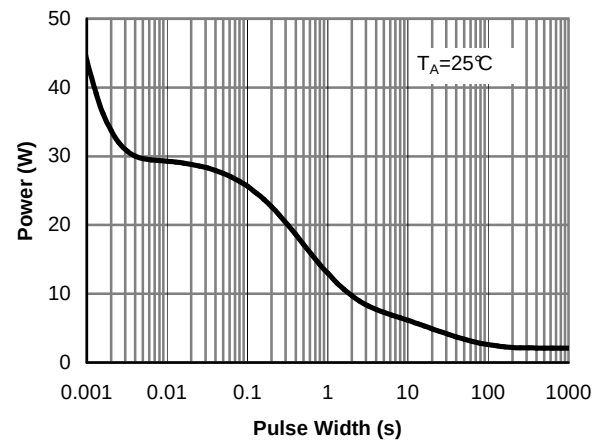


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

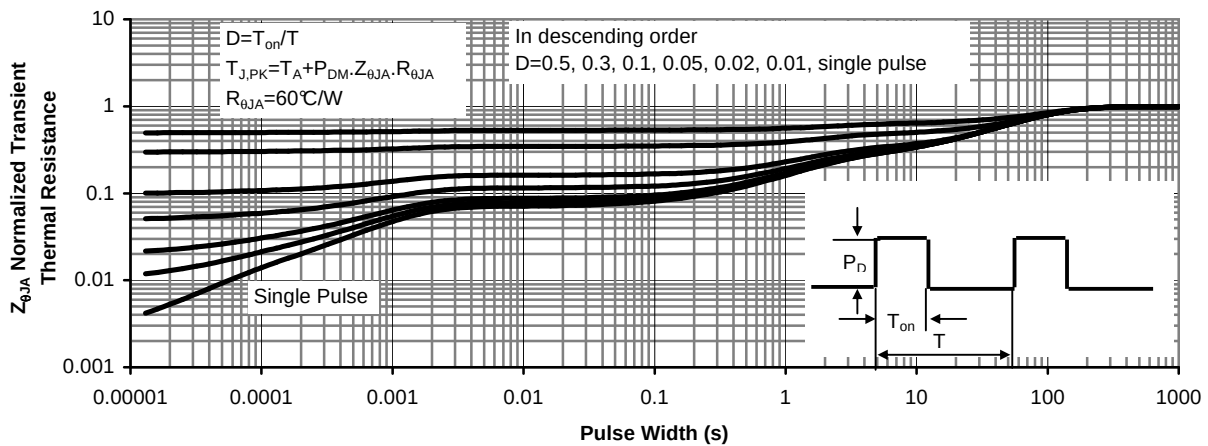


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

P-Channel MOSFET Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-48V, V _{GS} =0V T _J =55°C		-0.003	-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =-250μA	-1.5	-2.1	-3	V
I _{D(ON)}	On state drain current	V _{GS} =-10V, V _{DS} =-5V	-30			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-12A T _J =125°C		91 150	115	mΩ
		V _{GS} =-4.5V, I _D =-6A		114	150	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-12A		12.8		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.76	-1	V
I _S	Maximum Body-Diode Continuous Current				-12	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-30V, f=1MHz		987	1185	pF
C _{oss}	Output Capacitance			114		pF
C _{rss}	Reverse Transfer Capacitance			46		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		7	10	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge (10V)	V _{GS} =-10V, V _{DS} =-30V, I _D =-12A		15.8	20	nC
Q _g (4.5V)	Total Gate Charge (4.5V)			7.4	9	nC
Q _{gs}	Gate Source Charge			3		nC
Q _{gd}	Gate Drain Charge			3.5		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-30V, R _L =2.5Ω, R _{GEN} =3Ω		9		ns
t _r	Turn-On Rise Time			10		ns
t _{D(off)}	Turn-Off DelayTime			25		ns
t _f	Turn-Off Fall Time			11		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-12A, dI/dt=100A/μs		27.5	35	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-12A, dI/dt=100A/μs		30		nC

A: The value of R_{qJA} is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{qJA} and the maximum allowed junction temperature of 150°C. The value in any a given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation P_D is based on T_J(MAX)=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T_J(MAX)=175°C.

D: The R_{qJA} is the sum of the thermal impedance from junction to case R_{qJC} and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 ms pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_J(MAX)=175°C.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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P-Channel MOSFET Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

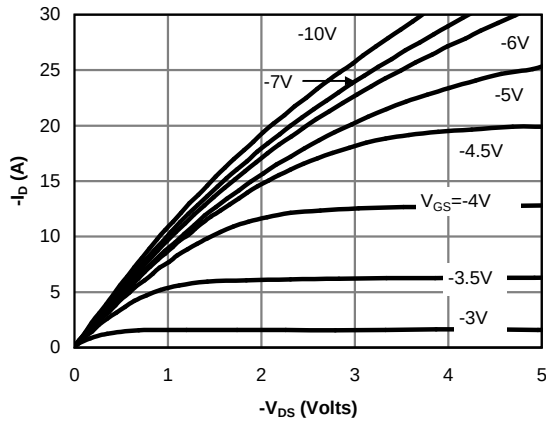


Fig 1: On-Region Characteristics

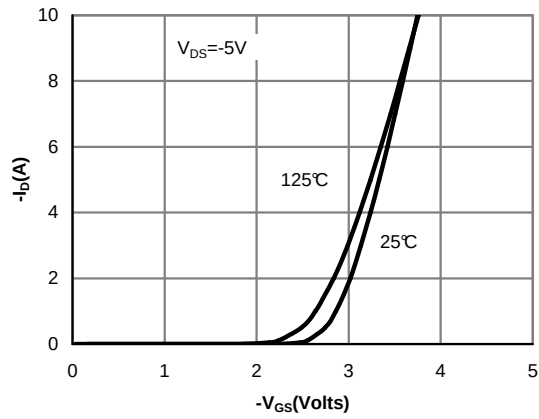


Figure 2: Transfer Characteristics

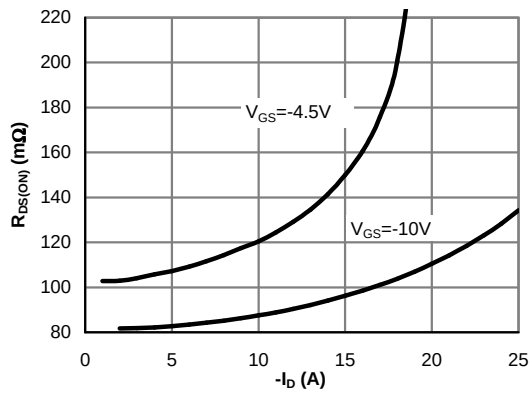


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

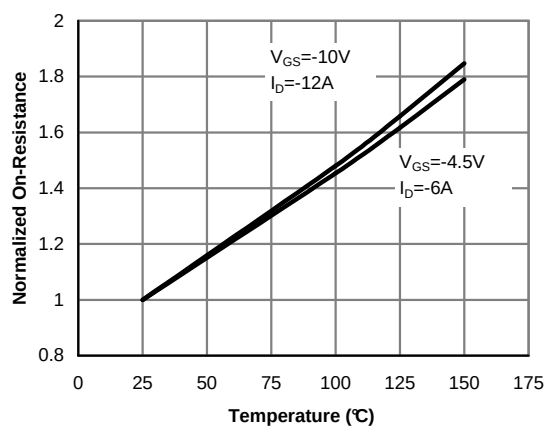


Figure 4: On-Resistance vs. Junction Temperature

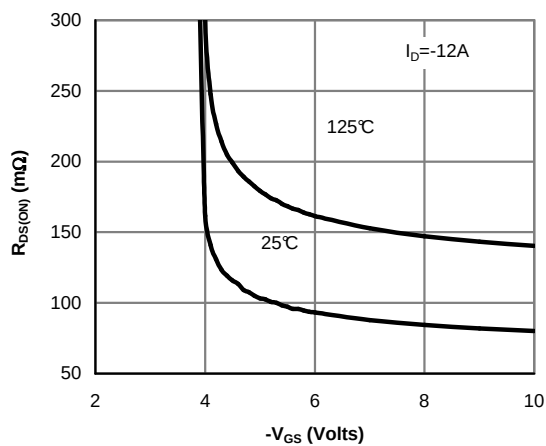


Figure 5: On-Resistance vs. Gate-Source Voltage

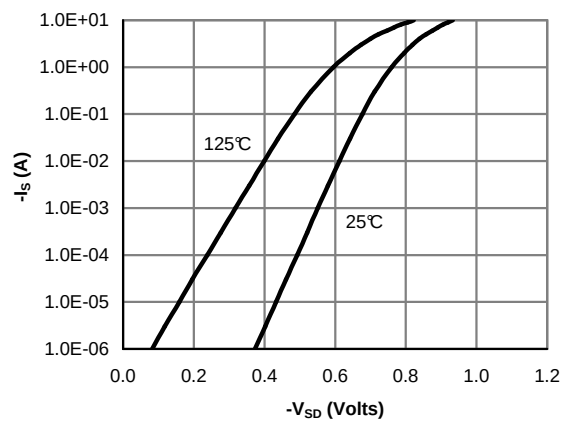
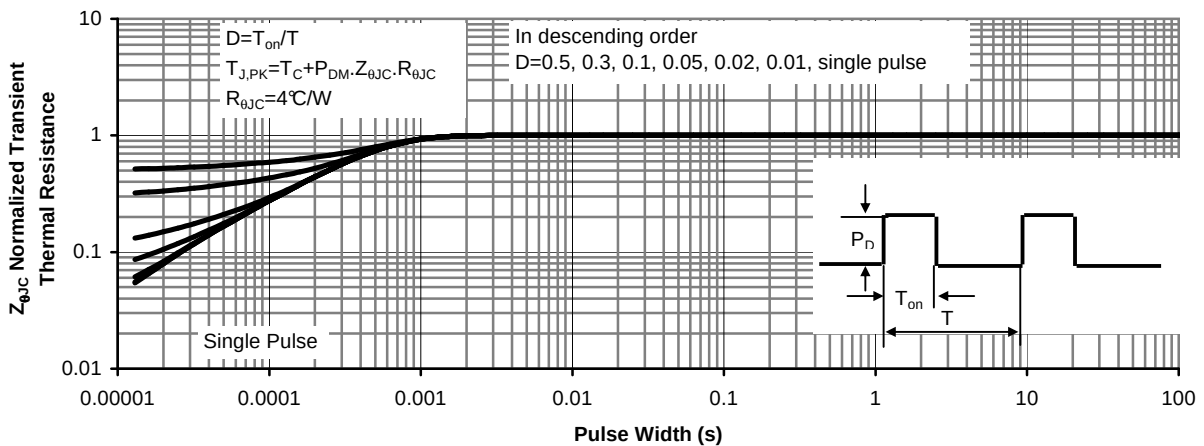
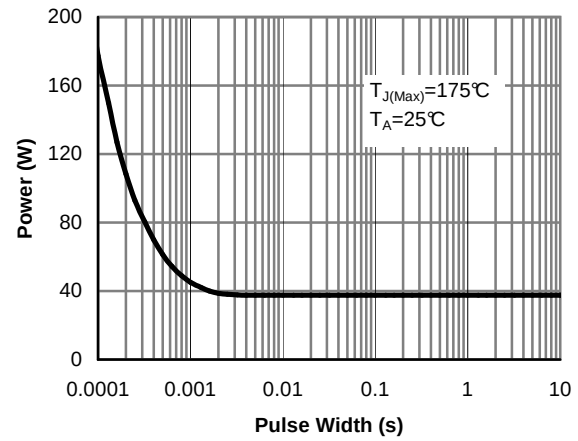
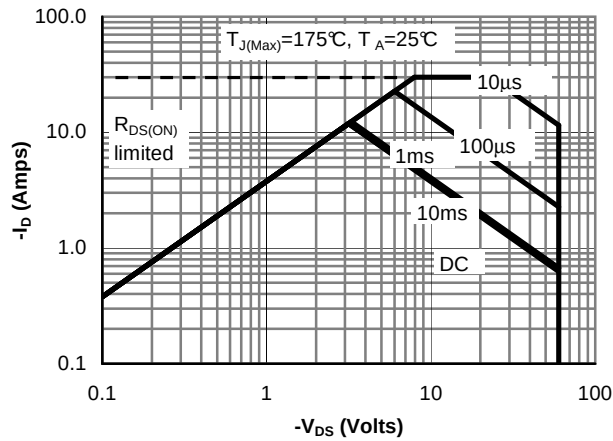
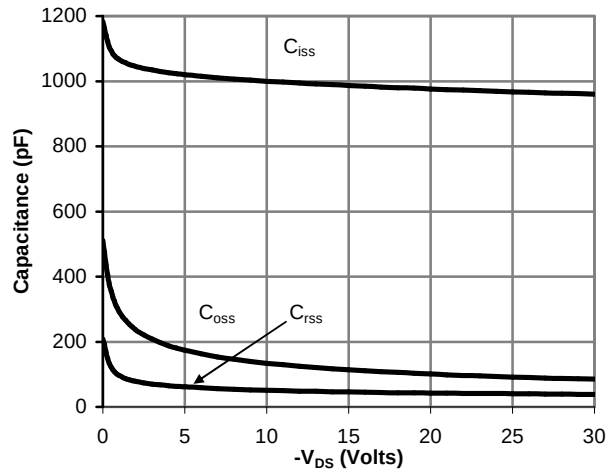
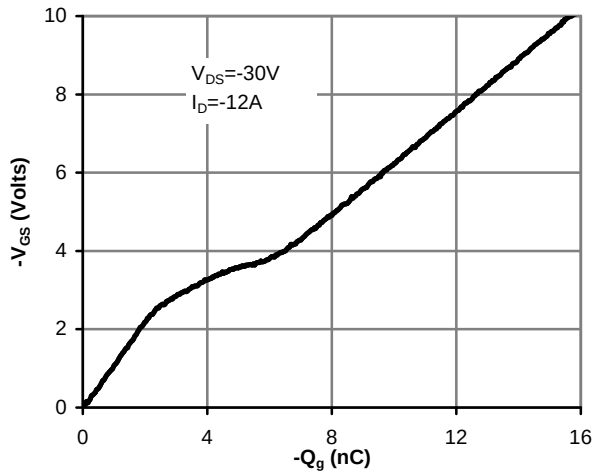


Figure 6: Body-Diode Characteristics

P-Channel MOSFET Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

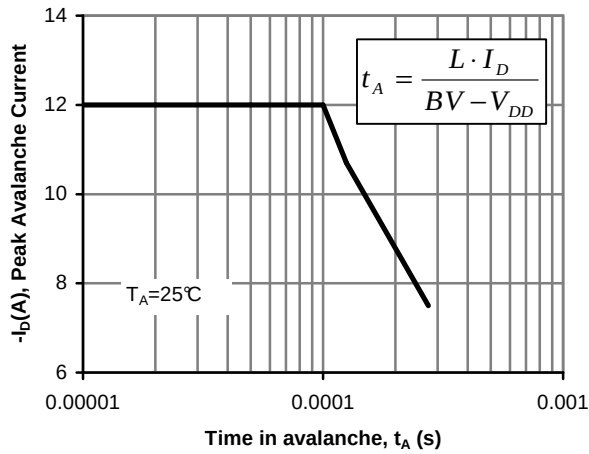
P-Channel MOSFET Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Figure 12: Single Pulse Avalanche capability

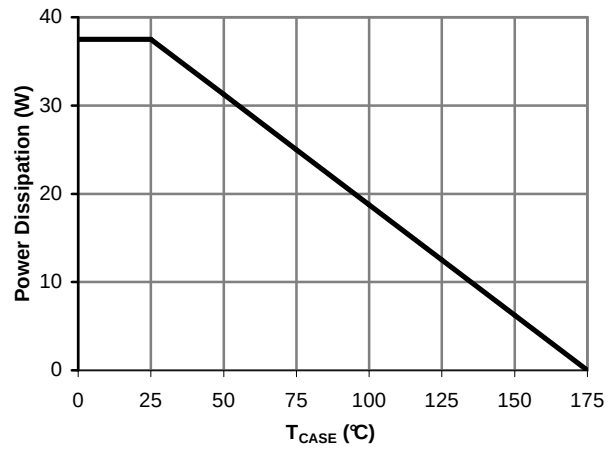


Figure 13: Power De-rating (Note B)

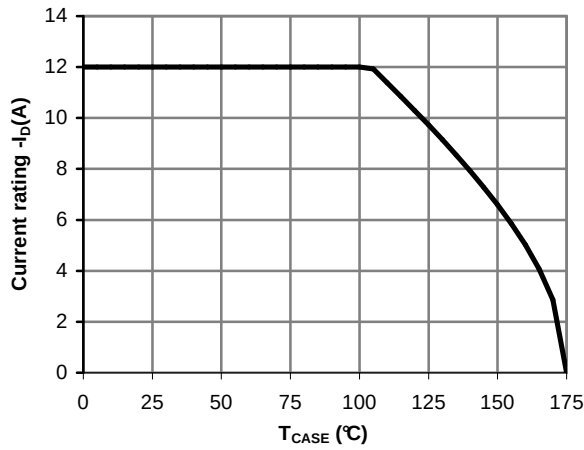


Figure 14: Current De-rating (Note B)

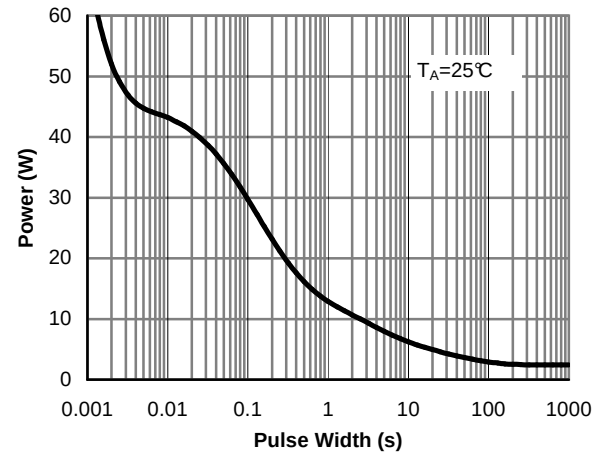


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

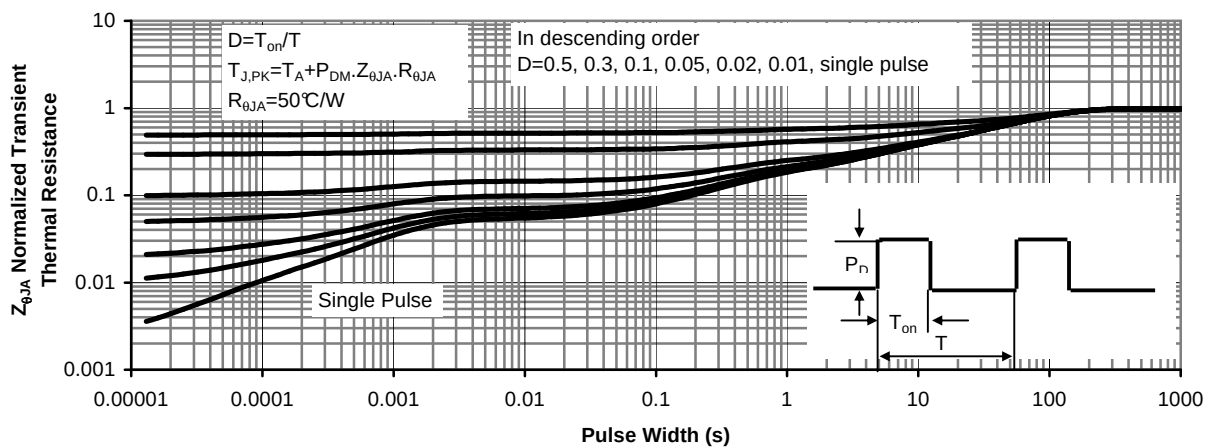
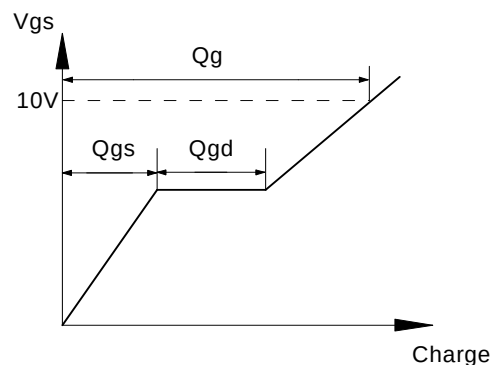
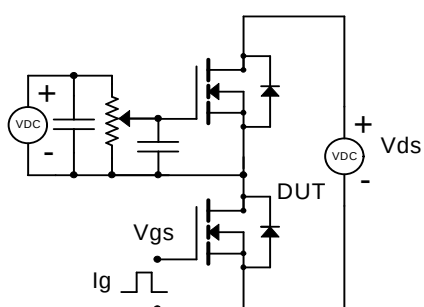
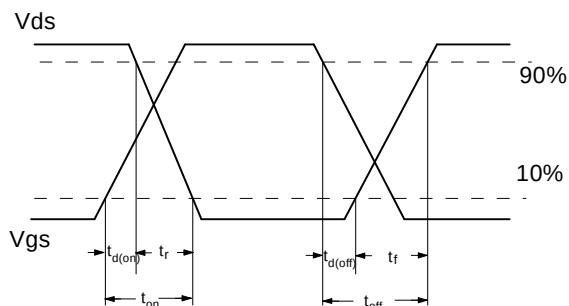
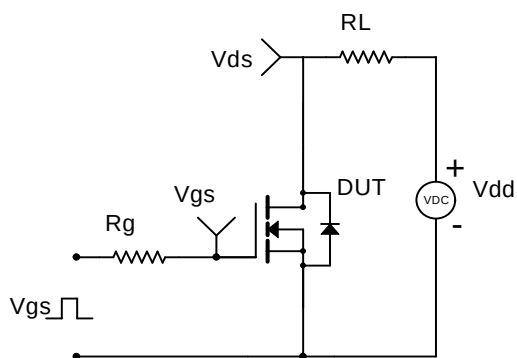


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

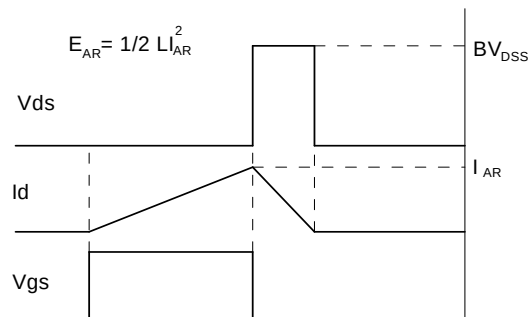
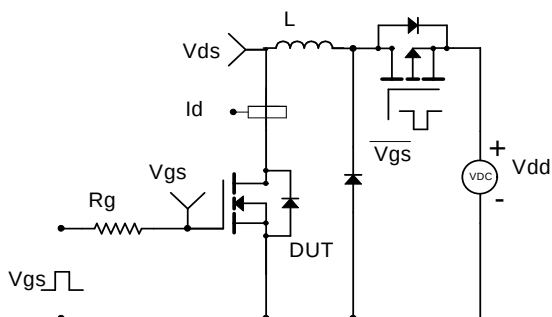
Gate Charge Test Circuit & Waveform



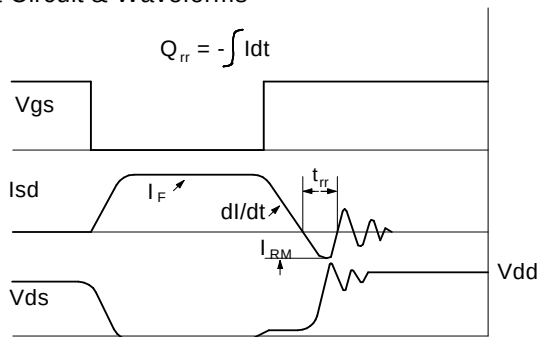
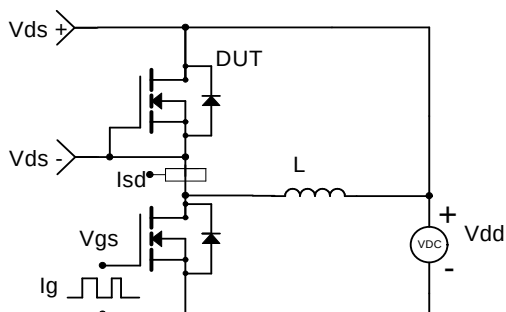
Resistive Switching Test Circuit & Waveforms



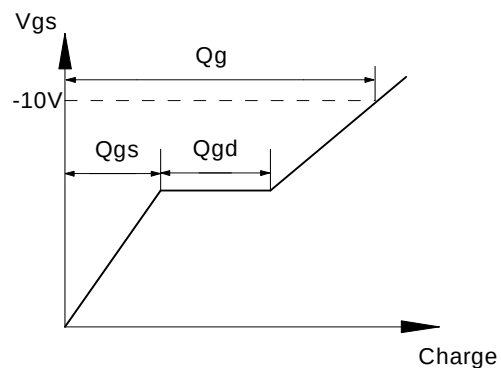
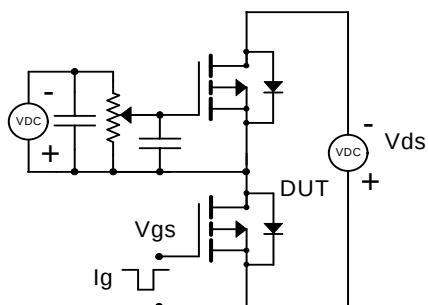
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



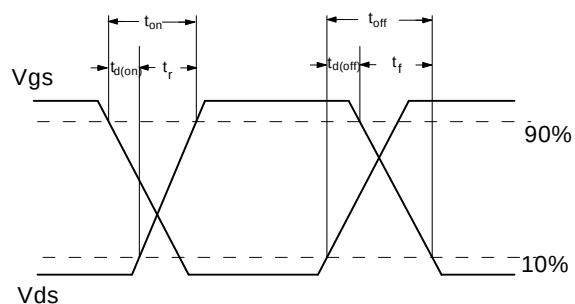
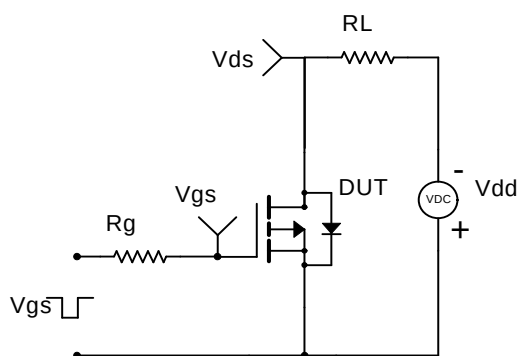
Diode Recovery Test Circuit & Waveforms



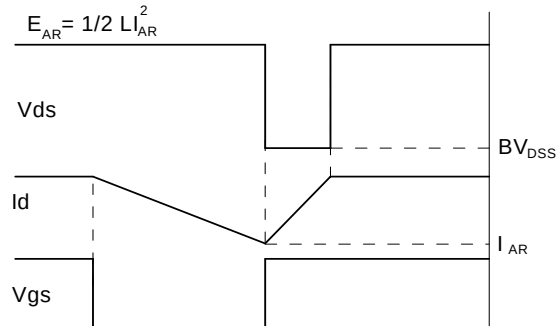
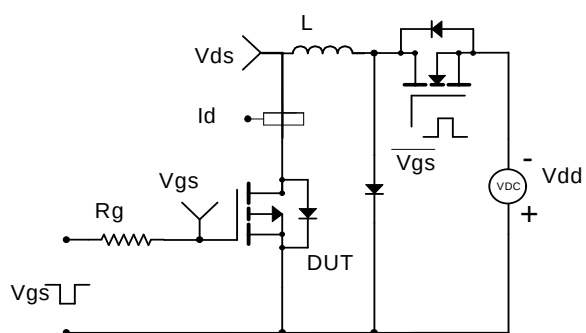
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

