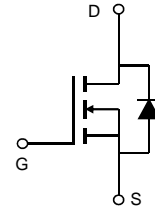
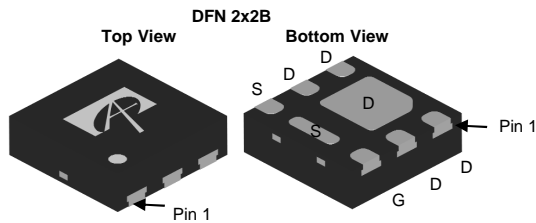


### General Description

The AON2400 combines advanced trench MOSFET technology with a low resistance package to provide extremely low  $R_{DS(ON)}$ . This device is ideal for load switch and battery protection applications.

### Product Summary

$V_{DS}$	8V
$I_D$ (at $V_{GS}=4.5V$ )	8A
$R_{DS(ON)}$ (at $V_{GS} = 2.5V$ )	< 11m $\Omega$
$R_{DS(ON)}$ (at $V_{GS} = 1.8V$ )	< 13m $\Omega$
$R_{DS(ON)}$ (at $V_{GS} = 1.5V$ )	< 16m $\Omega$
$R_{DS(ON)}$ (at $V_{GS} = 1.2V$ )	< 23m $\Omega$



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	8	V
Gate-Source Voltage	$V_{GS}$	$\pm 5$	V
Continuous Drain Current <sup>G</sup>	$I_D$	$T_A=25^\circ\text{C}$	8
		$T_A=100^\circ\text{C}$	6
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	32	A
Power Dissipation <sup>A</sup>	$P_D$	$T_A=25^\circ\text{C}$	2.8
		$T_A=70^\circ\text{C}$	1.8
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	37	45	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Ambient <sup>A,D</sup>		Steady-State	66	80

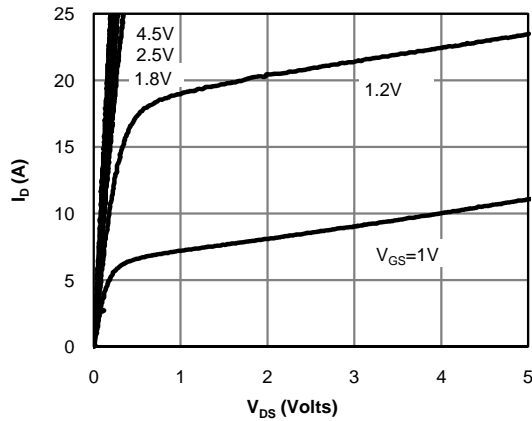
**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	8			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =8V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±5V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA		0.46		V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =5V	32			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =2.5V, I <sub>D</sub> =8A T <sub>J</sub> =125°C		8.5 11	11 14	mΩ
		V <sub>GS</sub> =1.8V, I <sub>D</sub> =6A		10	13	mΩ
		V <sub>GS</sub> =1.5V, I <sub>D</sub> =5A		11.5	16	mΩ
		V <sub>GS</sub> =1.2V, I <sub>D</sub> =3A		16	23	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =8A		100		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.53	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				4.5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =4V, f=1MHz		1645		pF
C <sub>oss</sub>	Output Capacitance			470		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			320		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		1.6	3.2	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =4V, I <sub>D</sub> =8A		16		nC
Q <sub>gs</sub>	Gate Source Charge			2		nC
Q <sub>gd</sub>	Gate Drain Charge			2.8		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =4V, R <sub>L</sub> =0.5Ω, R <sub>GEN</sub> =3Ω		7		ns
t <sub>r</sub>	Turn-On Rise Time			25		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			37		ns
t <sub>f</sub>	Turn-Off Fall Time			13		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =8A, di/dt=100A/μs		17		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =8A, di/dt=100A/μs		9		nC

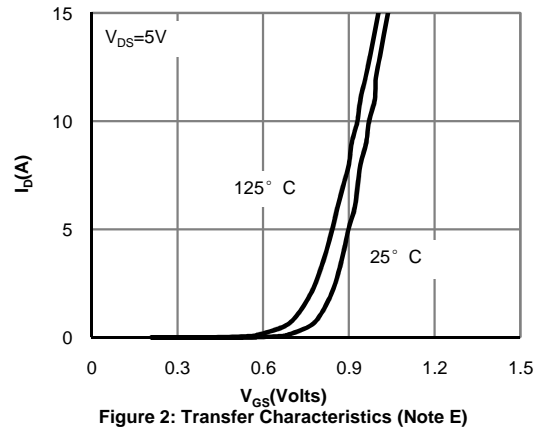
- A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> t ≤ 10s value and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
- B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25° C.
- D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.
- G. The maximum current rating is package limited.
- H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

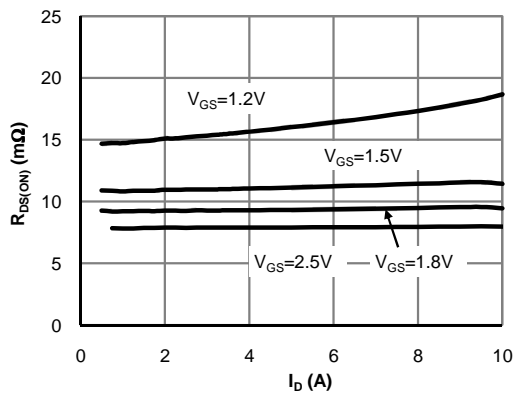
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



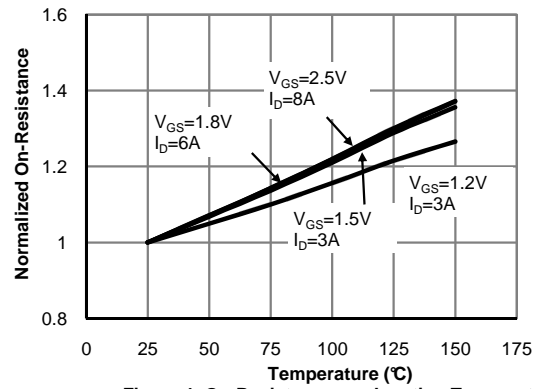
**Fig 1: On-Region Characteristics (Note E)**



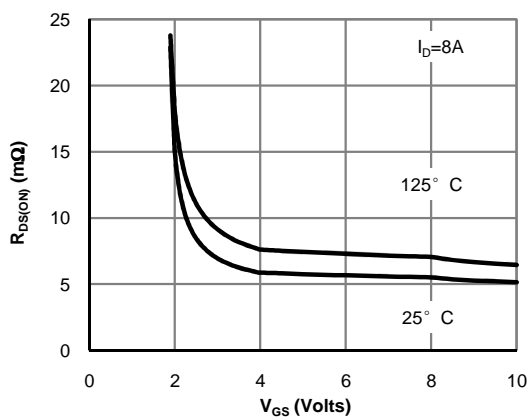
**Figure 2: Transfer Characteristics (Note E)**



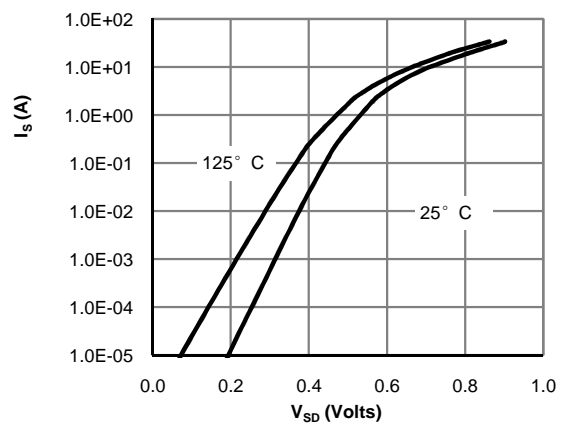
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

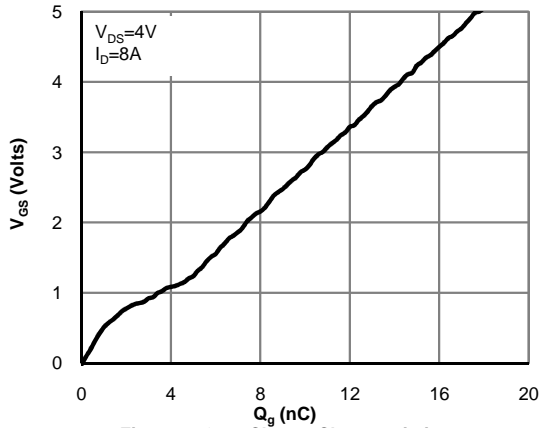


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

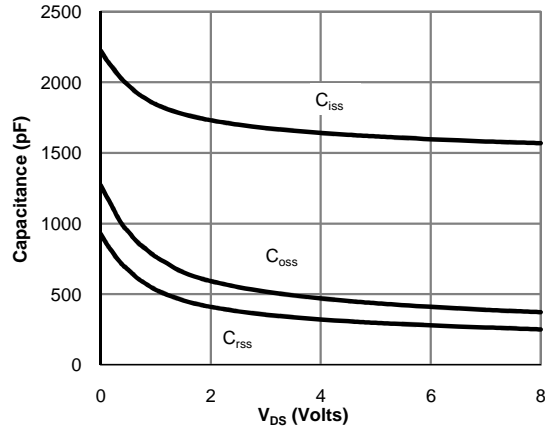


**Figure 6: Body-Diode Characteristics (Note E)**

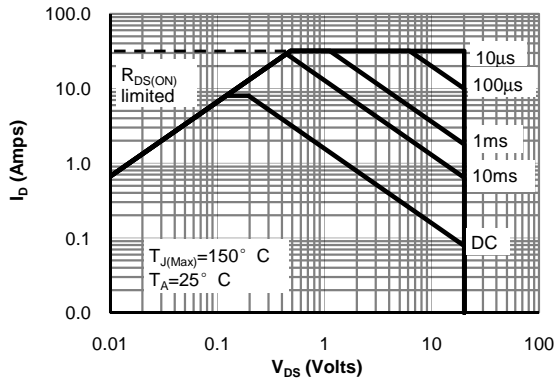
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



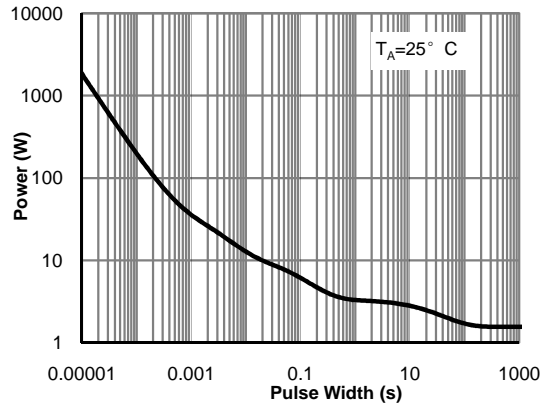
**Figure 7: Gate-Charge Characteristics**



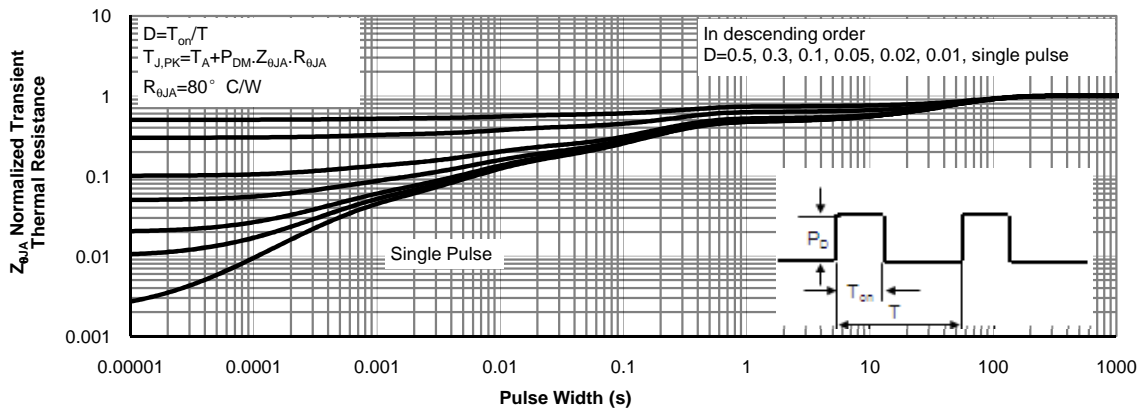
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note H)**



**Figure 12: Normalized Maximum Transient Thermal Impedance (Note H)**

**Gate Charge Test Circuit & Waveform**



**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**

