

AON6718L
N-Channel Enhancement Mode Field Effect Transistor
SRFET™
General Description

SRFET™ AON6718L uses advanced trench technology with a monolithically integrated Schottky diode to provide excellent $R_{DS(ON)}$ and low gate charge. This device is ideally suited for use as a low side switch in CPU core power conversion.

- RoHS Compliant
- Halogen Free

Features

V_{DS} (V) = 30V
 I_D = 80A (V_{GS} = 10V)
 $R_{DS(ON)} < 3.7m\Omega$ (V_{GS} = 10V)
 $R_{DS(ON)} < 5m\Omega$ (V_{GS} = 4.5V)

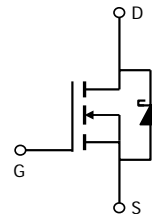
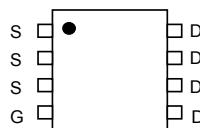
100% UIS Tested!
100% R_g Tested!

Fits SOIC8 footprint !



DFN5X6

Top View



SRFET™
 Soft Recovery MOSFET:
 Integrated Schottky Diode

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

| Parameter | Symbol | Maximum | Units |
|---|----------------|-------------------------|------------------|
| Drain-Source Voltage | V_{DS} | 30 | V |
| Gate-Source Voltage | V_{GS} | ± 20 | V |
| Continuous Drain Current ^G | I_D | $T_C=25^\circ\text{C}$ | 80 |
| | | $T_C=100^\circ\text{C}$ | 63 |
| Pulsed Drain Current ^C | I_{DM} | 210 | A |
| Continuous Drain Current | I_{DSM} | $T_A=25^\circ\text{C}$ | 19 |
| | | $T_A=70^\circ\text{C}$ | 15 |
| Avalanche Current ^C | I_{AR} | 40 | A |
| Repetitive avalanche energy $L=0.1\text{mH}$ ^C | E_{AR} | 80 | mJ |
| Power Dissipation ^B | P_D | $T_C=25^\circ\text{C}$ | 83 |
| | | $T_C=100^\circ\text{C}$ | 33 |
| Power Dissipation ^A | P_{DSM} | $T_A=25^\circ\text{C}$ | 2.5 |
| | | $T_A=70^\circ\text{C}$ | 1.6 |
| Junction and Storage Temperature Range | T_J, T_{STG} | -55 to 150 | $^\circ\text{C}$ |

Thermal Characteristics

| Parameter | Symbol | Typ | Max | Units |
|--|-----------------|---------------------|------|--------------------|
| Maximum Junction-to-Ambient ^A | $R_{\theta JA}$ | $t \leq 10\text{s}$ | 14.2 | $^\circ\text{C/W}$ |
| Maximum Junction-to-Ambient ^{A D} | | Steady-State | 42 | $^\circ\text{C/W}$ |
| Maximum Junction-to-Case | $R_{\theta JC}$ | 1.2 | 1.5 | $^\circ\text{C/W}$ |

Electrical Characteristics (T_J=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------|---------------------------------------|--|------|-------|------|-------|
| STATIC PARAMETERS | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | I _D =250μA, V _{GS} =0V | 30 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} =30V, V _{GS} =0V T _J =125°C | | 0.025 | 0.1 | mA |
| I _{GSS} | Gate-Body leakage current | V _{DS} =0V, V _{GS} = ±20V | | | 0.1 | |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} , I _D =250μA | 1.2 | 1.8 | 2.2 | V |
| I _{D(ON)} | On state drain current | V _{GS} =10V, V _{DS} =5V | 160 | | | A |
| R _{DS(ON)} | Static Drain-Source On-Resistance | V _{GS} =10V, I _D =20A T _J =125°C | | 3.1 | 3.7 | mΩ |
| | | V _{GS} =4.5V, I _D =20A | | 4.3 | 5.2 | |
| g _{FS} | Forward Transconductance | V _{DS} =5V, I _D =20A | | 87 | | S |
| V _{SD} | Diode Forward Voltage | I _S =1A, V _{GS} =0V | | 0.4 | 1 | V |
| I _S | Maximum Body-Diode Continuous Current | | | | 40 | A |
| DYNAMIC PARAMETERS | | | | | | |
| C _{iss} | Input Capacitance | V _{GS} =0V, V _{DS} =15V, f=1MHz | 2975 | 3719 | 4463 | pF |
| C _{oss} | Output Capacitance | | 485 | 693 | 900 | pF |
| C _{rss} | Reverse Transfer Capacitance | | 204 | 340 | 476 | pF |
| R _g | Gate resistance | V _{GS} =0V, V _{DS} =0V, f=1MHz | 0.28 | 0.56 | 0.84 | Ω |
| SWITCHING PARAMETERS | | | | | | |
| Q _g (10V) | Total Gate Charge | V _{GS} =10V, V _{DS} =15V, I _D =20A | 48 | 60 | 72 | nC |
| Q _g (4.5V) | Total Gate Charge | | 20 | 25 | 30 | nC |
| Q _{gs} | Gate Source Charge | | 12 | 15 | 18 | nC |
| Q _{gd} | Gate Drain Charge | | 6 | 10 | 14 | nC |
| t _{D(on)} | Turn-On Delay Time | V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω | | 9.2 | | ns |
| t _r | Turn-On Rise Time | | | 10.7 | | ns |
| t _{D(off)} | Turn-Off Delay Time | | | 40 | | ns |
| t _f | Turn-Off Fall Time | | | 12.5 | | ns |
| t _{rr} | Body Diode Reverse Recovery Time | I _F =20A, dI/dt=500A/μs | 10 | 13 | 16 | ns |
| Q _{rr} | Body Diode Reverse Recovery Charge | I _F =20A, dI/dt=500A/μs | 21 | 26.5 | 32 | nC |

A. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <30Q_s pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

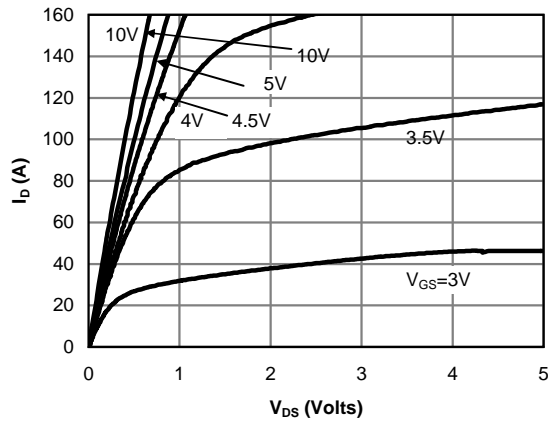


Figure 1: On-Region Characteristics (Note E)

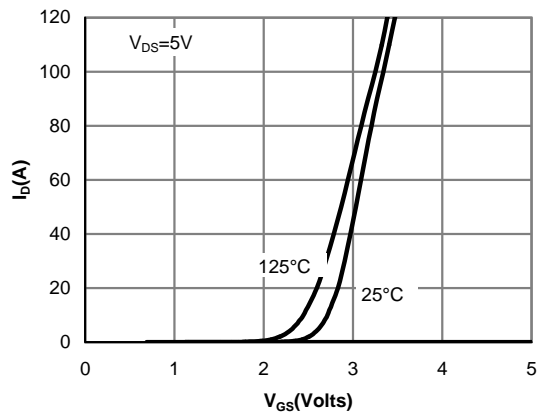


Figure 2: Transfer Characteristics (Note E)

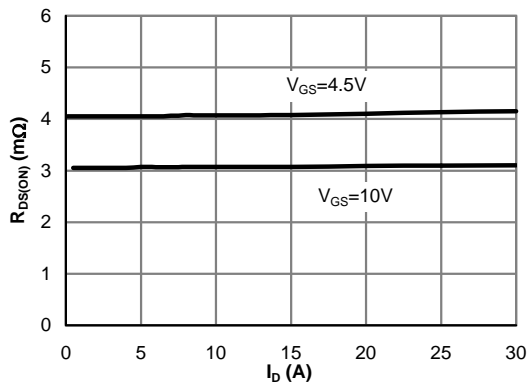


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

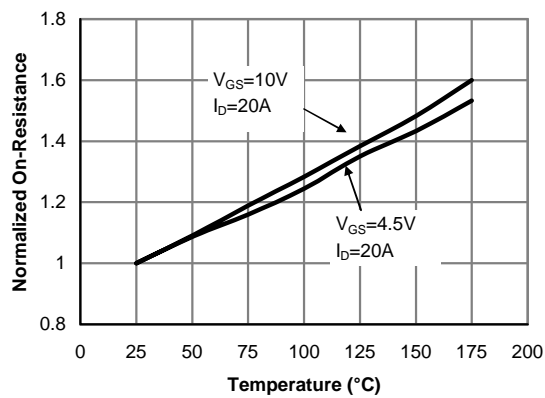


Figure 4: On-Resistance vs. Junction Temperature (Note E)

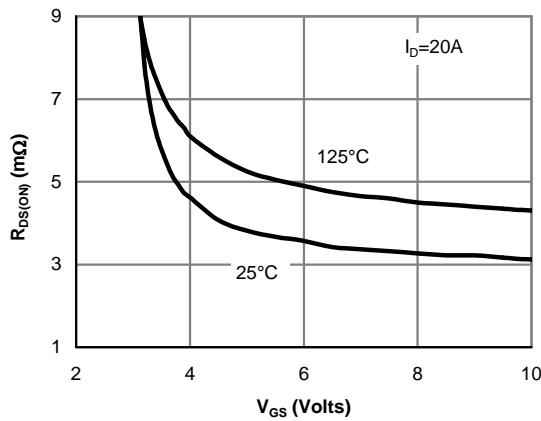


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

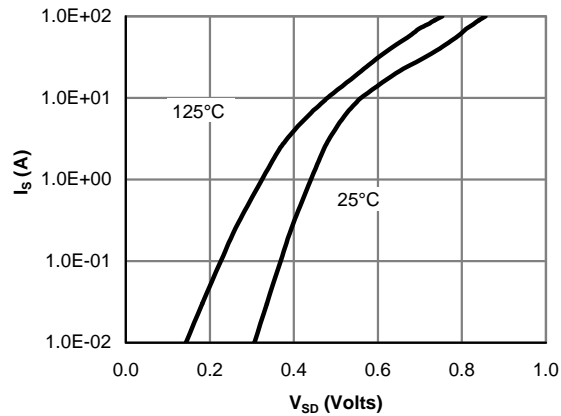


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

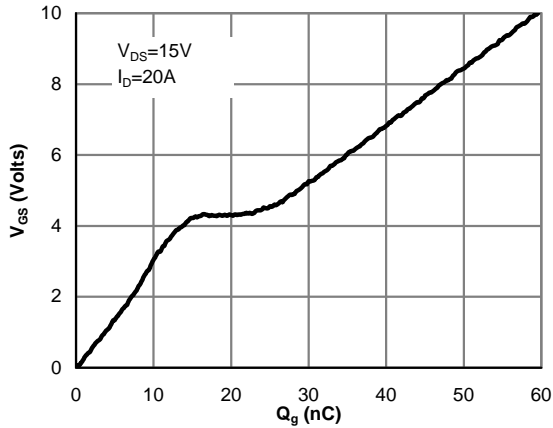


Figure 7: Gate-Charge Characteristics

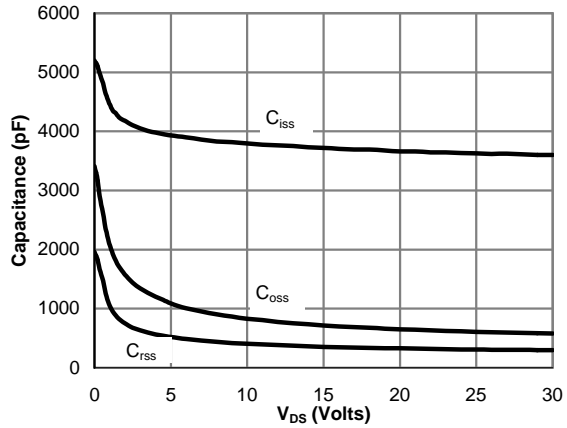


Figure 8: Capacitance Characteristics

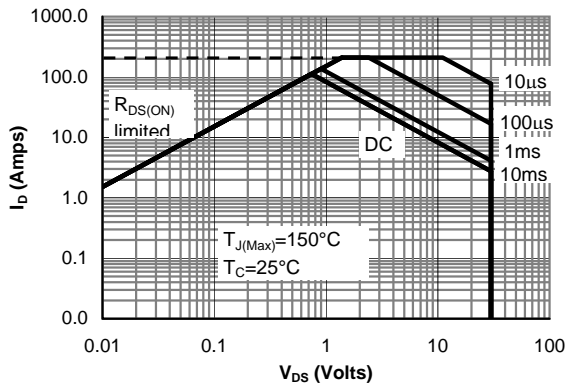


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

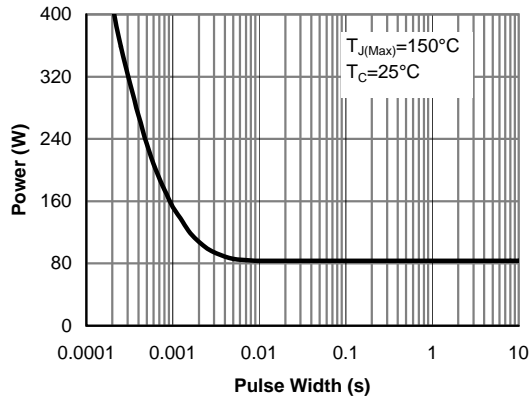


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

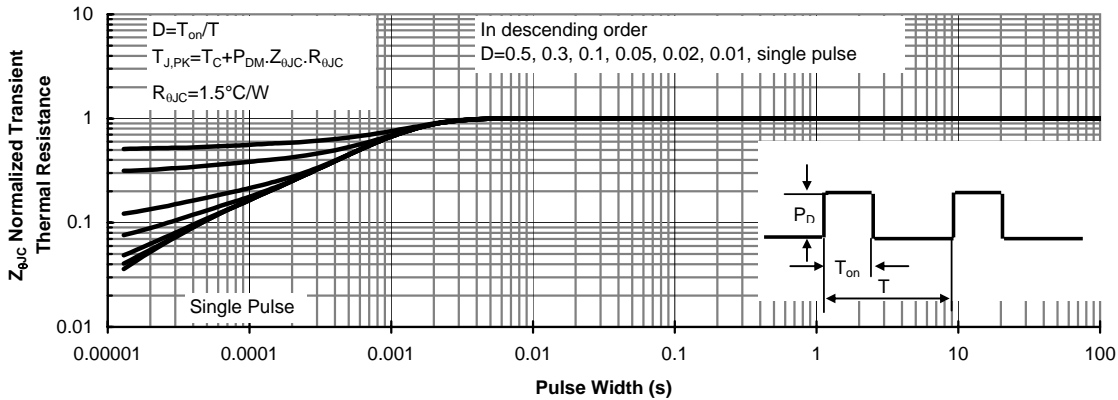


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

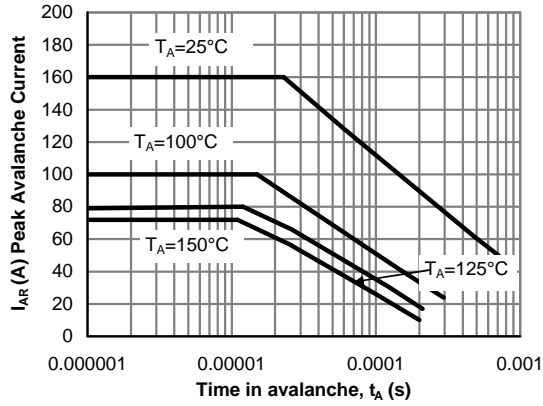


Figure 12: Single Pulse Avalanche capability (Note C)

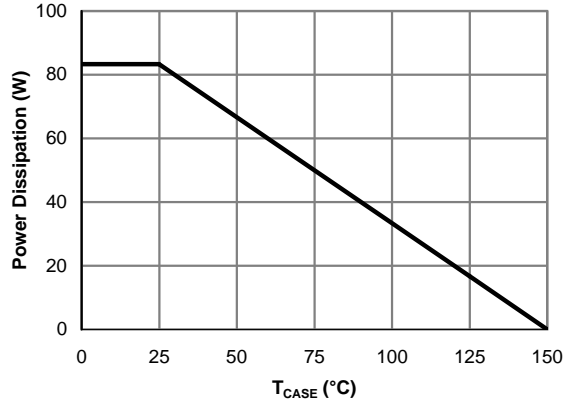


Figure 13: Power De-rating (Note F)

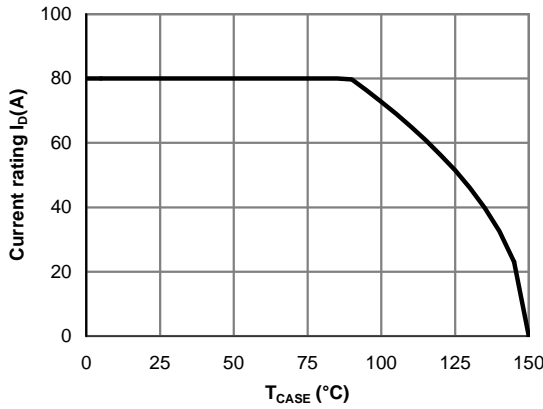


Figure 14: Current De-rating (Note F)

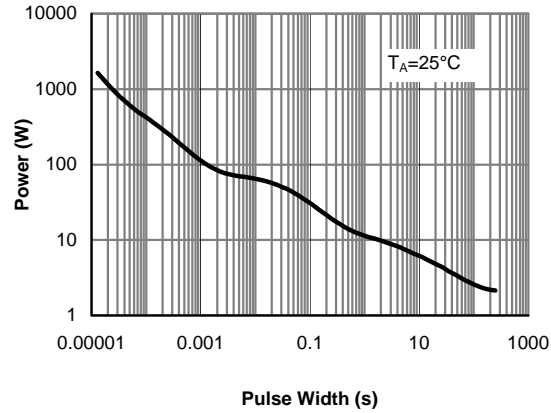


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

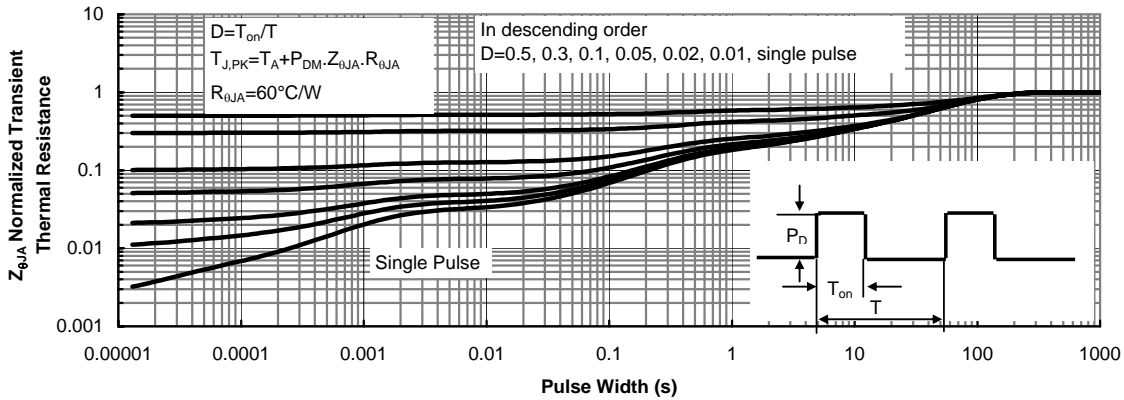


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

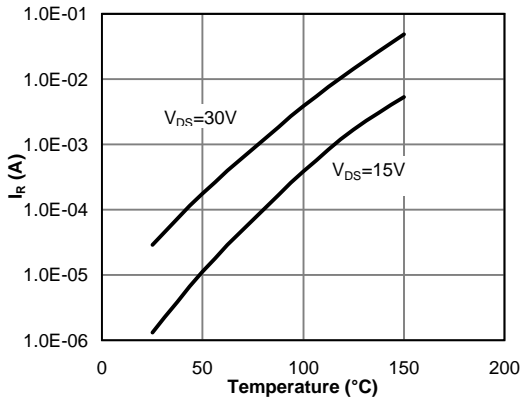


Figure 17: Diode Reverse Leakage Current vs. Junction Temperature

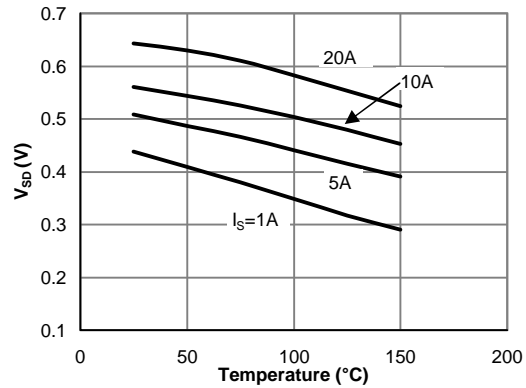


Figure 18: Diode Forward voltage vs. Junction Temperature

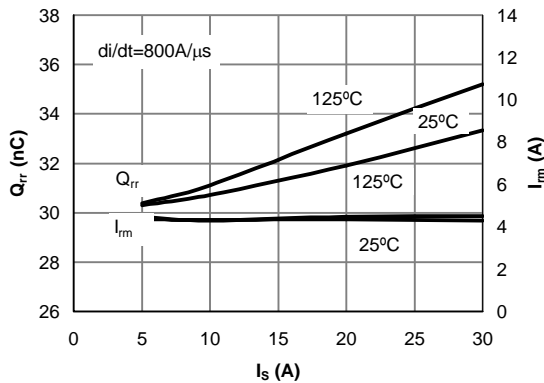


Figure 19: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

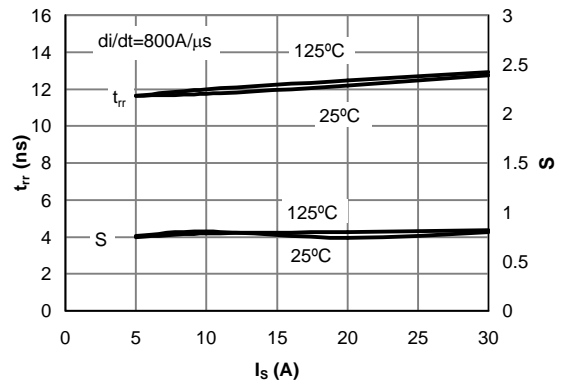


Figure 20: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current

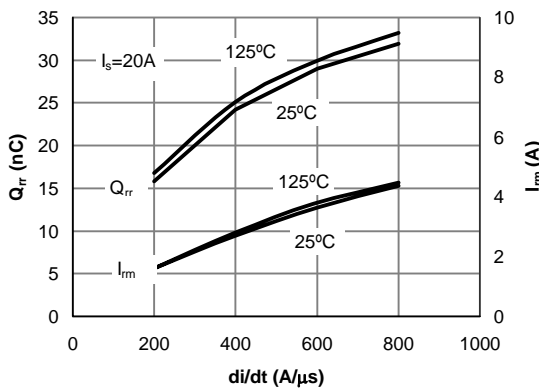


Figure 21: Diode Reverse Recovery Charge and Peak Current vs. di/dt

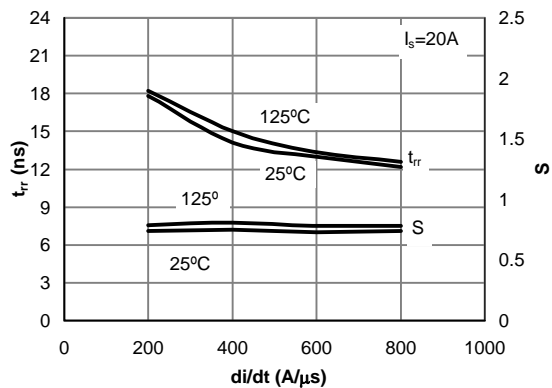
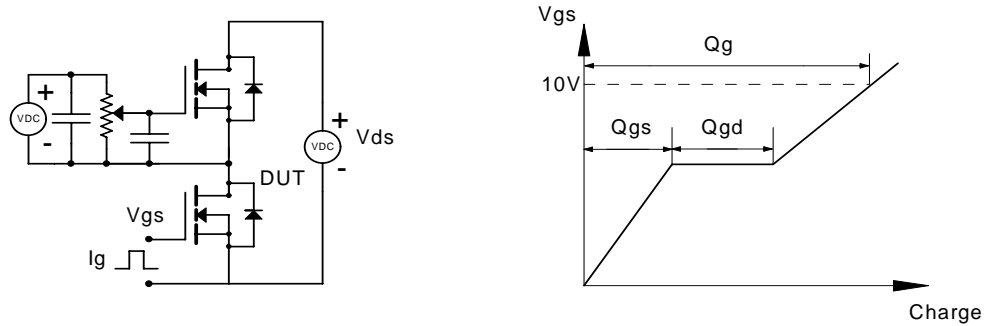
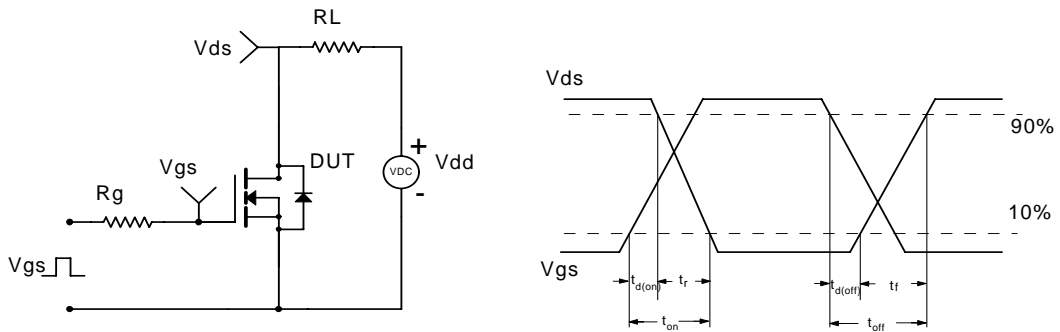


Figure 22: Diode Reverse Recovery Time and Softness Factor vs. di/dt

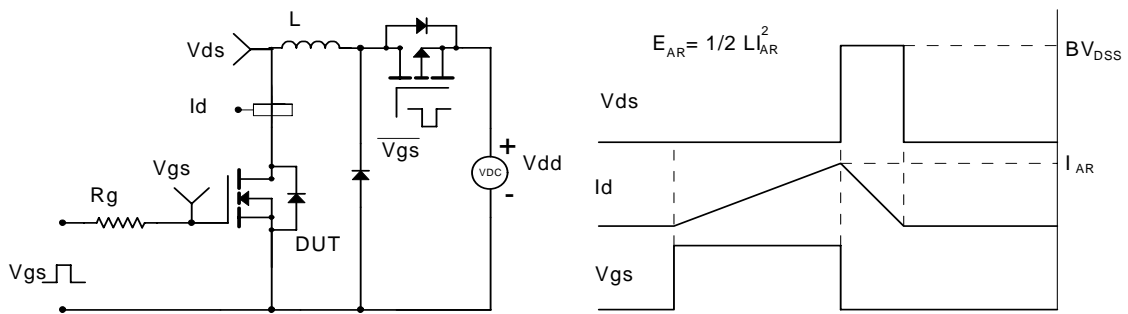
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

