

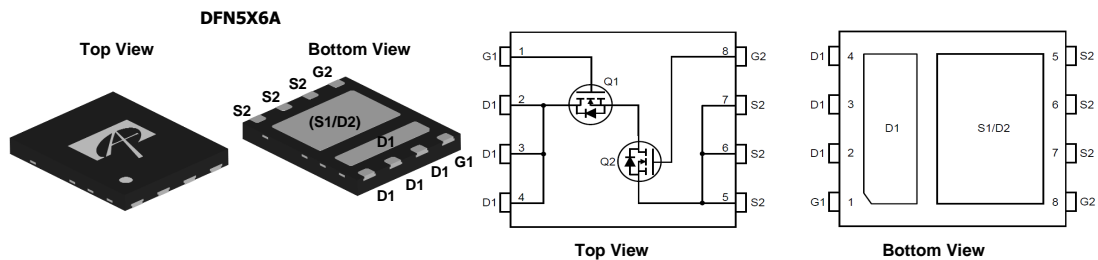
General Description

The AON6922 is designed to provide a high efficiency synchronous buck power stage with optimal layout and board space utilization. It includes two specialized MOSFETs in a dual Power DFN5x6A package. The Q1 "High Side" MOSFET is designed to minimize switching losses. The Q2 "Low Side" MOSFET is designed for low $R_{DS(ON)}$ to reduce conduction losses. The AON6922 is well suited for use in compact DC/DC converter applications.

Product Summary

| | Q1 | Q2 |
|------------------------------------|----------------|----------------|
| V_{DS} | 25V | 25V |
| I_D (at $V_{GS}=10V$) | 71A | 85A |
| $R_{DS(ON)}$ (at $V_{GS}=10V$) | <3.8m Ω | <1.4m Ω |
| $R_{DS(ON)}$ (at $V_{GS} = 4.5V$) | <4.8m Ω | <1.8m Ω |

100% UIS Tested
 100% Rg Tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

| Parameter | Symbol | Max Q1 | Max Q2 | Units |
|--|------------------|------------|--------|------------------|
| Drain-Source Voltage | V_{DS} | 25 | | V |
| Gate-Source Voltage | V_{GS} | ± 12 | | V |
| Continuous Drain Current ^G | I_D | 71 | 85 | A |
| $T_C=100^\circ\text{C}$ | | 44 | 66 | |
| Pulsed Drain Current ^C | I_{DM} | 240 | 420 | A |
| Continuous Drain Current | I_{DSM} | 18 | 31 | A |
| $T_A=70^\circ\text{C}$ | | 14 | 25 | |
| Avalanche Current ^C | I_{AS}, I_{AR} | 40 | 78 | A |
| Avalanche Energy $L=0.1\text{mH}$ ^C | E_{AS}, E_{AR} | 80 | 304 | mJ |
| Power Dissipation ^B | P_D | 31 | 104 | W |
| $T_C=100^\circ\text{C}$ | | 12.5 | 41.5 | |
| Power Dissipation ^A | P_{DSM} | 2 | 2.2 | W |
| $T_A=70^\circ\text{C}$ | | 1.3 | 1.4 | |
| Junction and Storage Temperature Range | T_J, T_{STG} | -55 to 150 | | $^\circ\text{C}$ |

Thermal Characteristics

| Parameter | Symbol | Typ Q1 | Typ Q2 | Max Q1 | Max Q2 | Units |
|--|-----------------|--------|--------|--------|--------|--------------------|
| Maximum Junction-to-Ambient ^A | $R_{\theta JA}$ | 25 | 20 | 30 | 25 | $^\circ\text{C/W}$ |
| $t \leq 10\text{s}$ | | 50 | 45 | 60 | 55 | |
| Maximum Junction-to-Ambient ^{A,D} | $R_{\theta JC}$ | 3.1 | 0.9 | 4 | 1.2 | $^\circ\text{C/W}$ |
| Steady-State | | | | | | |

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------|---------------------------------------|--|------|----------|------------|-------|
| STATIC PARAMETERS | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | I _D =250μA, V _{GS} =0V | 25 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} =25V, V _{GS} =0V T _J =55°C | | | 1 5 | μA |
| I _{GSS} | Gate-Body leakage current | V _{DS} =0V, V _{GS} = ±12V | | | 100 | nA |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} , I _D =250μA | 0.7 | 1.2 | 1.7 | V |
| I _{D(ON)} | On state drain current | V _{GS} =10V, V _{DS} =5V | 240 | | | A |
| R _{DS(ON)} | Static Drain-Source On-Resistance | V _{GS} =10V, I _D =20A T _J =125°C | | 3 4.3 | 3.8 5.4 | mΩ |
| | | V _{GS} =4.5V, I _D =20A | | 3.7 | 4.8 | |
| g _{FS} | Forward Transconductance | V _{DS} =5V, I _D =20A | | 125 | | S |
| V _{SD} | Diode Forward Voltage | I _S =1A, V _{GS} =0V | | 0.7 | 1 | V |
| I _S | Maximum Body-Diode Continuous Current | | | | 30 | A |
| DYNAMIC PARAMETERS | | | | | | |
| C _{iss} | Input Capacitance | V _{GS} =0V, V _{DS} =12.5V, f=1MHz | 1560 | 1950 | 2340 | pF |
| C _{oss} | Output Capacitance | | 530 | 755 | 980 | pF |
| C _{riss} | Reverse Transfer Capacitance | | 20 | 70 | 120 | pF |
| R _g | Gate resistance | V _{GS} =0V, V _{DS} =0V, f=1MHz | 0.7 | 1.4 | 2.1 | Ω |
| SWITCHING PARAMETERS | | | | | | |
| Q _{g(10V)} | Total Gate Charge | V _{GS} =10V, V _{DS} =12.5V, I _D =20A | 21 | 26.5 | 32 | nC |
| Q _{g(4.5V)} | Total Gate Charge | | 9 | 11.2 | 13.4 | nC |
| Q _{gs} | Gate Source Charge | | | 2.7 | | nC |
| Q _{gd} | Gate Drain Charge | | | 4 | | nC |
| t _{D(on)} | Turn-On DelayTime | V _{GS} =10V, V _{DS} =12.5V, R _L =1.25Ω, R _{GEN} =3Ω | | 5.5 | | ns |
| t _r | Turn-On Rise Time | | | 3.5 | | ns |
| t _{D(off)} | Turn-Off DelayTime | | | 30 | | ns |
| t _f | Turn-Off Fall Time | | | 4 | | ns |
| t _{rr} | Body Diode Reverse Recovery Time | I _F =20A, dI/dt=500A/μs | 12 | 15 | 18 | ns |
| Q _{rr} | Body Diode Reverse Recovery Charge | I _F =20A, dI/dt=500A/μs | 20 | 25 | 30 | nC |

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating g.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.

COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

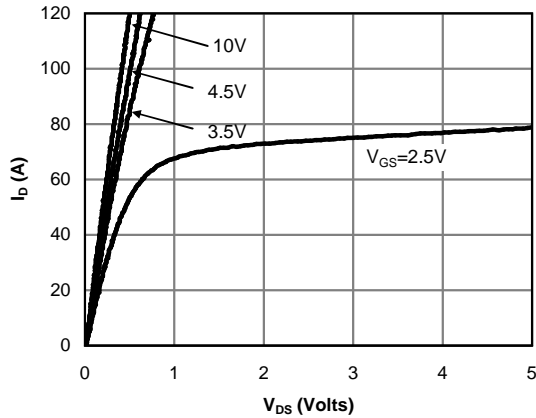


Fig 1: On-Region Characteristics (Note E)

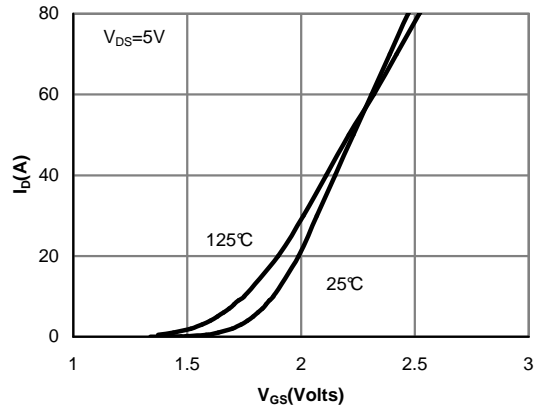


Figure 2: Transfer Characteristics (Note E)

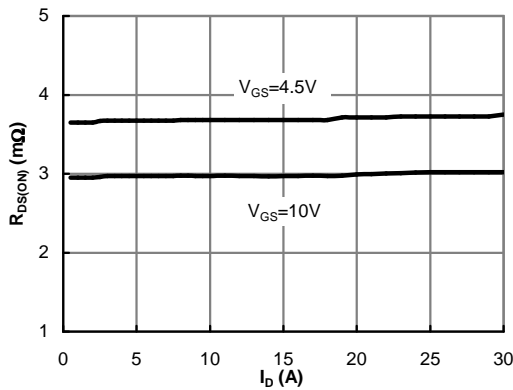


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

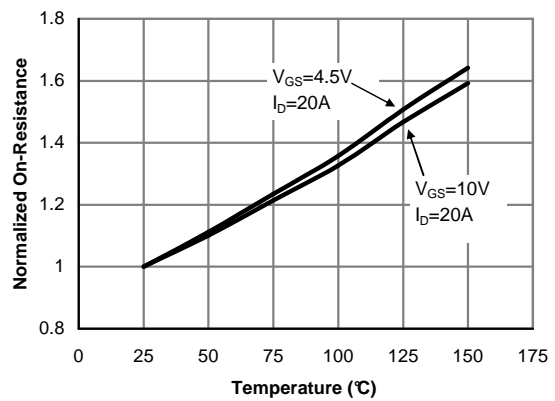


Figure 4: On-Resistance vs. Junction Temperature (Note E)

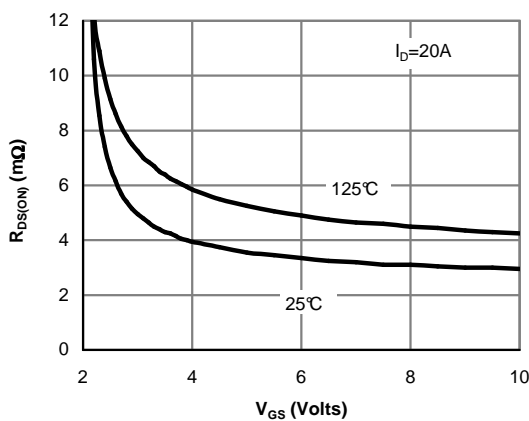


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

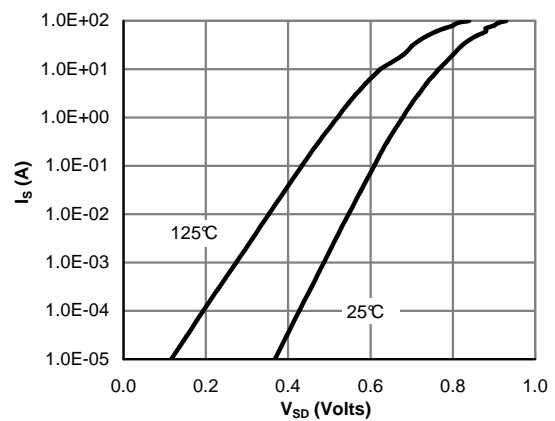


Figure 6: Body-Diode Characteristics (Note E)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

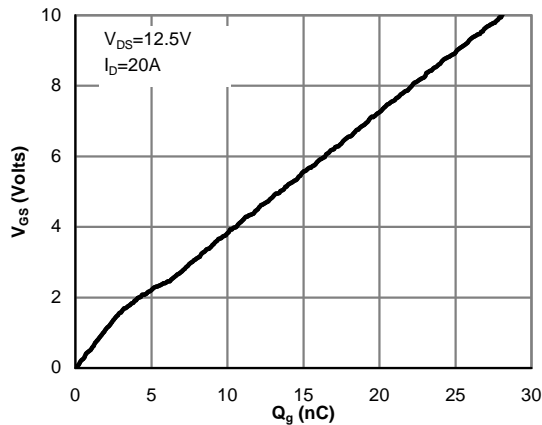


Figure 7: Gate-Charge Characteristics

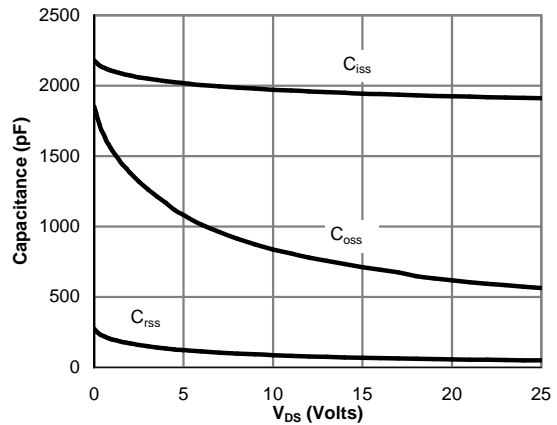


Figure 8: Capacitance Characteristics

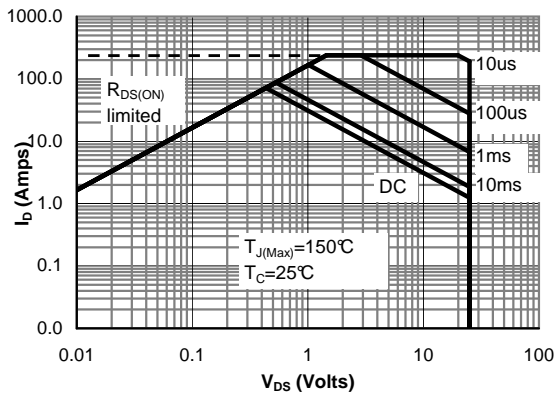


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

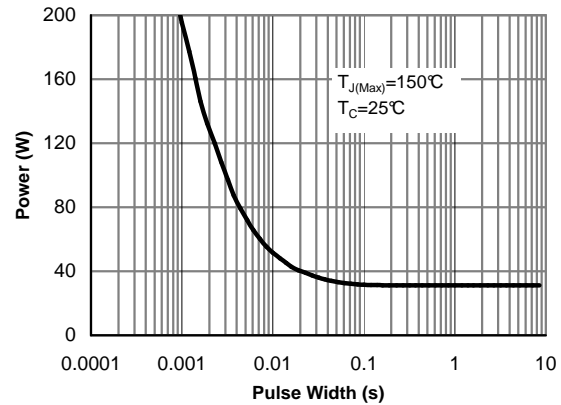


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

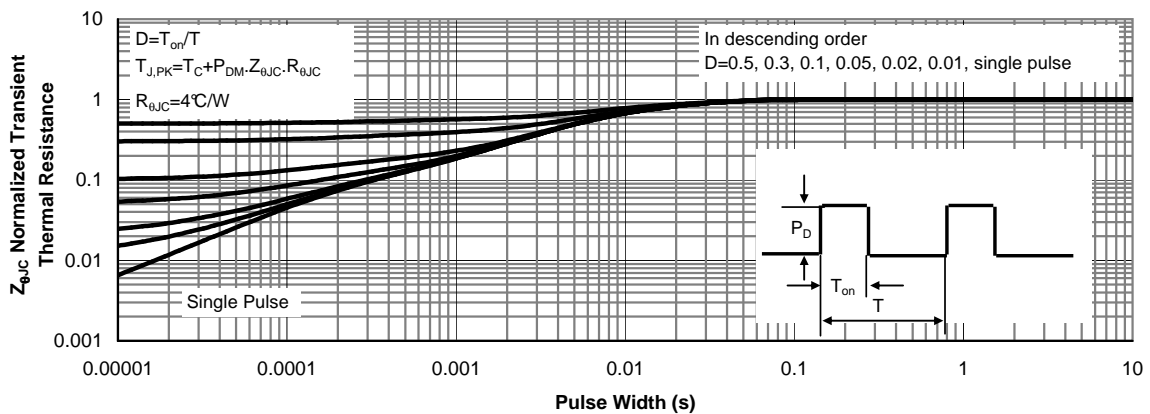


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

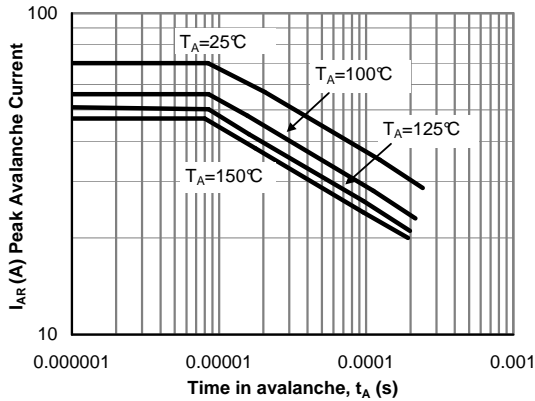


Figure 12: Single Pulse Avalanche capability (Note C)

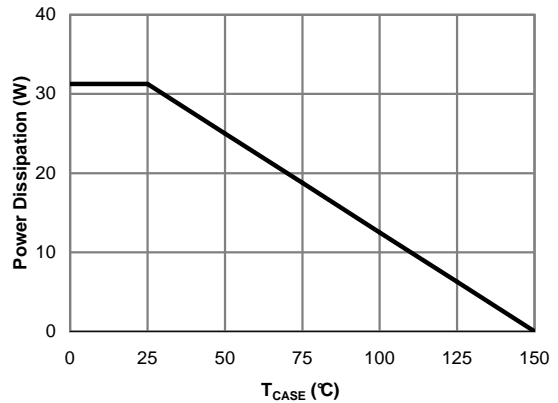


Figure 13: Power De-rating (Note F)

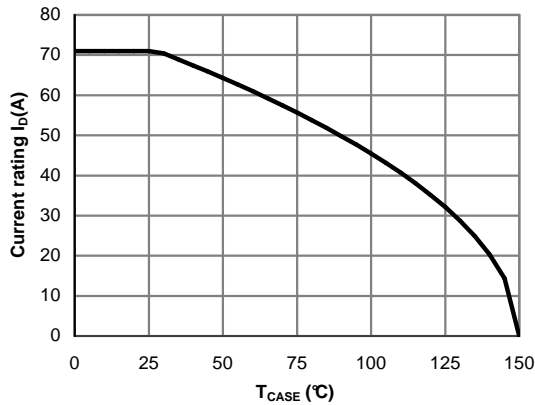


Figure 14: Current De-rating (Note F)

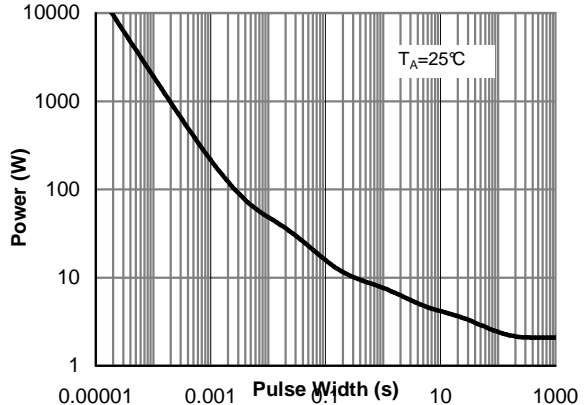


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

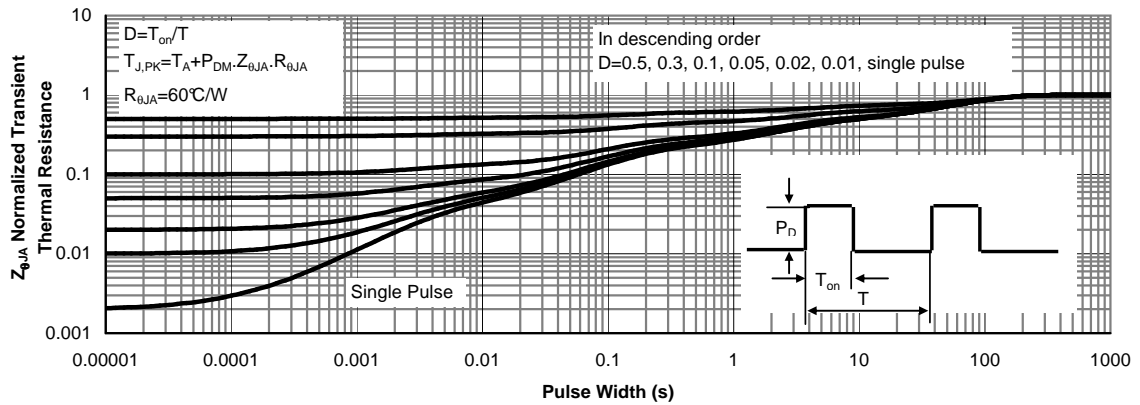


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------|--|---|------|-------------|----------|-------|
| STATIC PARAMETERS | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | I _D =250μA, V _{GS} =0V | 25 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} =25V, V _{GS} =0V T _J =55°C | | | 1 5 | μA |
| I _{GSS} | Gate-Body leakage current | V _{DS} =0V, V _{GS} = ±12V | | | 100 | nA |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} , I _D =250μA | 0.7 | 1.2 | 1.7 | V |
| I _{D(ON)} | On state drain current | V _{GS} =10V, V _{DS} =5V | 420 | | | A |
| R _{DS(ON)} | Static Drain-Source On-Resistance | V _{GS} =10V, I _D =20A T _J =125°C | | 1.15 1.6 | 1.4 2 | mΩ |
| | | V _{GS} =4.5V, I _D =20A | | 1.4 | 1.8 | |
| g _{FS} | Forward Transconductance | V _{DS} =5V, I _D =20A | | 135 | | S |
| V _{SD} | Diode Forward Voltage | I _S =1A, V _{GS} =0V | | 0.65 | 1 | V |
| I _S | Maximum Body-Diode Continuous Current ^G | | | | 85 | A |
| DYNAMIC PARAMETERS | | | | | | |
| C _{iss} | Input Capacitance | V _{GS} =0V, V _{DS} =12.5V, f=1MHz | 4550 | 5690 | 6830 | pF |
| C _{oss} | Output Capacitance | | 1730 | 2470 | 3210 | pF |
| C _{riss} | Reverse Transfer Capacitance | | 50 | 165 | 280 | pF |
| R _g | Gate resistance | V _{GS} =0V, V _{DS} =0V, f=1MHz | 0.4 | 0.8 | 1.2 | Ω |
| SWITCHING PARAMETERS | | | | | | |
| Q _{g(10V)} | Total Gate Charge | V _{GS} =10V, V _{DS} =12.5V, I _D =20A | 52 | 65 | 78 | nC |
| Q _{g(4.5V)} | Total Gate Charge | | 20 | 26 | 32 | nC |
| Q _{gs} | Gate Source Charge | | | 7.4 | | nC |
| Q _{gd} | Gate Drain Charge | | | 5.7 | | nC |
| t _{D(on)} | Turn-On DelayTime | V _{GS} =10V, V _{DS} =12.5V, R _L =0.6Ω, R _{GEN} =3Ω | | 9 | | ns |
| t _r | Turn-On Rise Time | | | 4.5 | | ns |
| t _{D(off)} | Turn-Off DelayTime | | | 60 | | ns |
| t _f | Turn-Off Fall Time | | | 8 | | ns |
| t _{rr} | Body Diode Reverse Recovery Time | I _F =20A, dI/dt=500A/μs | 19 | 24.5 | 30 | ns |
| Q _{rr} | Body Diode Reverse Recovery Charge | I _F =20A, dI/dt=500A/μs | 55 | 68 | 82 | nC |

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating g.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

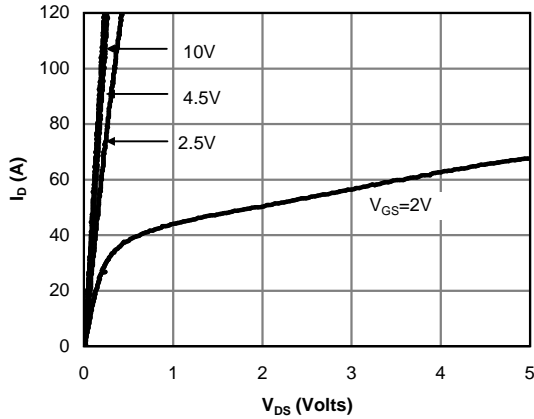


Fig 1: On-Region Characteristics (Note E)

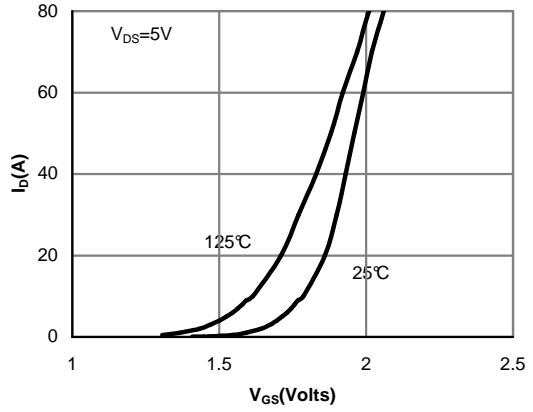


Figure 2: Transfer Characteristics (Note E)

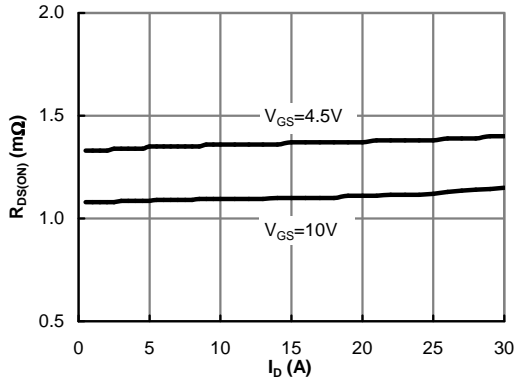


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

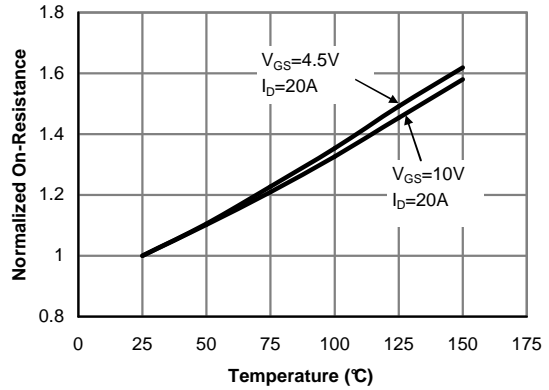


Figure 4: On-Resistance vs. Junction Temperature (Note E)

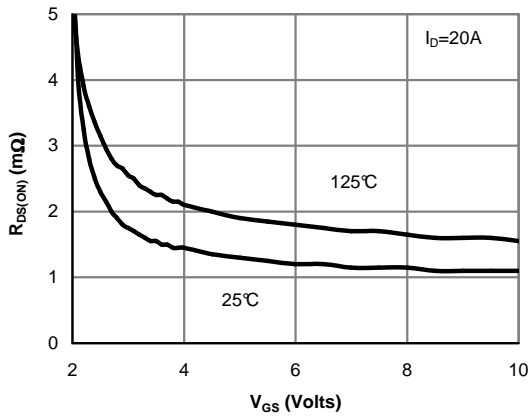


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

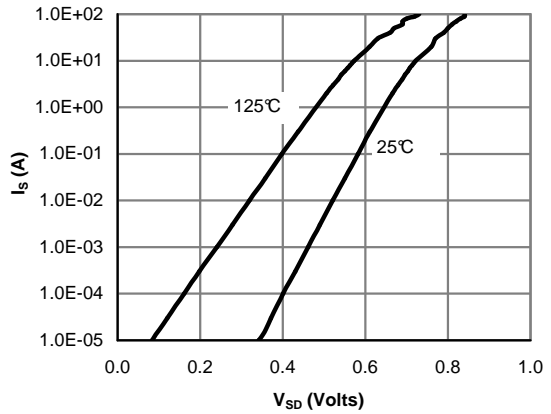


Figure 6: Body-Diode Characteristics (Note E)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

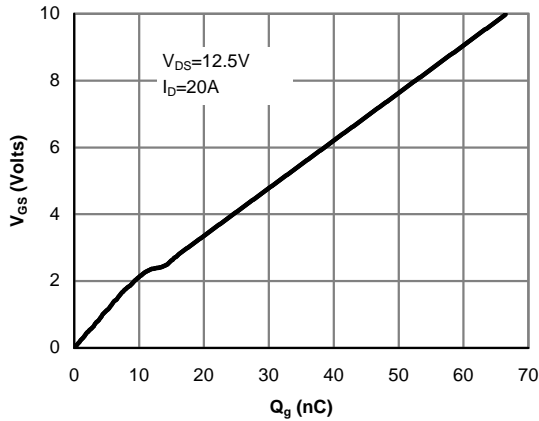


Figure 7: Gate-Charge Characteristics

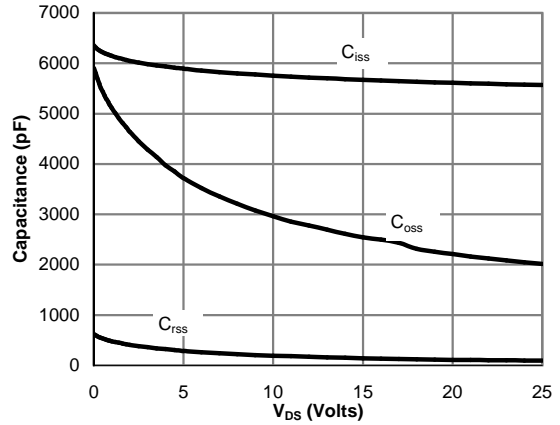


Figure 8: Capacitance Characteristics

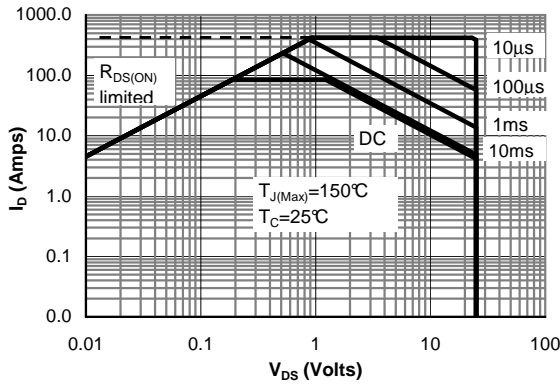


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

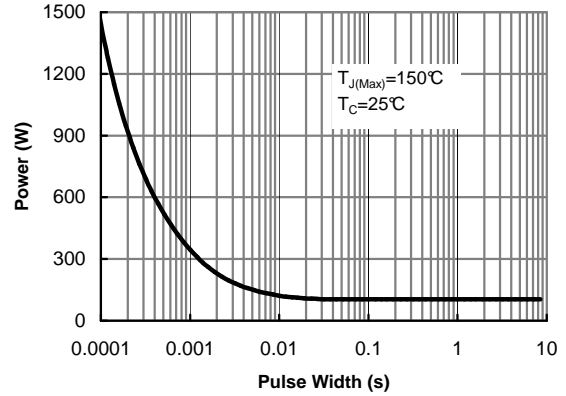


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

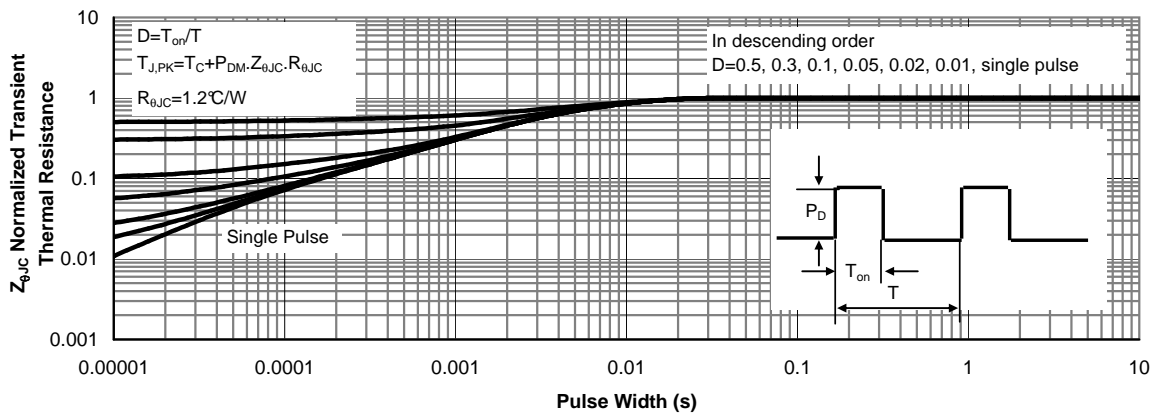


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

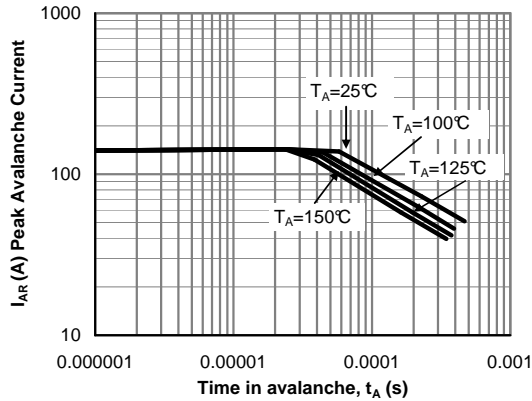


Figure 12: Single Pulse Avalanche capability (Note C)

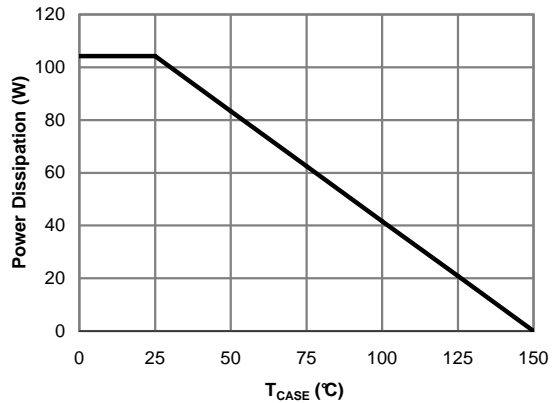


Figure 13: Power De-rating (Note F)

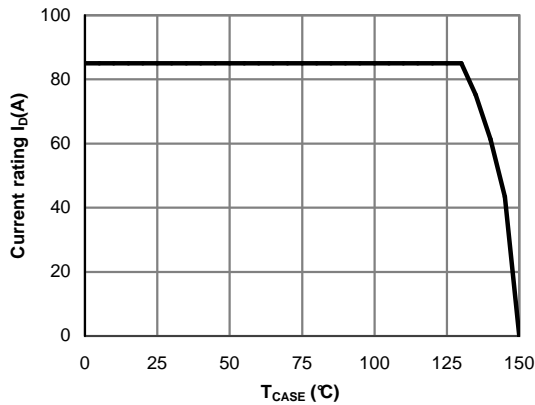


Figure 14: Current De-rating (Note F)

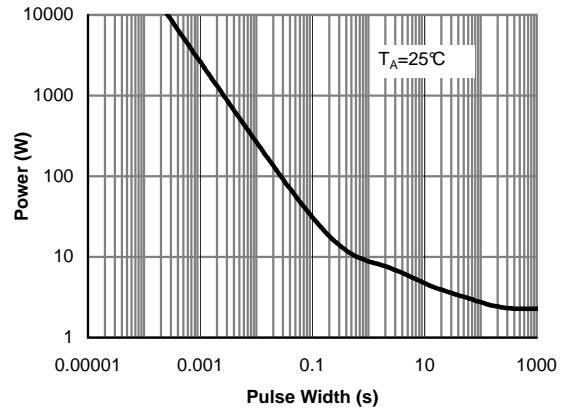


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note G)

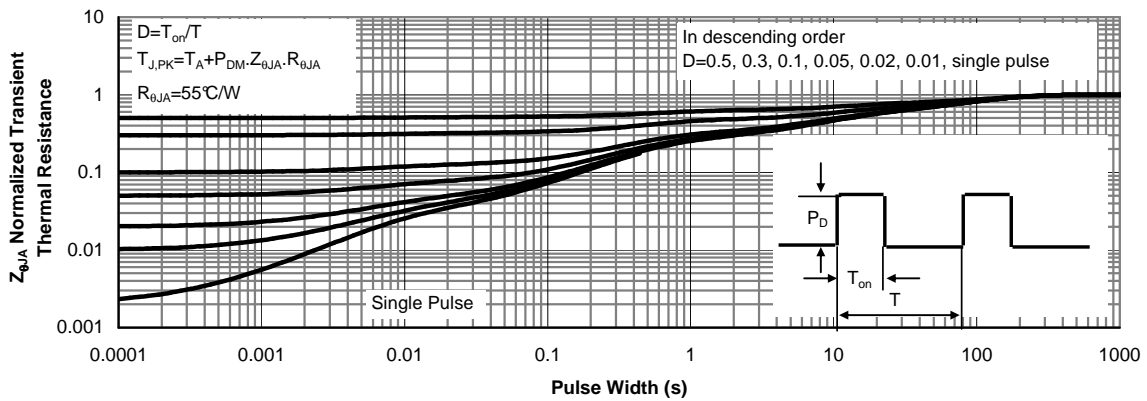
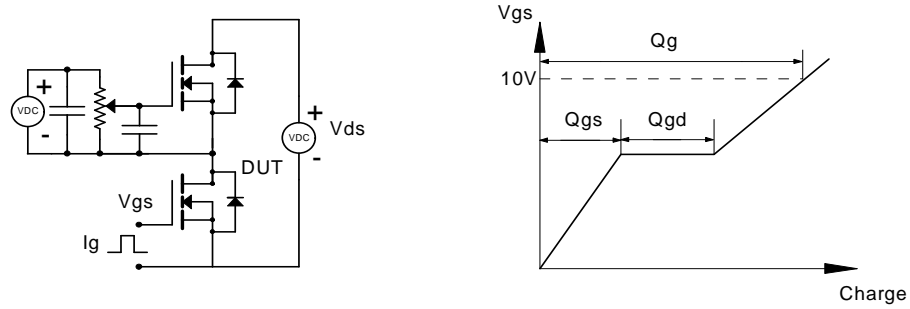
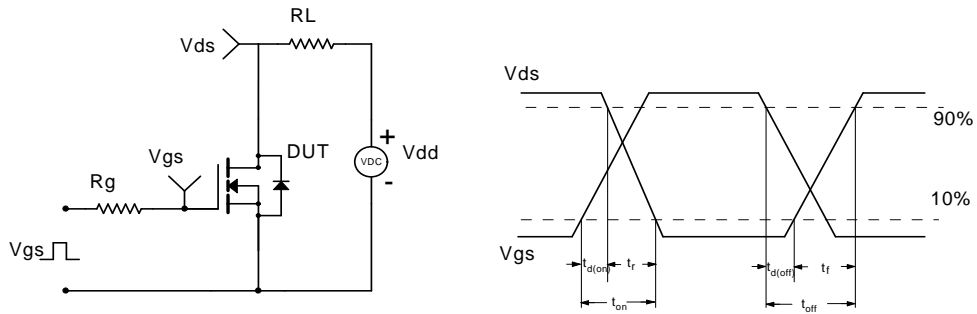


Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

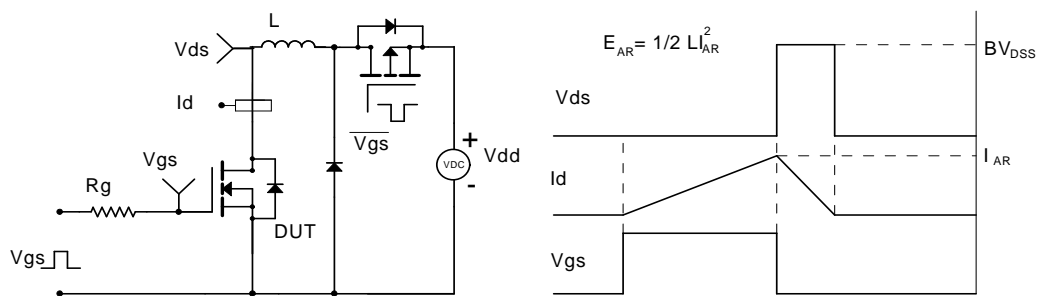
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

