

General Description

- Pch+Nch Complementary MOSFET
- Trench Power MOSFET
- Low $R_{DS(ON)}$
- Low Gate Charge
- Excellent Thermal Performance
- RoHS and Halogen Free Compliant

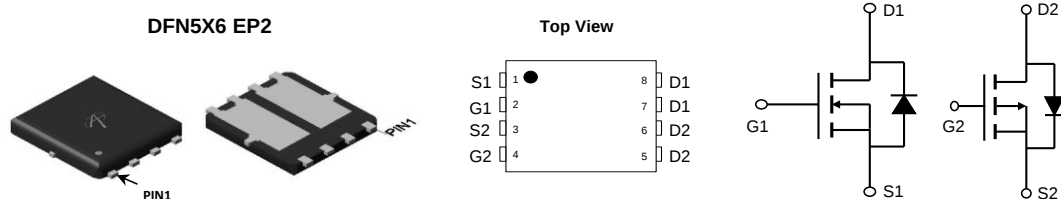
Applications

- Motor Drive
- DC-FAN

Product Summary

	Q1	Q2
V_{DS}	30V	-30V
I_D (at $V_{GS}=10V$)	16A	-16A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 14m Ω	< 12m Ω
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 18m Ω	< 19.5m Ω

100% UIS Tested
100% Rg Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOND32324	DFN 5x6	Tape & Reel	3000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max Q1	Max Q2	Units
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	± 20	± 25	V
Continuous Drain Current ^G	I_D	16	-16	A
$T_C=25^\circ\text{C}$		16	-16	
$T_C=100^\circ\text{C}$				
Pulsed Drain Current ^C	I_{DM}	50	-65	A
Continuous Drain Current	I_{DSM}	13	-15	A
$T_A=25^\circ\text{C}$		10	-12	
$T_A=70^\circ\text{C}$				
Avalanche Current ^C	I_{AS}	22	33	A
Avalanche energy $L=0.1\text{mH}$ ^C	E_{AS}	24	54	mJ
Power Dissipation ^B	P_D	12.5	30	W
$T_C=25^\circ\text{C}$		5	12	
$T_C=100^\circ\text{C}$				
Power Dissipation ^A	P_{DSM}	3.5	4.1	W
$T_A=25^\circ\text{C}$		2.2	2.6	
$T_A=70^\circ\text{C}$				
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	25	20	35	30	$^\circ\text{C/W}$
$t \leq 10\text{s}$						
Maximum Junction-to-Ambient ^{A D}	$R_{\theta JA}$	50	48	70	65	$^\circ\text{C/W}$
Steady-State						
Maximum Junction-to-Case	$R_{\theta JC}$	7	3.5	10	4.2	$^\circ\text{C/W}$
Steady-State						

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	ID=250μA, VGS=0V	30			V
IDSS	Zero Gate Voltage Drain Current	VDS=30V, VGS=0V TJ=55°C			1 5	μA
IGSS	Gate-Body leakage current	VDS=0V, VGS=±20V			±100	nA
VGS(th)	Gate Threshold Voltage	VDS=VGS, ID=250μA	1.5	1.9	2.5	V
RDS(on)	Static Drain-Source On-Resistance	VGS=10V, ID=12A TJ=125°C		11 16	14 20	mΩ
		VGS=4.5V, ID=10A		14	18	mΩ
gFS	Forward Transconductance	VDS=5V, ID=12A		43		S
VSD	Diode Forward Voltage	IS=1A, VGS=0V		0.75	1	V
IS	Maximum Body-Diode Continuous Current				10	A
DYNAMIC PARAMETERS						
Ciss	Input Capacitance	VGS=0V, VDS=15V, f=1MHz		760		pF
Coss	Output Capacitance			125		pF
Crss	Reverse Transfer Capacitance			70		pF
Rg	Gate resistance	f=1MHz	0.8	1.6	2.4	Ω
SWITCHING PARAMETERS						
Qg(10V)	Total Gate Charge	VGS=10V, VDS=15V, ID=12A		14	20	nC
Qg(4.5V)	Total Gate Charge			6.6	10	nC
Qgs	Gate Source Charge			2.4		nC
Qgd	Gate Drain Charge			3		nC
tD(on)	Turn-On DelayTime	VGS=10V, VDS=15V, RL=1.25Ω, RGEN=3Ω		4.4		ns
tr	Turn-On Rise Time			9		ns
tD(off)	Turn-Off DelayTime			17		ns
tf	Turn-Off Fall Time			6		ns
trr	Body Diode Reverse Recovery Time	IF=12A, di/dt=500A/μs		7		ns
Qrr	Body Diode Reverse Recovery Charge	IF=12A, di/dt=500A/μs		8		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO MAKE CHANGES TO PRODUCT SPECIFICATIONS WITHOUT NOTICE. IT IS THE RESPONSIBILITY OF THE CUSTOMER TO EVALUATE SUITABILITY OF THE PRODUCT FOR THEIR INTENDED APPLICATION. CUSTOMER SHALL COMPLY WITH APPLICABLE LEGAL REQUIREMENTS, INCLUDING ALL APPLICABLE EXPORT CONTROL RULES, REGULATIONS AND LIMITATIONS.

AOS' products are provided subject to AOS' terms and conditions of sale which are set forth at:

http://www.aosmd.com/terms_and_conditions_of_sale

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

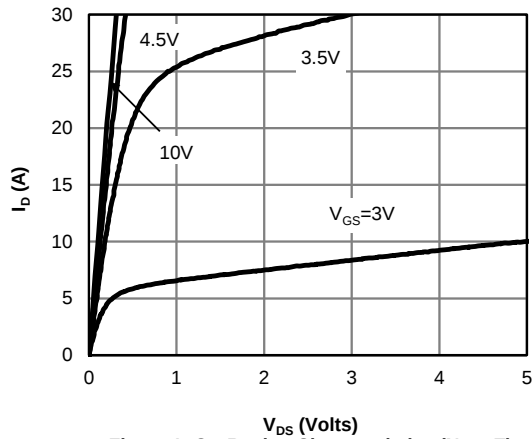


Figure 1: On-Region Characteristics (Note E)

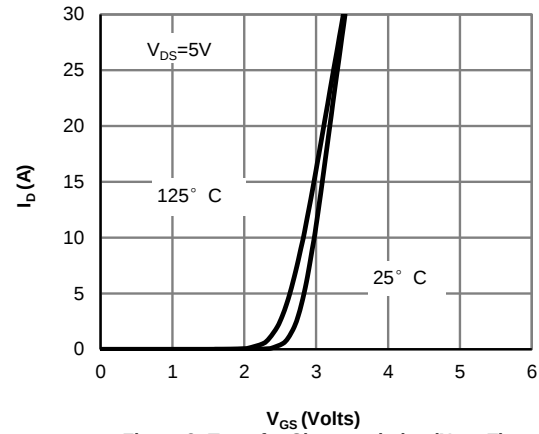


Figure 2: Transfer Characteristics (Note E)

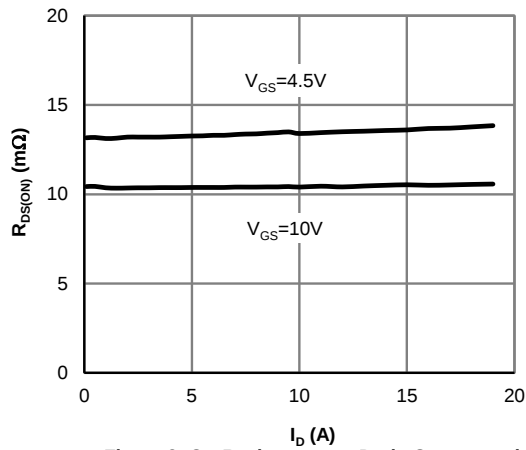


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

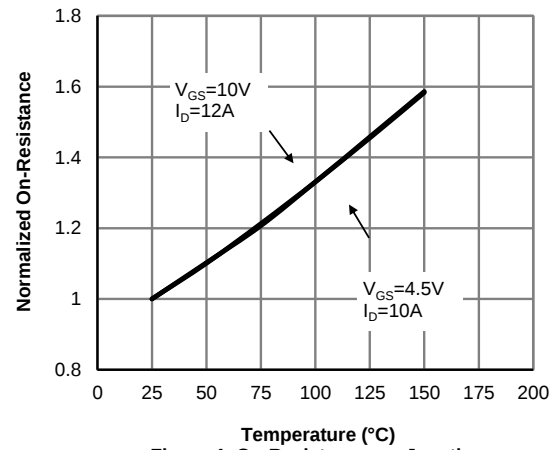


Figure 4: On-Resistance vs. Junction Temperature (Note E)

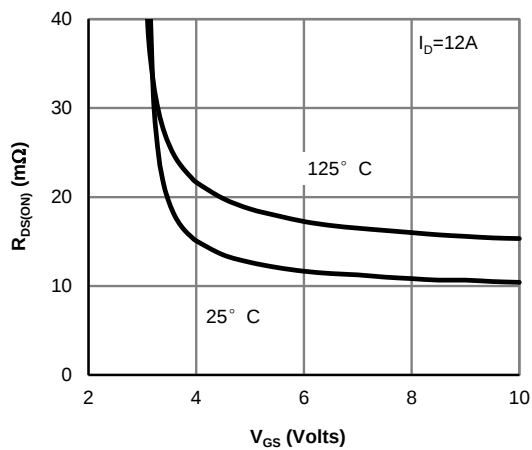


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

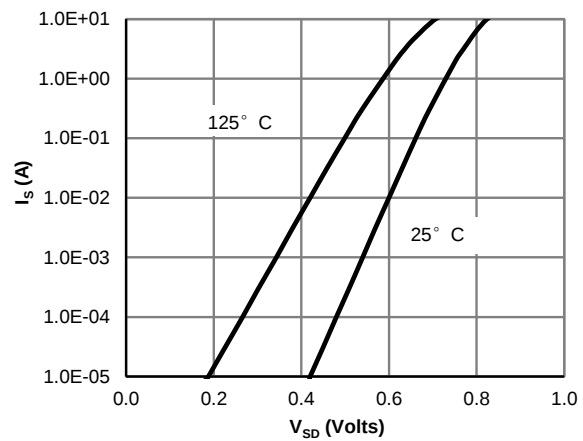
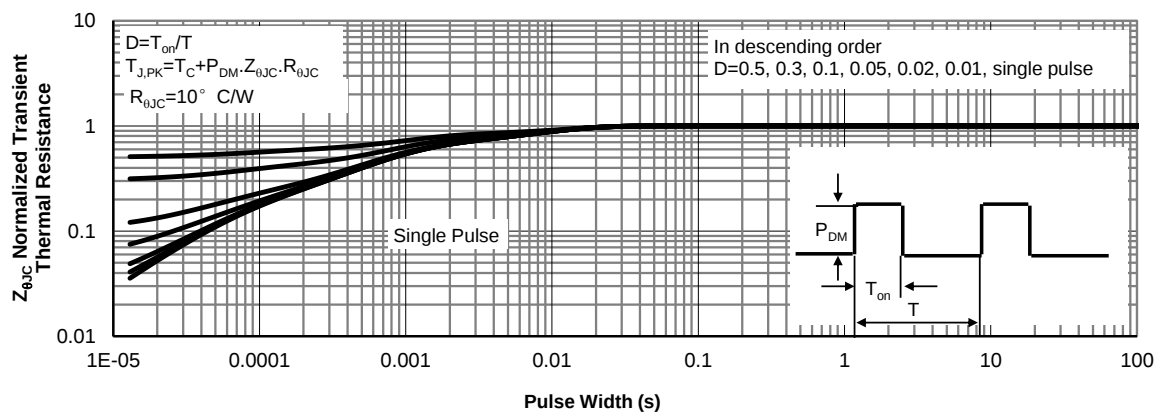
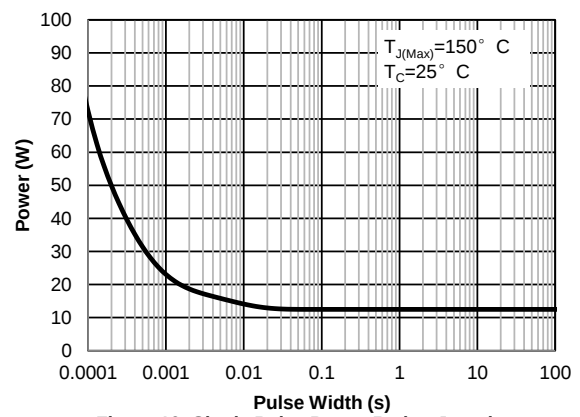
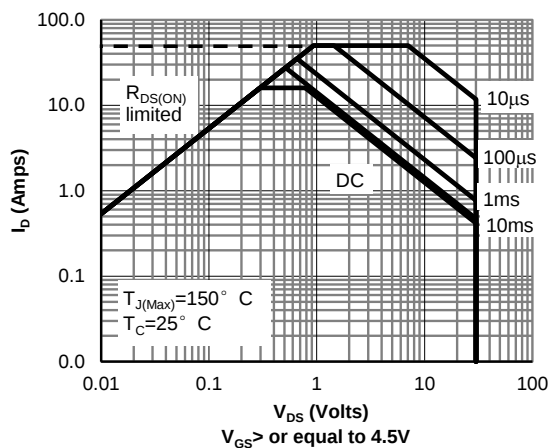
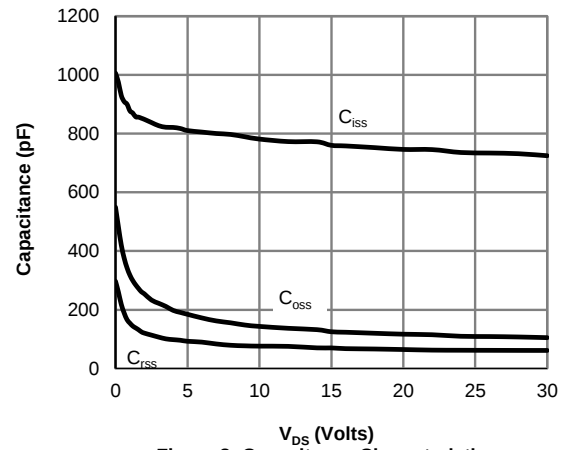
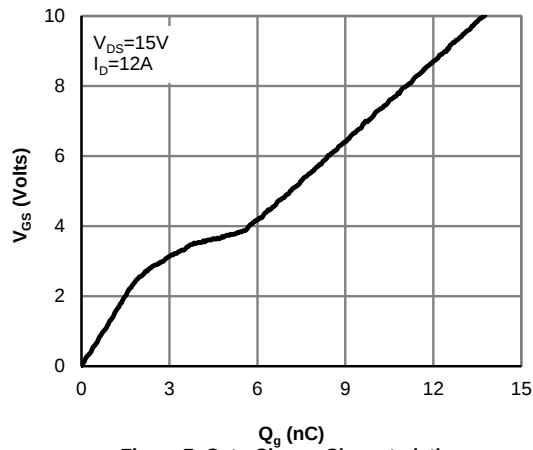
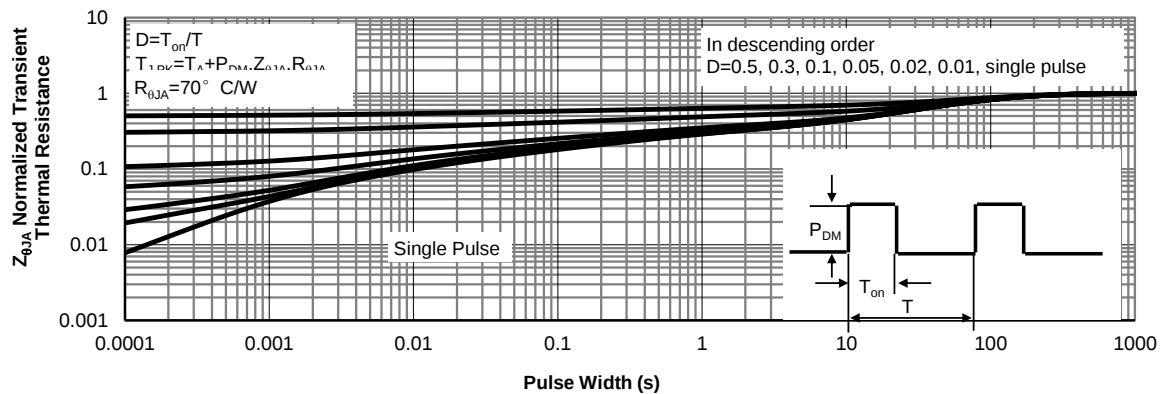
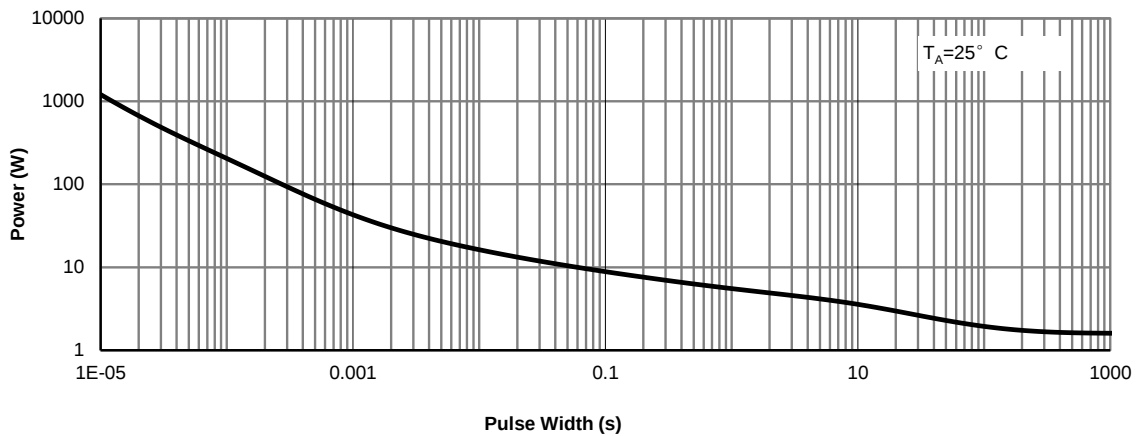
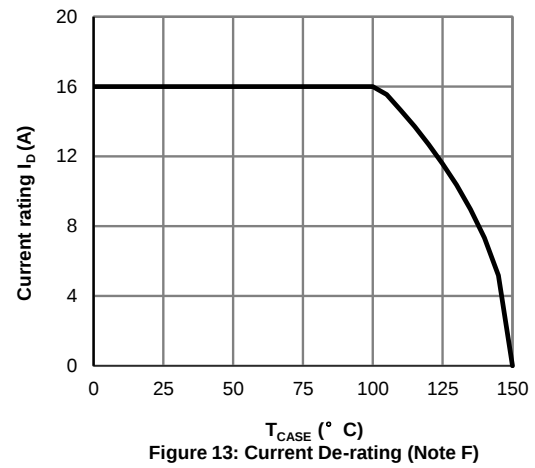
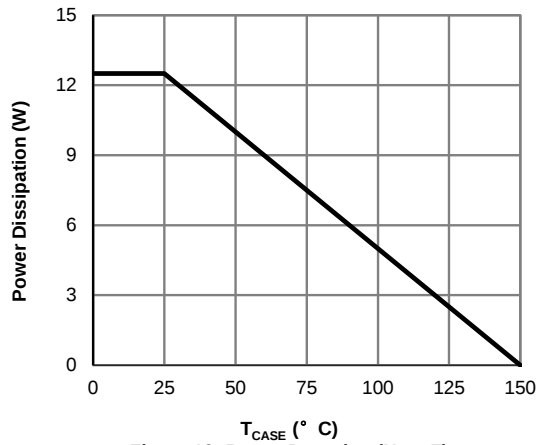


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±25V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.3	-1.8	-2.3	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-16A T _J =125°C		10 14	12 16.8	mΩ
		V _{GS} =-4.5V, I _D =-12A		15.4	19.5	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-16A		43		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.7	-1	V
I _S	Maximum Body-Diode Continuous Current ^G				-16	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz		1995		pF
C _{oss}	Output Capacitance			300		pF
C _{rss}	Reverse Transfer Capacitance			260		pF
R _g	Gate resistance	f=1MHz		4.5	9	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =-10V, V _{DS} =-15V, I _D =-16A		35	50	nC
Q _{g(4.5V)}	Total Gate Charge			17	25	nC
Q _{gs}	Gate Source Charge			5.7		nC
Q _{gd}	Gate Drain Charge			8.8		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-15V, R _L =0.9Ω, R _{GEN} =3Ω		11		ns
t _r	Turn-On Rise Time			7.5		ns
t _{D(off)}	Turn-Off DelayTime			43.5		ns
t _f	Turn-Off Fall Time			17.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-16A, di/dt=500A/μs		13.3		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-16A, di/dt=500A/μs		20		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO MAKE CHANGES TO PRODUCT SPECIFICATIONS WITHOUT NOTICE. IT IS THE RESPONSIBILITY OF THE CUSTOMER TO EVALUATE SUITABILITY OF THE PRODUCT FOR THEIR INTENDED APPLICATION. CUSTOMER SHALL COMPLY WITH APPLICABLE LEGAL REQUIREMENTS, INCLUDING ALL APPLICABLE EXPORT CONTROL RULES, REGULATIONS AND LIMITATIONS.

AOS' products are provided subject to AOS' terms and conditions of sale which are set forth at:

http://www.aosmd.com/terms_and_conditions_of_sale

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

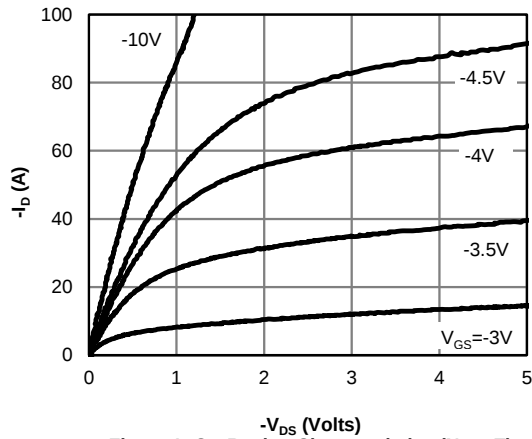


Figure 1: On-Region Characteristics (Note E)

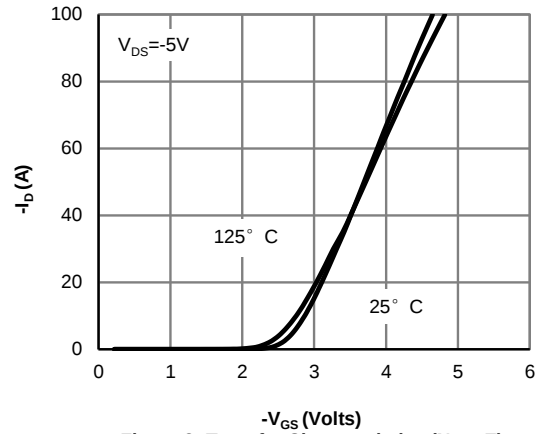


Figure 2: Transfer Characteristics (Note E)

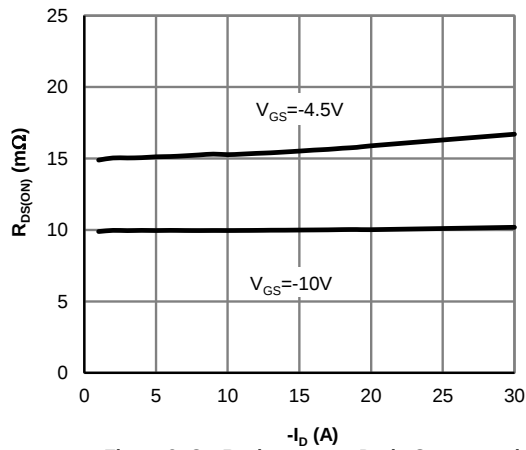


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

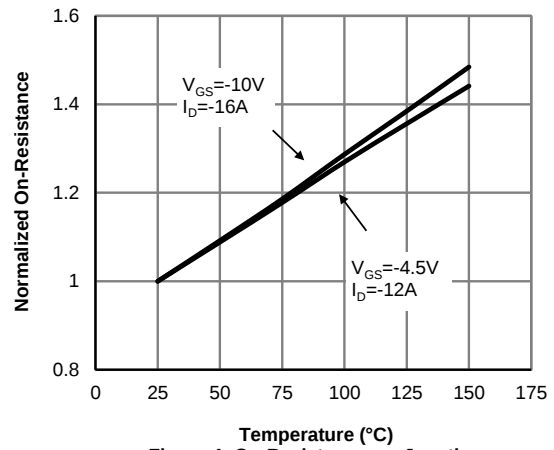


Figure 4: On-Resistance vs. Junction Temperature (Note E)

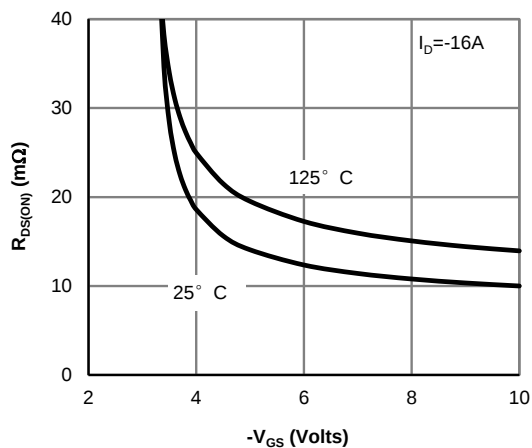


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

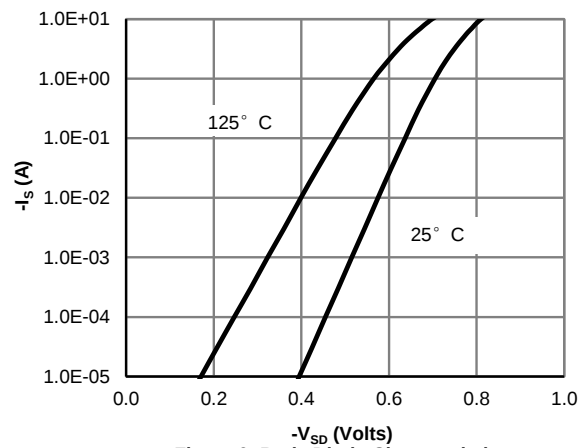


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

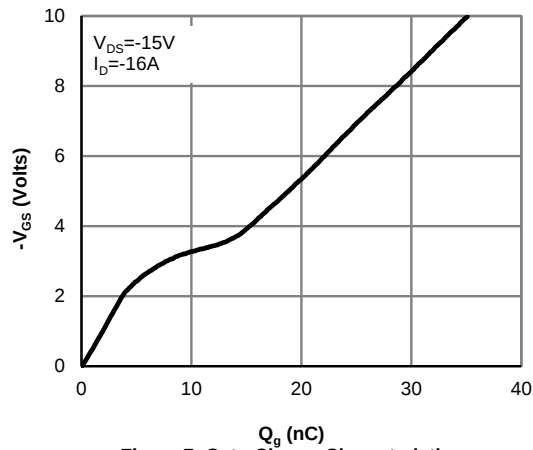


Figure 7: Gate-Charge Characteristics

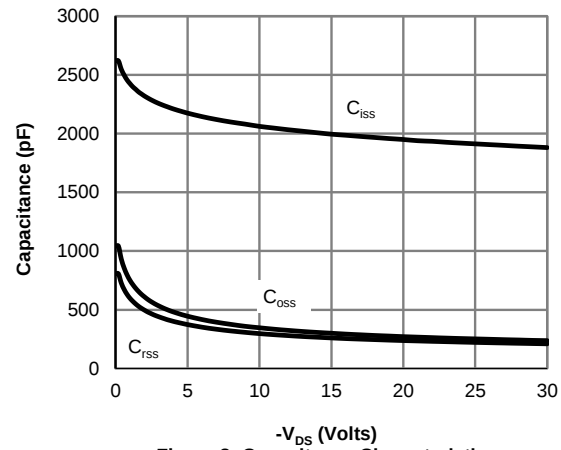


Figure 8: Capacitance Characteristics

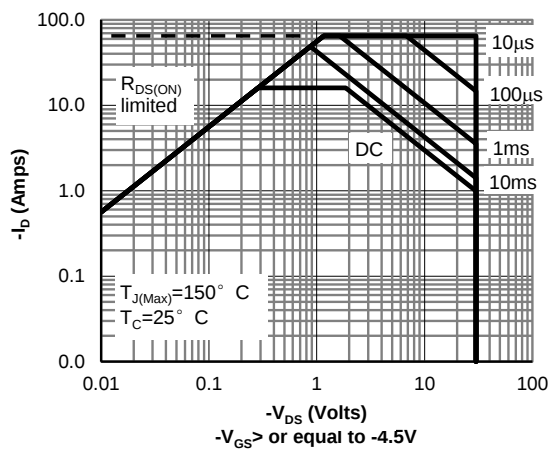


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

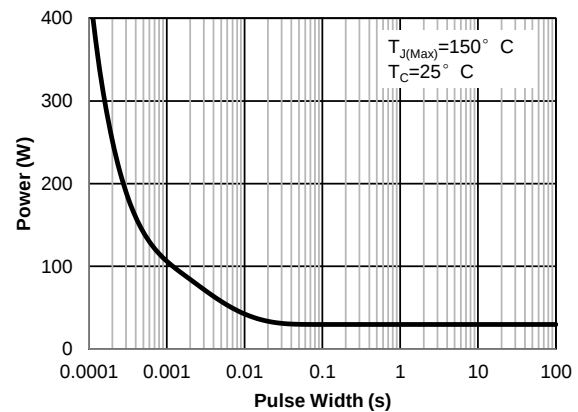


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

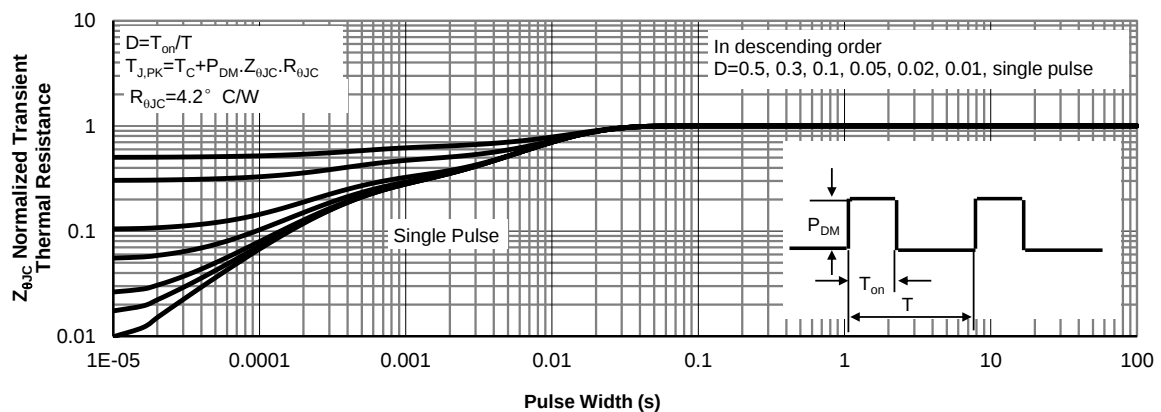


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

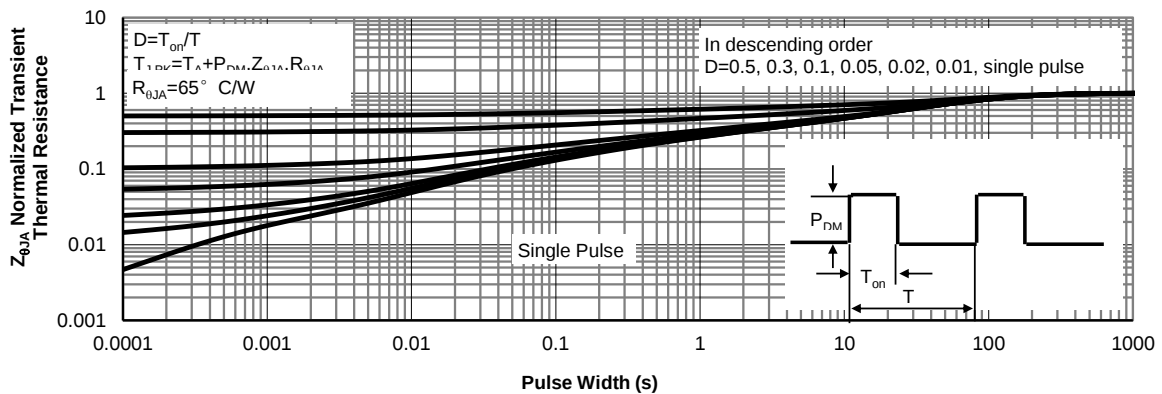
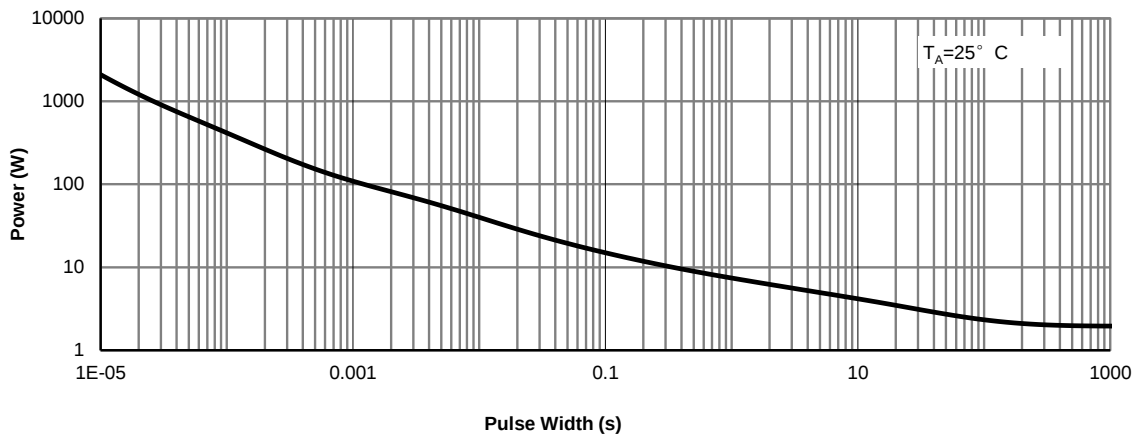
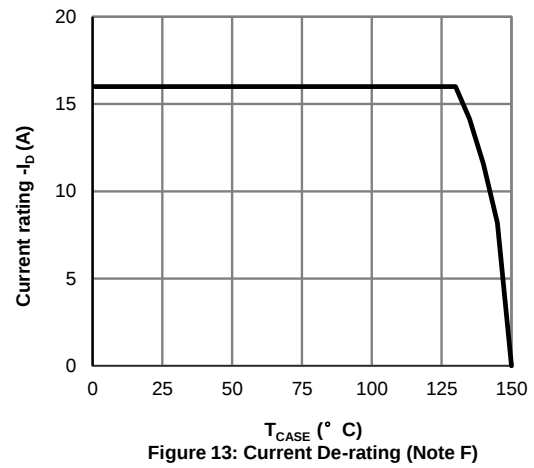
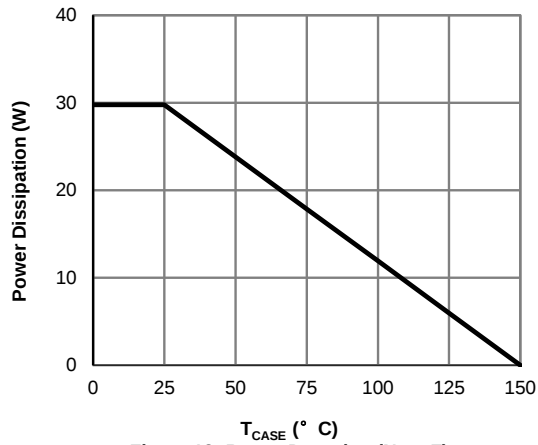


Figure A: Gate Charge Test Circuit & Waveforms

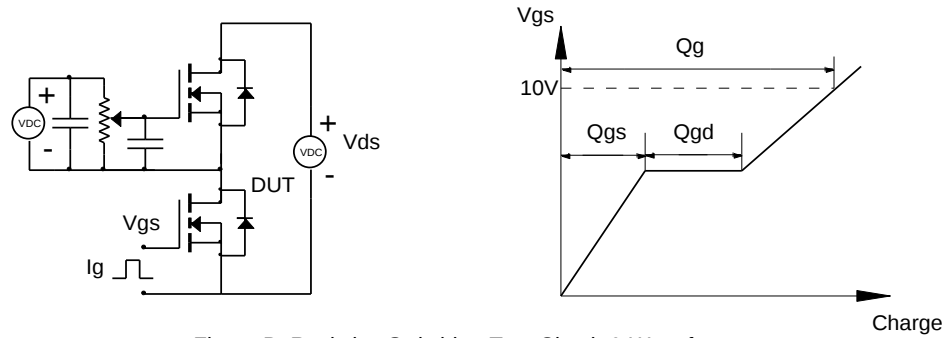


Figure B: Resistive Switching Test Circuit & Waveforms

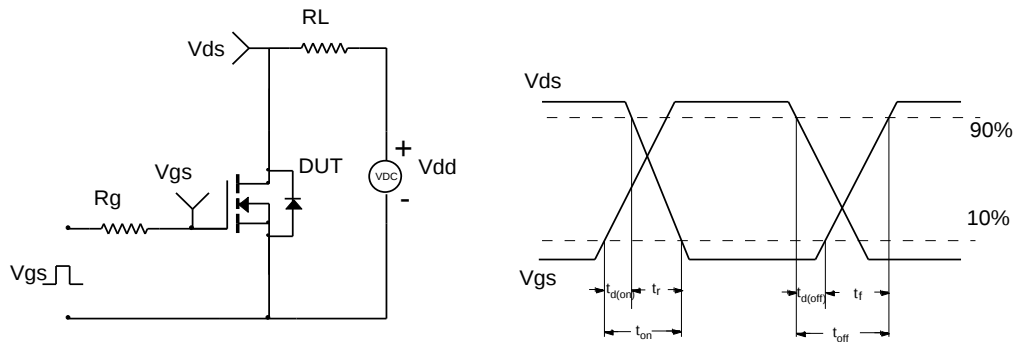


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

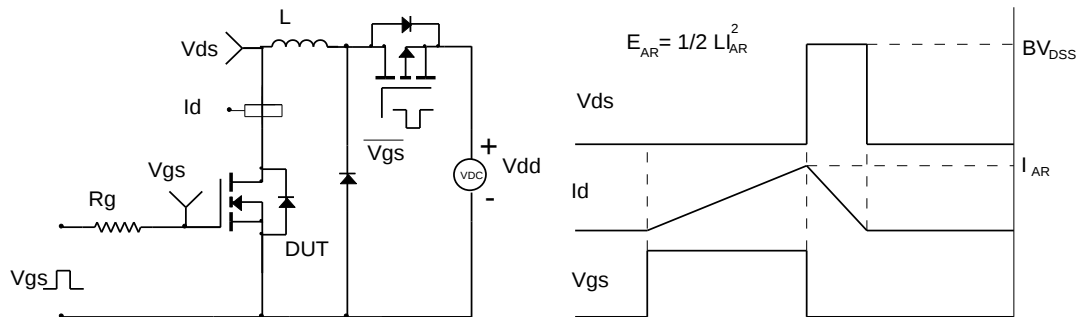
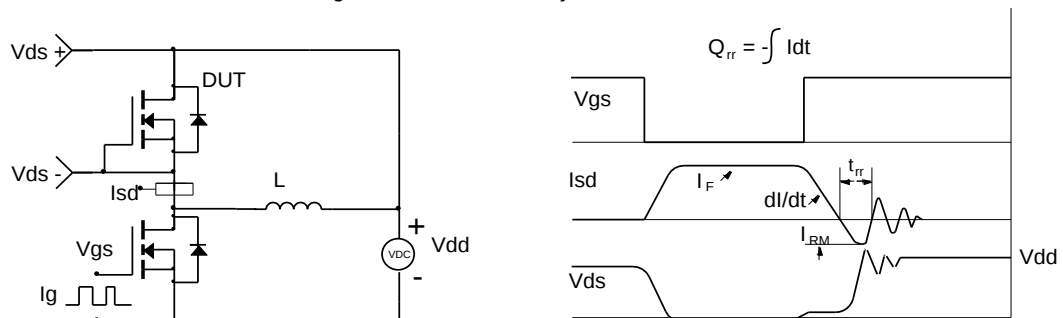
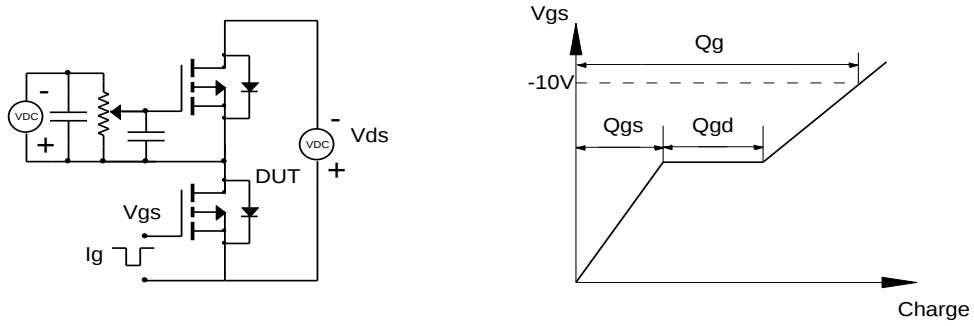


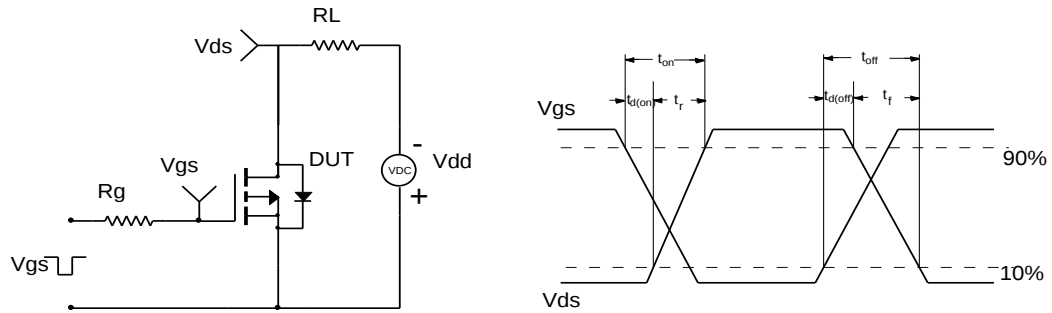
Figure D: Diode Recovery Test Circuit & Waveforms



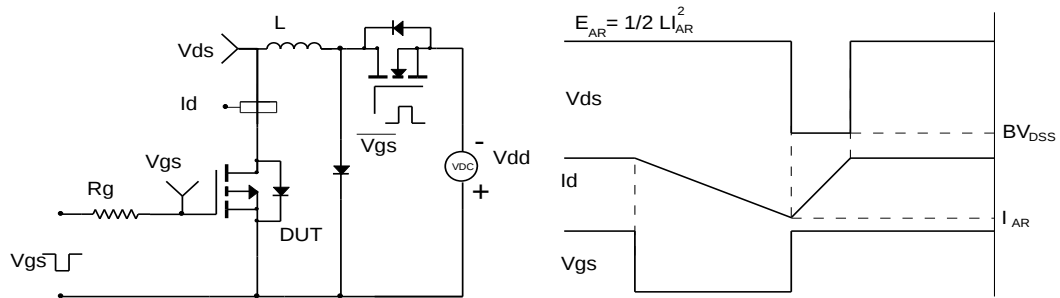
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

