

General Description

The AOT14N50FD/AOTF14N50FD have been fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications. By providing low $R_{DS(on)}$, C_{iss} and C_{rss} along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.

For Halogen Free add "L" suffix to part number:
 AOT14N50FDL & AOTF14N50FDL

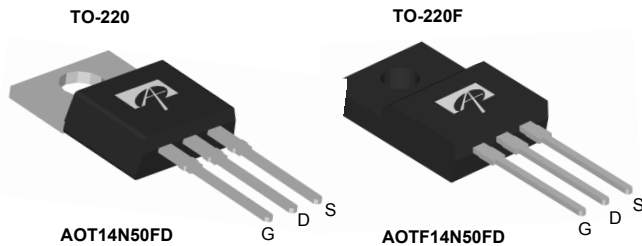
Product Summary

V_{DS}	600V@150°C
I_D (at $V_{GS}=10V$)	14A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 0.47Ω

100% UIS Tested
 100% R_g Tested



Top View



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	AOT14N50FD	AOTF14N50FD	Units
Drain-Source Voltage	V_{DS}	500		V
Gate-Source Voltage	V_{GS}	±30		V
Continuous Drain Current	$T_C=25^\circ\text{C}$	14	14*	A
	$T_C=100^\circ\text{C}$	9.6	9.6*	
Pulsed Drain Current ^C	I_{DM}	56		A
Avalanche Current ^C	I_{AR}	5		A
Repetitive avalanche energy ^C	E_{AR}	375		mJ
Single pulsed avalanche energy ^G	E_{AS}	750		mJ
Peak diode recovery dv/dt	dv/dt	5		V/ns
Power Dissipation ^B	$T_C=25^\circ\text{C}$	278	50	W
	Derate above 25°C	2.2	0.4	W/°C
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		°C
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	T_L	300		°C

Thermal Characteristics

Parameter	Symbol	AOT14N50FD	AOTF14N50FD	Units
Maximum Junction-to-Ambient ^{A,D}	$R_{\theta JA}$	65	65	°C/W
Maximum Case-to-sink ^A	$R_{\theta CS}$	0.5	--	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	0.45	2.5	°C/W

* Drain current limited by maximum junction temperature.

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =10mA, V _{GS} =0V, T _J =25°C	500			V
		I _D =10mA, V _{GS} =0V, T _J =150°C		600		
BV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D =10mA, V _{GS} =0V		0.57		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =500V, V _{GS} =0V			10	μA
		V _{DS} =400V, T _J =125°C			100	
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±30V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =5V, I _D =250μA	2.4	3	4	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =7A		0.37	0.47	Ω
g _{FS}	Forward Transconductance	V _{DS} =40V, I _D =7A		15		S
V _{SD}	Diode Forward Voltage	I _S =14A, V _{GS} =0V		1.3	1.6	V
I _S	Maximum Body-Diode Continuous Current				14	A
I _{SM}	Maximum Body-Diode Pulsed Current				56	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =25V, f=1MHz	1300	1654	2010	pF
C _{oss}	Output Capacitance		120	179	235	pF
C _{rss}	Reverse Transfer Capacitance		8	14.5	21	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	1.7	3.4	5.1	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =400V, I _D =14A	30	38.8	47	nC
Q _{gs}	Gate Source Charge			8.7		nC
Q _{gd}	Gate Drain Charge			17.5		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =250V, I _D =14A, R _G =25Ω		32		ns
t _r	Turn-On Rise Time			94		ns
t _{D(off)}	Turn-Off DelayTime			104		ns
t _f	Turn-Off Fall Time			78		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =14A, dI/dt=100A/μs, V _{DS} =100V		90	145	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =14A, dI/dt=100A/μs, V _{DS} =100V		0.3	0.5	μC

A. The value of R_{θJA} is measured with the device in a still air environment with T_A=25°C.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C, Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating.

G. L=60mH, I_{AS}=5A, V_{DD}=150V, R_G=25Ω, Starting T_J=25°C

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

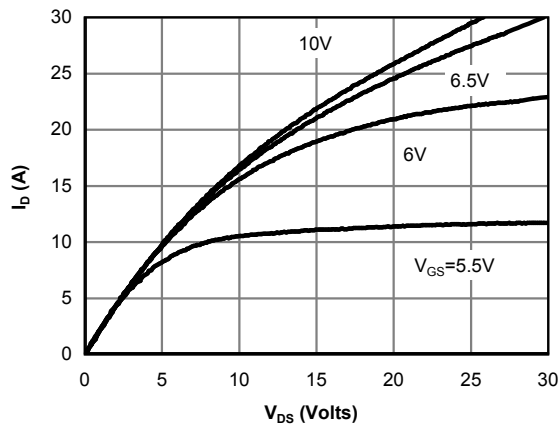


Fig 1: On-Region Characteristics

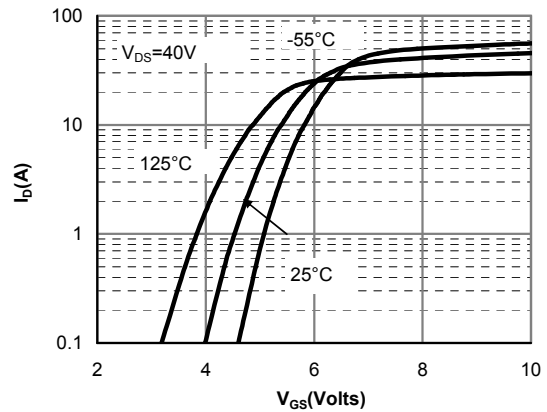


Figure 2: Transfer Characteristics

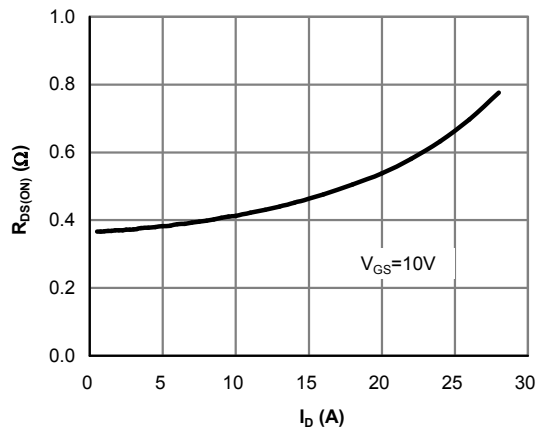


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

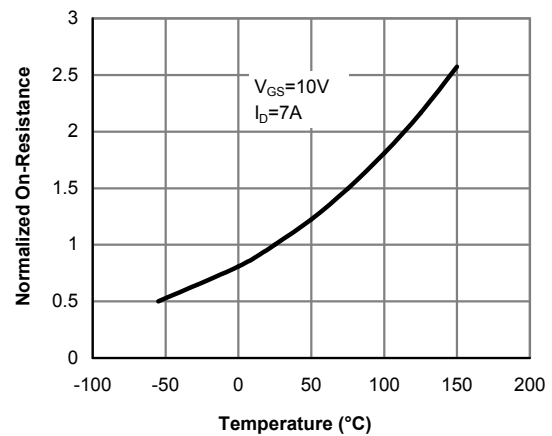


Figure 4: On-Resistance vs. Junction Temperature

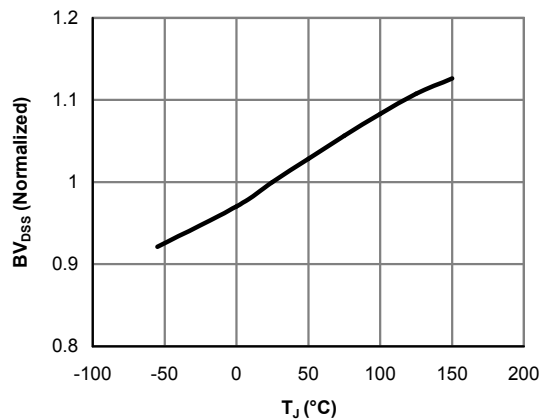


Figure 5: Break Down vs. Junction Temperature

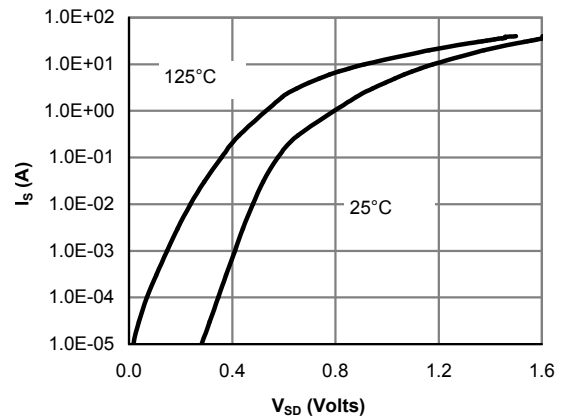


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

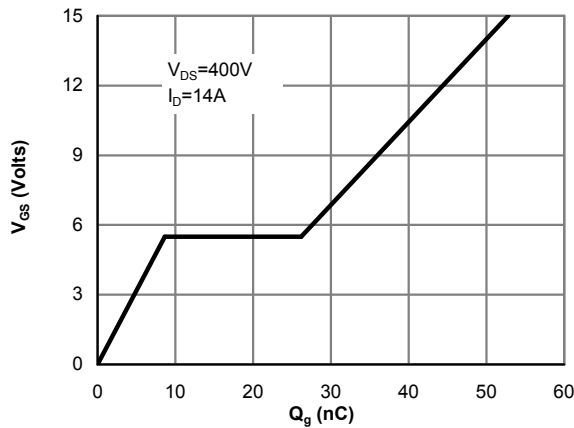


Figure 7: Gate-Charge Characteristics

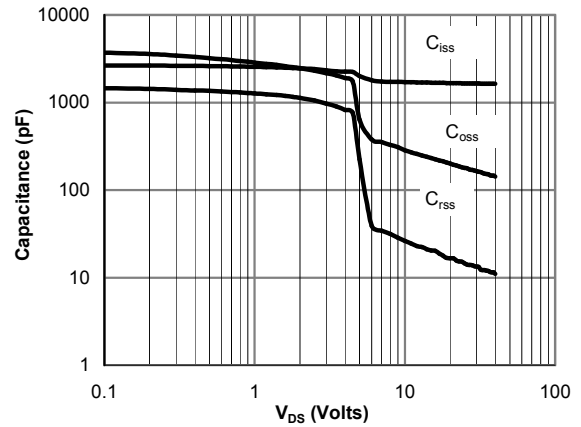


Figure 8: Capacitance Characteristics

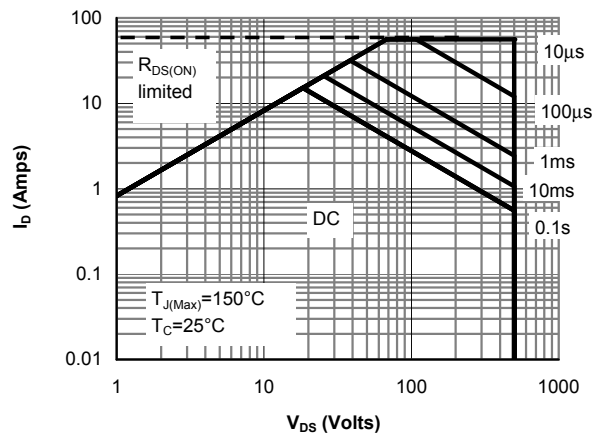


Figure 9: Maximum Forward Biased Safe Operating Area for AOT14N50FD (Note F)

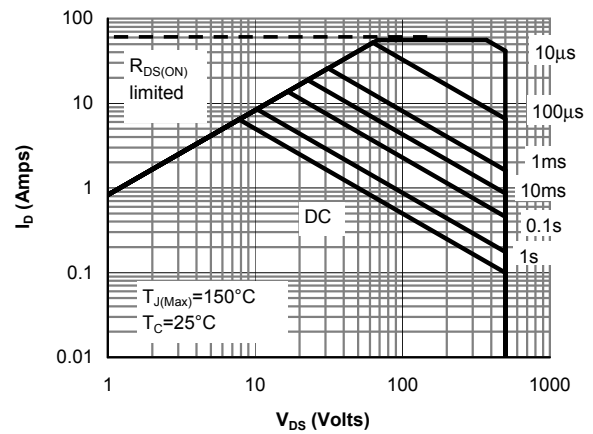


Figure 10: Maximum Forward Biased Safe Operating Area for AOTF14N50FD (Note F)

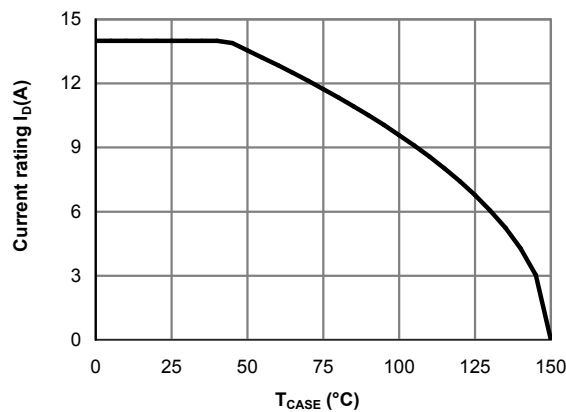


Figure 11: Current De-rating (Note B)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

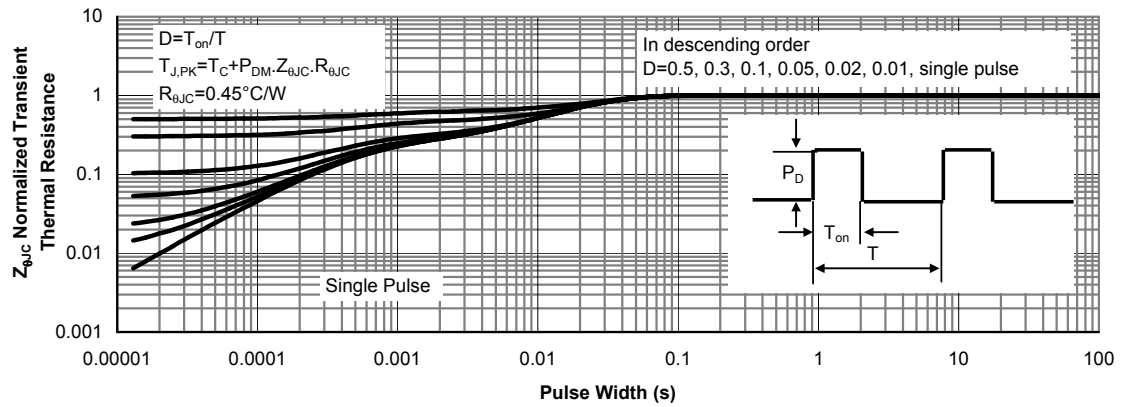


Figure 12: Normalized Maximum Transient Thermal Impedance for AOT14N50FD (Note F)

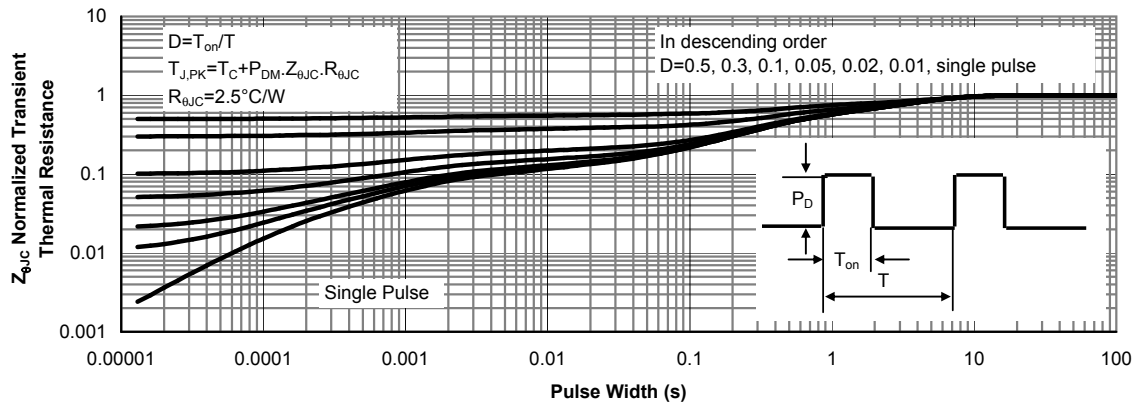


Figure 13: Normalized Maximum Transient Thermal Impedance for AOTF14N50FD (Note F)

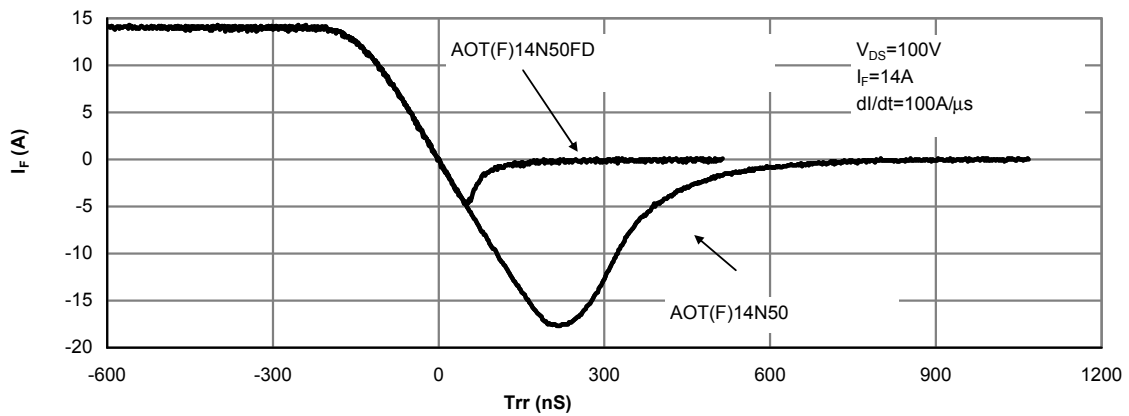
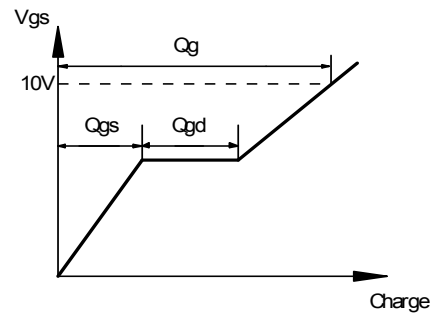
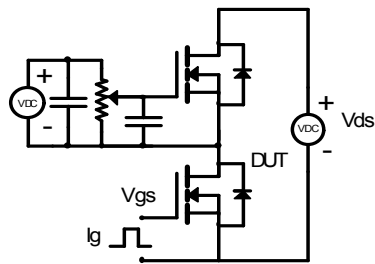
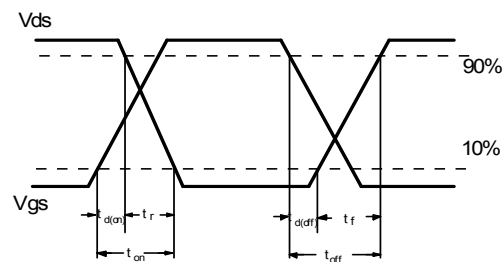
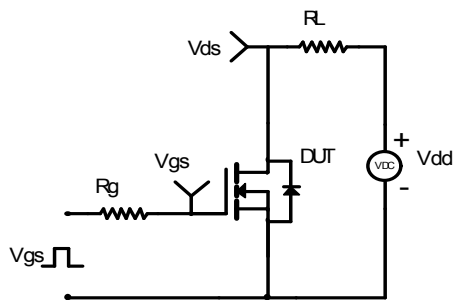


Figure 14: Diode Recovery Characteristics

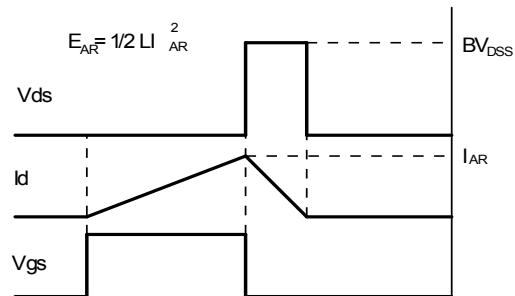
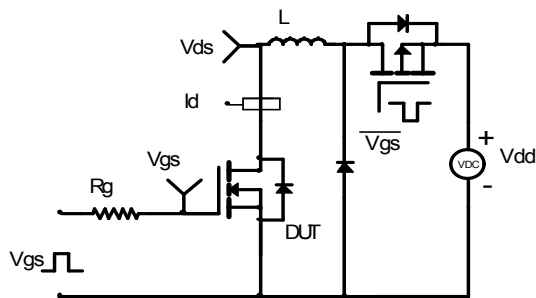
Gate Charge Test Circuit & Waveform



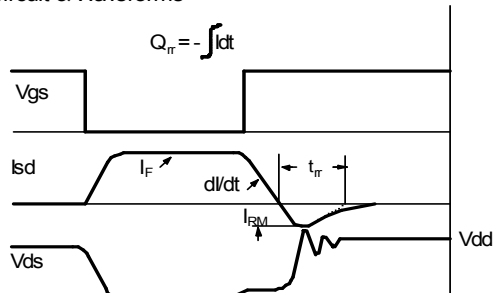
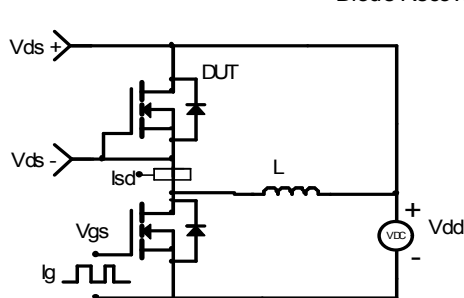
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



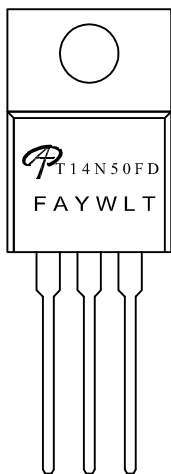
Diode Recovery Test Circuit & Waveforms



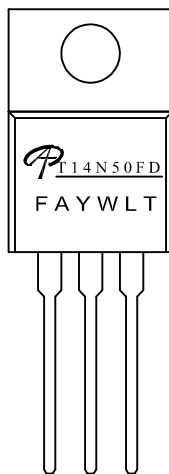


Document No.	PD-01211
Version	A
Title	AOT14N50FD Marking Description

TO220 PACKAGE MARKING DESCRIPTION



Standard product



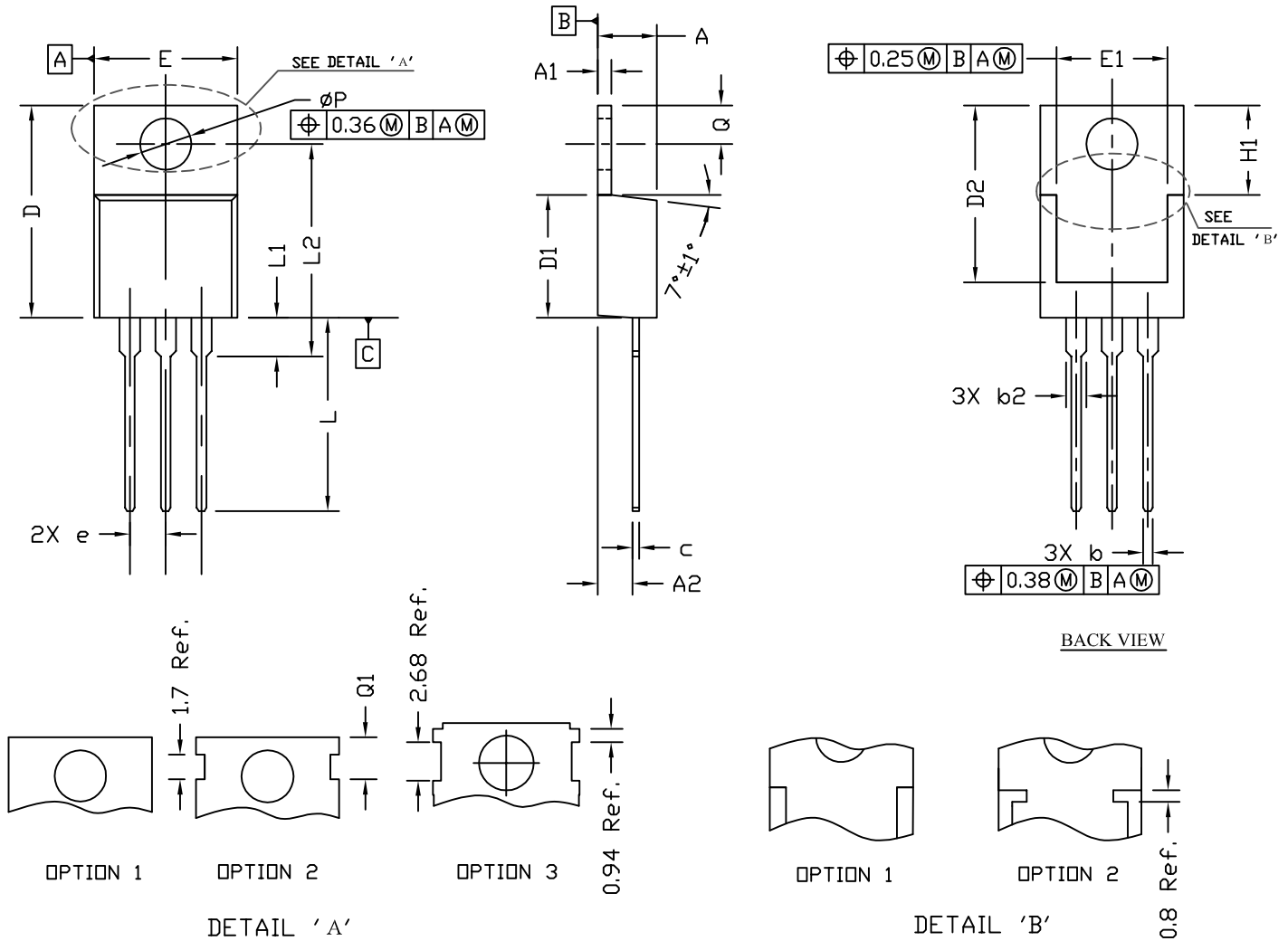
Green product

NOTE:
LOGO - AOS Logo
T14N50FD - Part number code
F - Fab code
A - Assembly location code
Y - Year code
W - Week code
L&T - Assembly lot code

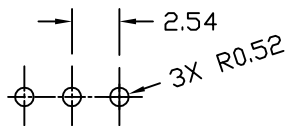
PART NO.	DESCRIPTION	CODE
AOT14N50FD	Standard product	T14N50FD
AOT14N50FDL	Green product	<u>T14N50FD</u>



TO220 PACKAGE OUTLINE



RECOMMENDATION OF HOLE PATTERN



UNIT: mm

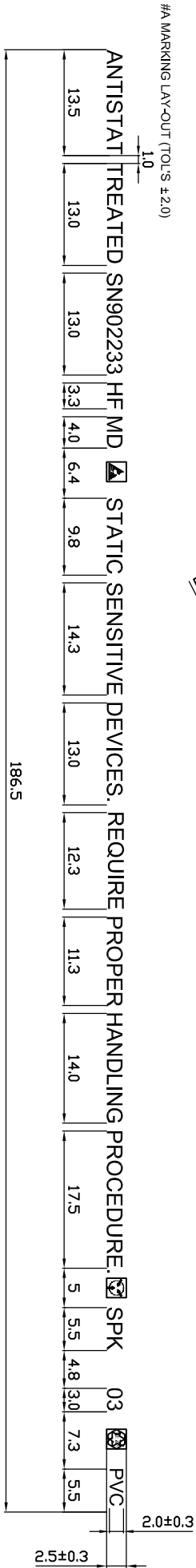
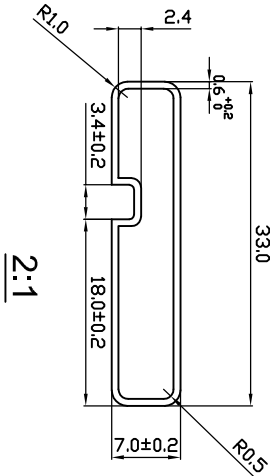
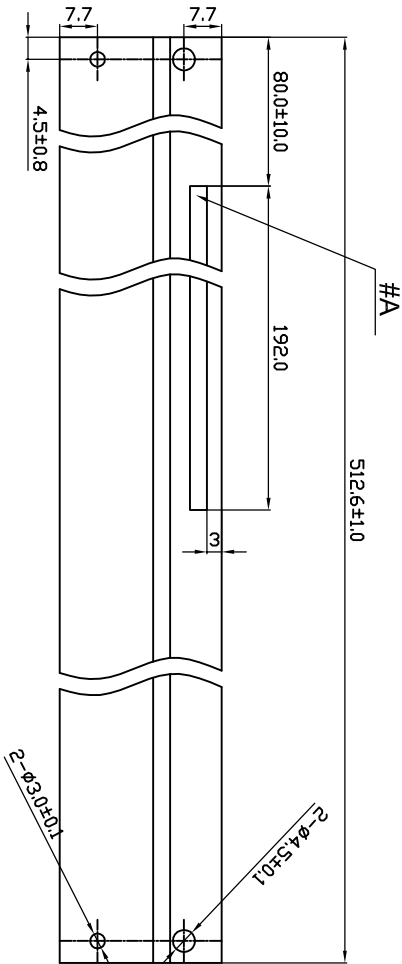
NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH SHOULD BE LESS THAN 6 MIL.
2. TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
3. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.30	4.45	4.72	0.169	0.175	0.186
A1	1.15	1.27	1.40	0.045	0.050	0.055
A2	2.20	2.67	2.90	0.087	0.105	0.114
b	0.69	0.81	0.95	0.027	0.032	0.037
b2	1.17	1.37	1.45	0.046	0.050	0.068
c	0.36	0.38	0.60	0.014	0.015	0.024
D	14.50	15.44	15.80	0.571	0.608	0.622
D1	8.59	9.14	9.65	0.338	0.360	0.380
D2	11.43	11.73	12.48	0.450	0.462	0.491
e	2.54 BSC			0.100 BSC		
E	9.66	10.03	10.54	0.380	0.395	0.415
E1	6.22	---	---	0.245	---	---
H1	6.10	6.30	6.50	0.240	0.248	0.256
L	12.27	12.82	14.27	0.483	0.505	0.562
L1	2.47	---	3.90	0.097	---	0.154
L2	---	---	16.70	---	---	0.657
Q	2.59	2.74	2.89	0.102	0.108	0.114
ϕP	3.50	3.84	3.89	0.138	0.151	0.153
Q1	2.70	---	2.90	0.106	---	0.114

REV.	DATE	DESCRIPTION	DRG.
A		NEW ISSUE	

TO220/TO262 PLASTIC TUBE DRAWING



(NOTE)

2:1

1. TUBE
 - MATERIAL : P.V.C
 - COLOR : TRANSPARENCY, RED, YELLOW
 - MARKING #A : 6 MONTHS, BLACK COLOR
 - LETTER STYLE : Arial
 - CAMBAR : 1.5 MAX
2. PIN
 - COLOR : GREEN (ONE PIN MUST BE INSERTED IN LEFT-SIDE OF " ANTISTATIC~" AND ANOTHER PIN IS FREE.)
3. ALL UNSPECIFICATED SPECIFICATIONS FOLLOW TUBE GENERAL SPEC. UNSPECIFICATED TOLERANCE ±0.2
4. PACKING Q'TY :

PKG	QTY(PCS)
TO220/ TO262	50

 ALPHA & OMEGA SEMICONDUCTOR				TITLE			
DRAWN BY				T0220/T0262 TUBE DRAWING			
APPROVED BY							
SCALE							
N.T.S.							
PROJECTION							
TR-00060							
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1 OF 1							
REV.							
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AOS Semiconductor Product Reliability Report

AOT14N50FD, rev B

Plastic Encapsulated Device

ALPHA & OMEGA Semiconductor, Inc

www.aosmd.com

Nov. 2017

This AOS product reliability report summarizes the qualification result for AOT14N50FD. Accelerated environmental tests are performed on a specific sample size, and then followed by electrical test at end point. Review of final electrical test result confirms that AOT14N50FD passes AOS quality and reliability requirements. The released product will be categorized by the process family and be routine monitored for continuously improving the product quality.

I. Reliability Stress Test Summary and Results

Test Item	Test Condition	Time Point	Total Sample Size	Number of Failures	Reference Standard
HTGB	Temp = 150°C , Vgs=100% of Vgsmax	168 / 500 / 1000 hours	924 pcs	0	JESD22-A108
HTRB	Temp = 150°C , Vds=80% of Vdsmax	168 / 500 / 1000 hours	924 pcs	0	JESD22-A108
HAST	130°C , 85%RH, 33.3 psia, Vds = 80% of Vdsmax up to 42V	96 hours	693 pcs	0	JESD22-A110
H3TRB	85°C , 85%RH, Vds = 80% of Vdsmax up to 100V	1000 hours	693 pcs	0	JESD22-A101
Autoclave	121°C , 29.7psia, RH=100%	96 hours	924 pcs	0	JESD22-A102
Temperature Cycle	-65°C to 150°C , air to air,	1000cycles	924 pcs	0	JESD22-A104
HTSL	Temp = 150°C	1000 hours	693 pcs	0	JESD22-A103
IOL	$\Delta T_j = 100^\circ\text{C}$	8572 cycles	693 pcs	0	AEC Q101
Resistance to Solder Heat	Temp = 270°C	15 seconds	30 pcs	0	JESD22-B106

Note: The reliability data presents total of available generic data up to the published date.

II. Reliability Evaluation

FIT rate (per billion): 1.91

MTTF = 59839 years

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size. Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

Failure Rate = $\text{Chi}^2 \times 10^9 / [2 (N) (H) (Af)] = 1.91$

MTTF = $10^9 / \text{FIT} = 59839$ years

Chi² = Chi Squared Distribution, determined by the number of failures and confidence interval

N = Total Number of units from burn-in tests

H = Duration of burn-in testing

Af = Acceleration Factor from Test to Use Conditions (Ea = 0.7eV and Tuse = 55°C)

Acceleration Factor **[Af]** = $\text{Exp} [E_a / k (1/T_j u - 1/T_j s)]$

Acceleration Factor ratio list:

	55 deg C	70 deg C	85 deg C	100 deg C	115 deg C	130 deg C	150 deg C
Af	259	87	32	13	5.64	2.59	1

Tj s = Stressed junction temperature in degree (Kelvin), K = C+273.16

Tj u = The use junction temperature in degree (Kelvin), K = C+273.16

k = Boltzmann's constant, $8.617164 \times 10^{-5} \text{ eV} / \text{K}$