ALPHA & OMEGA SEMICONDUCTOR

AOZ1012D

EZBuck™ 3A Simple Buck Regulator

April 2006

General Description

The AOZ1012D is a high efficiency, simple to use, 3A buck regulator. The AOZ1012D works from a 4.5V to 16V input voltage range, and provides up to 3A of continuous output current with an output voltage adjustable down to 0.8V.

The AOZ1012D comes in 4X5 DFN-8 packages and is rated over a -40°C to +85°C ambient temperature range.

Features

- 4.5V to 16V operating input voltage range
- 50 m Ω internal PFET switch for high efficiency: up to 95%
- Internal Schottky Diode
- Internal soft start
- Output voltage adjustable to 0.8V
- 3A continuous output current
- Fixed 500kHz PWM operation
- Cycle-by-cycle current limit
- Short-circuit protection
- Thermal shutdown
- Small size DFN-8 packages

Applications

- Point of load dc/dc conversion
- PCIe graphics cards
- Set top boxes
- DVD drives and HDD
- LCD panels
- Cable modems
- Telecom/Networking/Datacom equipment

Typical Application

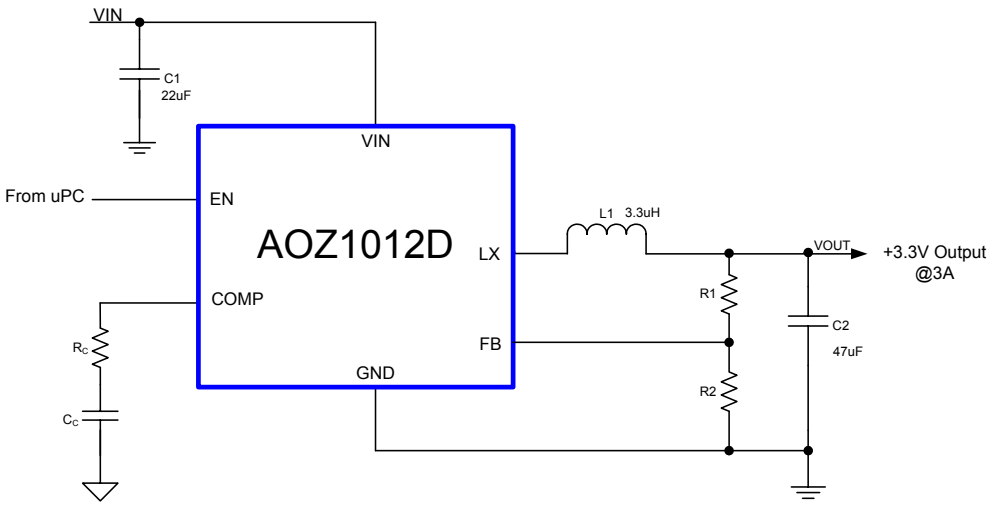
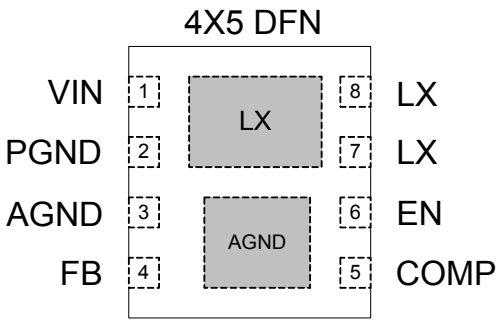


Figure 1. 3.3V/3A Buck Down Regulator

Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ1012DI	-40°C to +85°C	DFN-8	RoHS Compliant

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Function
1	VIN	Supply voltage input. When VIN rises above the UVLO threshold the device starts up.
2	PGND	Power ground. Electrically needs to be connected to AGND.
3	AGND	Reference connection for controller section. Also used as thermal connection for controller section. Electrically needs to be connected to PGND.
4	FB	The FB pin is used to determine the output voltage via a resistor divider between the output and GND.
5	COMP	External loop compensation pin.
6	EN	The enable pin is active high. Connect EN pin to VIN if not used. Do not leave the EN pin floating.
7,8	LX	PWM output connection to inductor. Thermal connection for output stage.

Absolute Maximum Ratings[1]

Parameter	Units
Supply Voltage (V_{IN})	18V
LX to AGND	-0.7V to V_{IN}+0.3V
EN to AGND	-0.3V to V_{IN}+0.3V
FB to AGND	-0.3V to 6V
COMP to AGND	-0.3V to 6V
PGND to AGND	-0.3V to +0.3V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C

Recommend Operating Ratings[2]

Parameter	Units
Supply Voltage (V_{IN})	4.5V to 16V
Output Voltage Range	0.8V to V_{IN}
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance DFN-8 (Θ_{JA})	53° C/W

Electrical Characteristics

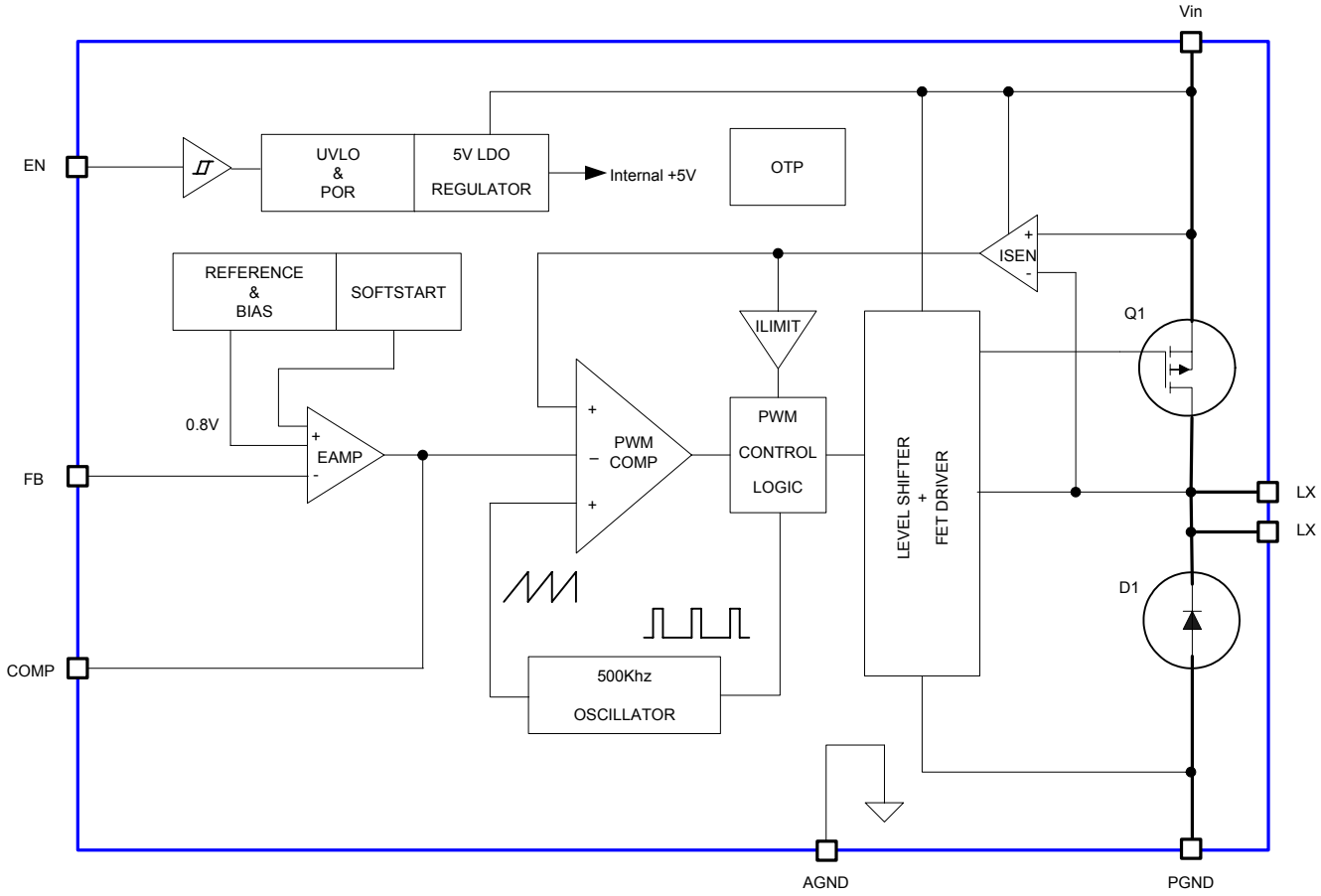
T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V unless otherwise specified[4].

Parameter	Symbol	Conditions	MIN	TYP	MAX	UNITS
Supply Voltage	V_{IN}		**4.5**		**16**	V
Input Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising V_{IN} falling		**4.0** **3.7**		V V
Supply Current (Quiescent)	I_{IN}	I_{OUT} = 0, V_{FB} = 1.2V, V_{EN} >2V		**2**	**3**	mA
Shutdown Supply Current	I_{OFF}	V_{EN} = 0V		**3**	**20**	µA
Feedback Voltage	V_{FB}		0.782	0.8	0.818	V
Load Regulation				0.5		**%**
Line Regulation				1		**%**
Feedback Voltage Input Current	I_{FB}				200	nA
EN Input Threshold	V_{EN}	Off threshold On threshold	 **2.0**		**0.6**	V V
EN Input Hysteresis	V_{HYS}			**100**		mV
Modulator						
Frequency	f_O		350	500	600	kHz
Maximum Duty Cycle	D_{MAX}		100			%
Minimum Duty Cycle	D_{MIN}				6	%
Error Amplifier Voltage Gain				500		V/V
Error Amplifier Transconductance				200		µA/V
Protection						
Current Limit	I_{LIM}		4		5	A
Over-Temperature Shutdown Limit		T_J rising T_J falling		145 100		°C °C
Soft Start Interval	t_{SS}			4		ms
Output Stage						
High-Side Switch On-Resistance		V_{IN} = 12V V_{IN} = 5V		**40** **65**	**50** **85**	mΩ mΩ

Notes:

1. Exceeding the Absolute Maximum ratings may damage the device.
2. The device is not guaranteed to operate beyond the Maximum Operating ratings.
3. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5KΩ in series with 100pF.
4. Specification in BOLD indicate an ambient temperature range of -40°C to +85°C. These specifications are guaranteed by design.

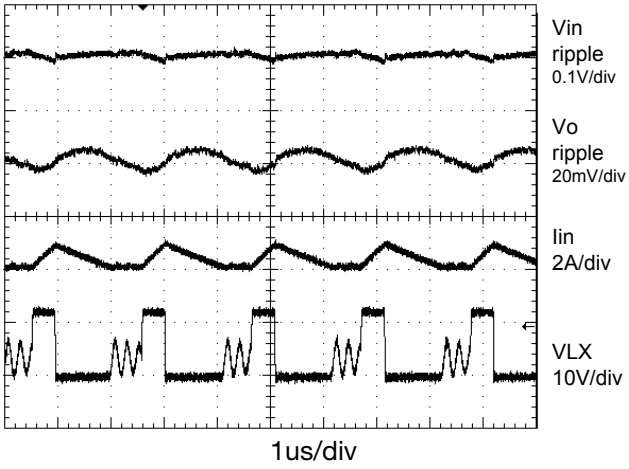
Functional Block Diagram



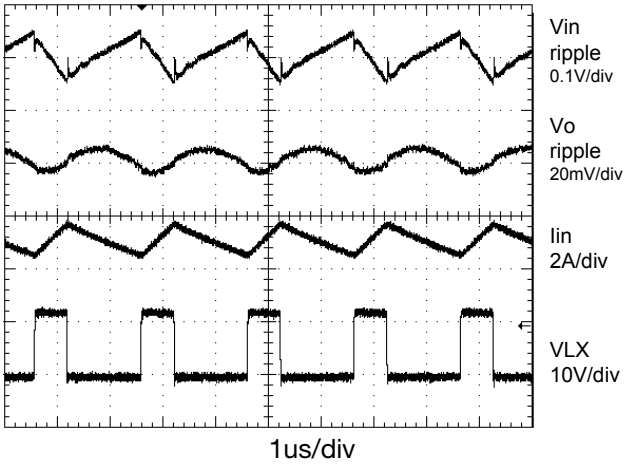
Typical Performance Characteristics

Circuit of figure 1. T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V unless otherwise specified.

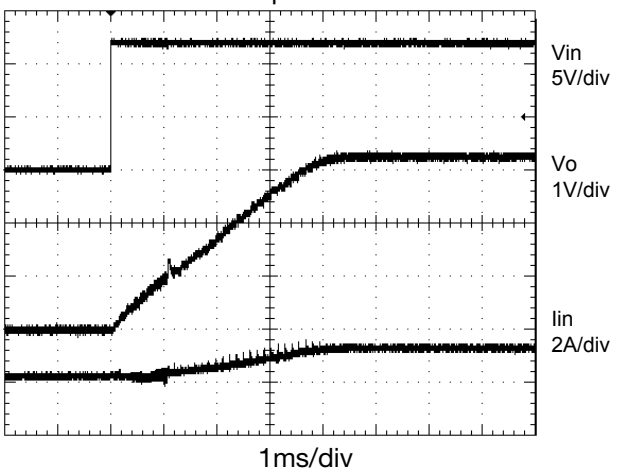
Light load (DCM) operation



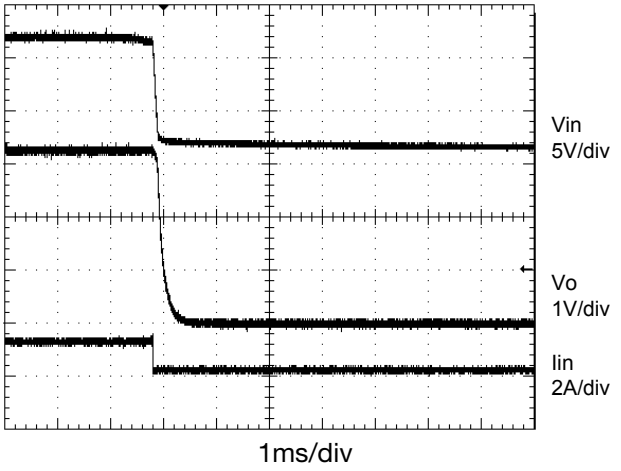
Full load (CCM) operation



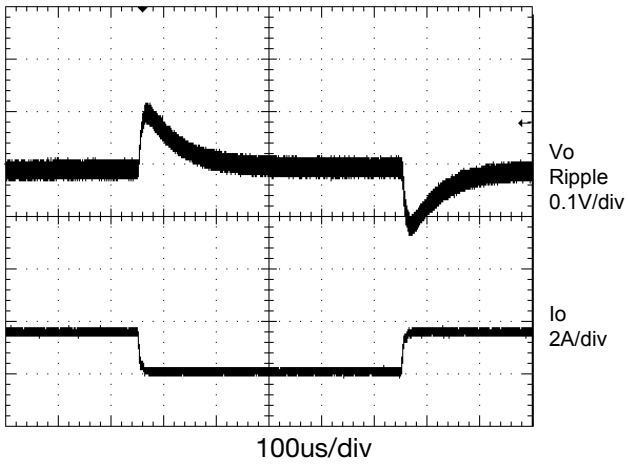
Start up to full load



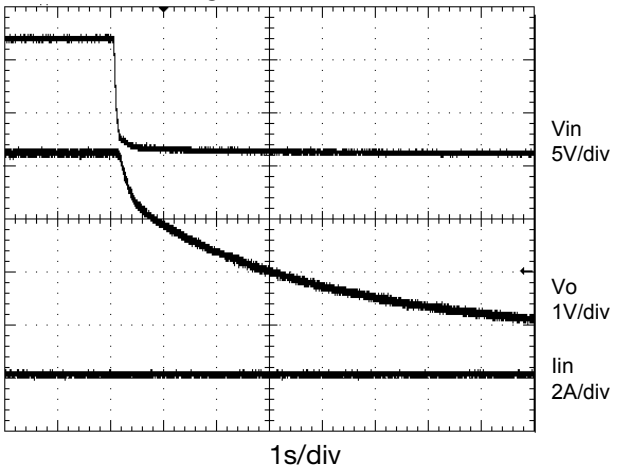
Full load to turn off



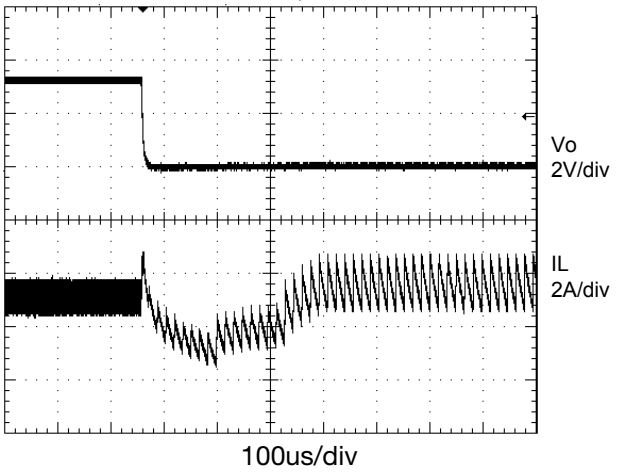
50% to 100% Load transient



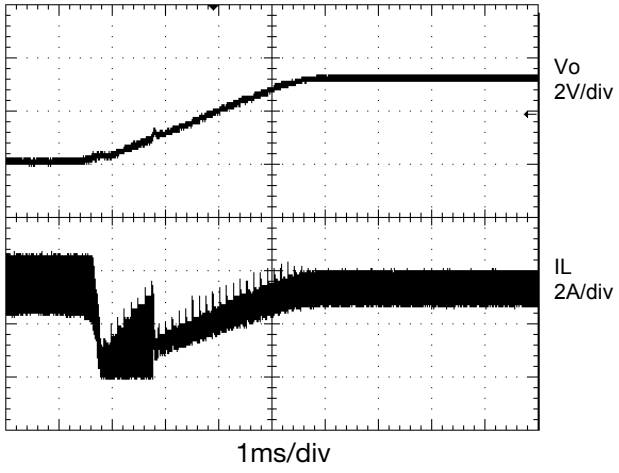
Light load to turn off



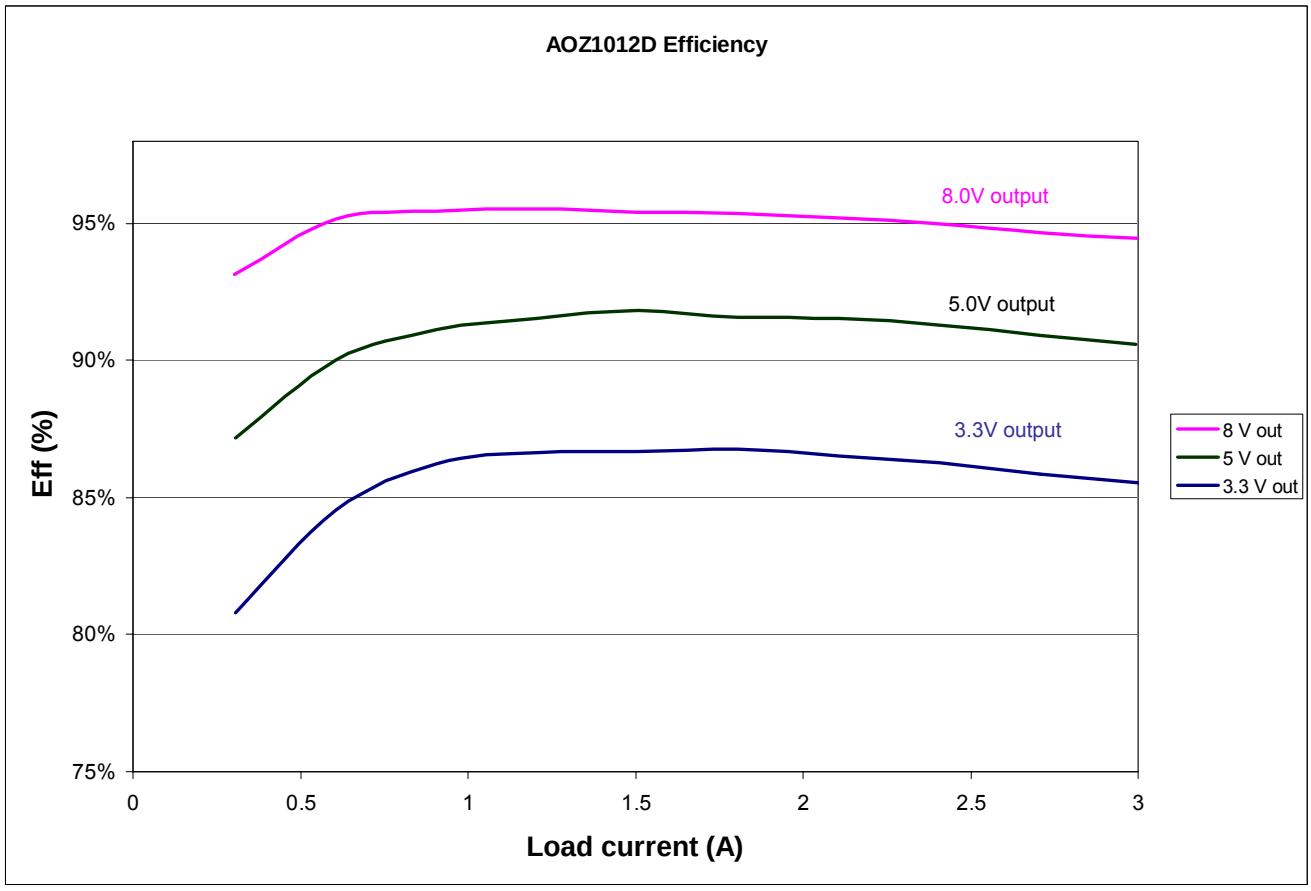
Short circuit protection



Short circuit recovery

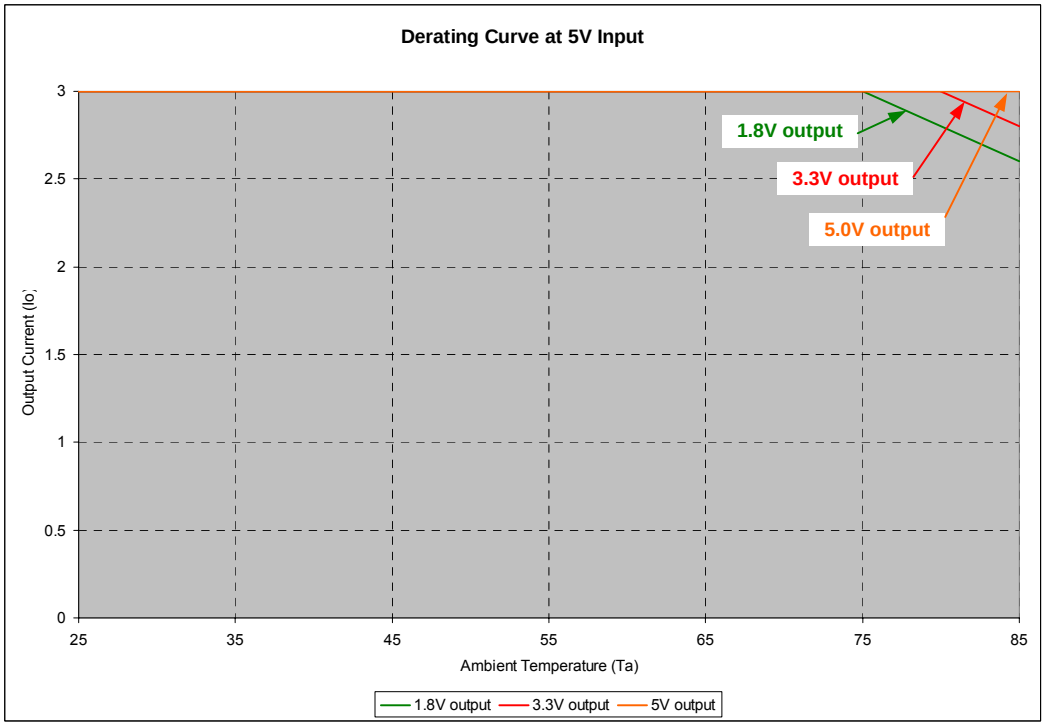


Efficiency (Vin=12V) vs. load current

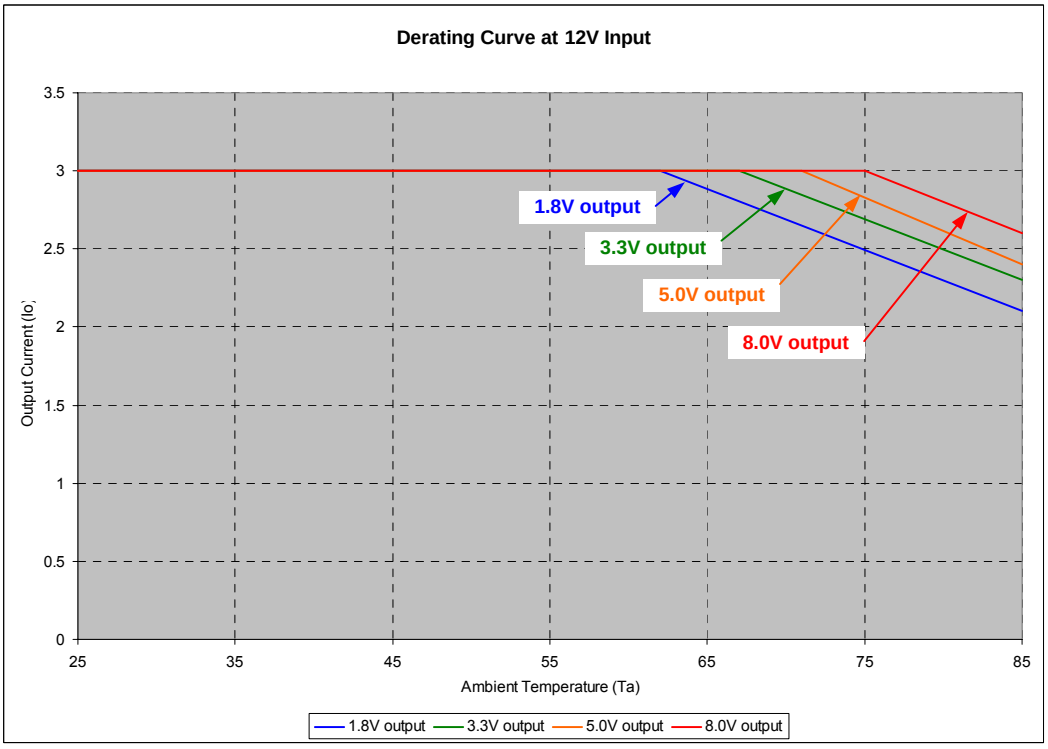


Thermal de-rating curves for DFN-8 package part under typical input and output condition
Circuit of figure 1. 25ºC ambient temperature and natural convection (air speed<50LFM) unless otherwise specified.

AOZ1012DI De-rating curves at 5 V input



AOZ1012DI De-rating curves at 12V input



Detailed Description

AOZ1012D is a current-mode step down regulator with integrated high side PMOS switch and a low side freewheeling Schottky diode. It operates from a 4.5V to 16V input voltage range and supplies up to 3A of load current. The duty cycle can be adjusted from 6% to 100% allowing a wide range of output voltage. Features include enable control, Power-On Reset, input under voltage lockout, fixed internal soft-start and thermal shut down.

AOZ1012D is available in thermally enhanced DFN-8 package.

Enable and Soft Start

AOZ1012D has internal soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulation voltage. A soft start process begins when the input voltage rises to 4.0V and voltage on EN pin is HIGH. In soft start process, the output voltage is ramped to regulation voltage in typically 4ms. The 4ms soft start time is set internally.

The EN pin of the AOZ1012D is active high. Connect the EN pin to VIN if enable function is not used. Pull it to ground will disable the AOZ1012D. Do not leave it open. The voltage on EN pin must be above 2.0 V to enable the AOZ1012D. When voltage on EN pin falls below 0.6 V, the AOZ1012D is disabled. If an application circuit requires the AOZ1012D to be disabled, an open drain or open collector circuit should be used to interface to EN pin.

Steady-State Operation

Under steady-state conditions, the converter operates in fixed frequency and Continuous-Conduction Mode (CCM).

AOZ1012D integrates an internal P-MOSFET as the high-side switch. Inductor current is sensed by amplifying the voltage drop across the drain to source of the high side power MOSFET. Output voltage is divided down by the external voltage divider at the FB pin. The difference of the FB pin voltage and reference is amplified by the internal transconductance error amplifier. The error voltage, which shows on the COMP pin, is compared against the current signal, which is sum of inductor current signal and ramp compensation signal, at PWM comparator input. If the current signal is less than the error voltage, the internal high-side switch is on. The inductor current flows from the input through the inductor to the output. When the current signal exceeds the error voltage, the high-side switch is off.

The inductor current is freewheeling through the internal Schottky diode to output.

The AOZ1012D uses a P-Channel MOSFET as the high side switch. It saves the bootstrap capacitor normally seen in a circuit which is using an NMOS switch. It allows 100% turn-on of the upper switch to achieve linear regulation mode of operation. The minimum voltage drop from V_{IN} to V_O is the load current times DC resistance of MOSFET plus DC resistance of buck inductor. It can be calculated by equation below:

$$V_{O\_MAX} = V_{IN} - I_O \times (R_{DS(ON)} + R_{inductor})$$

Where V_{O_MAX} is the maximum output voltage;
V_{IN} is the input voltage from 4.5V to 16V;
I_O is the output current from 0A to 3A;
$R_{DS(ON)}$ is the on resistance of internal MOSFET, the value is between 40m and 85m depending on input voltage and junction temperature;
$R_{inductor}$ is the inductor DC resistance;

Switching Frequency

The AOZ1012D switching frequency is fixed and set by an internal oscillator. The actuall switching frequency could range from 350kHz to 600kHz due to device variation.

Output Voltage Programming

Output voltage can be set by feeding back the output to the FB pin with a resistor divider network. In the application circuit shown in Figure 1. The resistor divider network includes R_1 and R_2. Usually, a design is started by picking a fixed R_2 value and calculating the required R1 with equation below.

$$V_O = 0.8 \times (1 + \frac{R_1}{R_2})$$

Some standard value of R_1, R_2 for most commonly used output voltage values are listed in Table 1.

Table 1.

Vo (V)	R1 (k Ω)	R2 (k Ω)
0.8	1.0	open
1.2	4.99	10
1.5	10	11.5
1.8	12.7	10.2
2.5	21.5	10
3.3	31.6	10
5.0	52.3	10

Combination of R1 and R2 should be large enough to avoid drawing excessive current from the output, which will cause power loss.

Since the switch duty cycle can be as high as 100%, the maximum output voltage can be set as high as the input voltage minus the voltage drop on upper PMOS and inductor.

Protection Features
AOZ1012D has multiple protection features to prevent system circuit damage under abnormal conditions.

Over Current Protection (OCP)
The sensed inductor current signal is also used for over current protection. Since AOZ1012D employs peak current mode control, the COMP pin voltage is proportional to the peak inductor current. The COMP pin voltage is limited to be between 0.4V and 2.5V internally. The peak inductor current is automatically limited cycle by cycle.

The cycle by cycle current limit threshold is set between 4A and 5A. When the load current reaches the current limit threshold, the cycle by cycle current limit circuit turns off the high side switch immediately to terminate the current duty cycle. The inductor current stop rising. The cycle by cycle current limit protection directly limits inductor peak current. The average inductor current is also limited since the limitation of peak inductor current. When cycle by cycle current limit circuit is triggered, the output voltage drops as the duty cycle decreasing.

The AOZ1012D has internal short circuit protection circuit to protect itself from catastrophic failure under output short circuit conditions. The FB pin voltage is proportional to the output voltage. Whenever FB pin voltage is below 0.2V, the short circuit protection circuit is triggered. As a result, the converter is shut down and hiccups at a frequency equals to 1/8 of normal switching

frequency. The converter will start up via a soft start once the short circuit condition disappears. In short circuit protection mode, the inductor average current is greatly reduced because of the low hiccup frequency.

Power-On Reset (POR)
A power-on reset circuit monitors the input voltage. When the input voltage exceeds 4V, the converter starts operation. When input voltage falls below 3.7V, the converter will stop switching.

Thermal Protection
An internal temperature sensor monitors the junction temperature. It shuts down the internal control circuit and high side PMOS if the junction temperature exceeds 145ºC. The regulator will restart automatically under the control of soft-start circuit when the junction temperature decreases to 100ºC.

Application Information
The basic AOZ1012D application circuit is shown in Figure 1. Component selection is explained below.

Input capacitor
The input capacitor must be connected to the V_{IN} pin and PGND pin of AOZ1012D to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times (1 - \frac{V_O}{V_{IN}}) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}}(1 - \frac{V_O}{V_{IN}})}$$

if let *m* equal the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relation between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Fig. 2 below. It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is $0.5 \cdot I_O$.

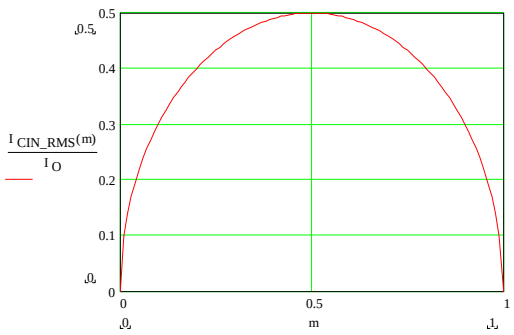


Figure 2. I_{CIN} vs. voltage conversion ratio

For reliable operation and best performance, the input capacitors must have current rating higher than $I_{CIN-RMS}$ at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high ripple current rating. Depending on the application circuits, other low ESR tantalum capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors are preferred for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures are based on certain amount of life time. Further de-rating may be necessary for practical design requirement.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is,

$$\Delta I_L = \frac{V_O}{f \times L} \times (1 - \frac{V_O}{V_{IN}})$$

The peak inductor current is:

$$I_{Lpeak} = I_O + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 20% to 30% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Table below lists some inductors for typical output voltage design.

Table 2.

Vout	L1	Manufacture
5.0 V	Shield, 5.8uH ET553-5R8	ELYTONE
	Un-shielded, 4.7uH DO3316P-472MLD	Coilcraft
3.3 V	Un-shielded, 4.7uH DO3316P-472MLD	Coilcraft
	Un-shielded, 4.7uH DO1813P-472HC	Coilcraft
1.8 V	Shield, 2.2uH ET553-2R2	ELYTONE
	Un-shielded, 2.2uH DO3316P-222MLD	Coilcraft
	Un-shielded, 2.2uH DO1813P-222HC	Coilcraft

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_O = \Delta I_L \times (ESR_{CO} + \frac{1}{8 \times f \times C_O})$$

where C_O is output capacitor value and ESR_{CO} is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = \Delta I_L \times \frac{1}{8 \times f \times C_O}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_O = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

Loop Compensation

AOZ1012D employs peak current mode control for easy use and fast transient response. Peak current mode control eliminates the double pole effect of the output L&C filter. It greatly simplifies the compensation loop design.

With peak current mode control, the buck power stage can be simplified to be a one-pole and one-zero system in frequency domain. The pole is dominant pole and can be calculated by:

$$f_{p1} = \frac{1}{2\pi \times C_O \times R_L}$$

The zero is a ESR zero due to output capacitor and its ESR. It is can be calculated by:

$$f_{Z1} = \frac{1}{2\pi \times C_O \times ESR_{CO}}$$

Where C_O is the output filter capacitor;
R_L is load resistor value;
ESR_{CO} is the equivalent series resistance of output capacitor;

The compensation design is actually to shape the converter close loop transfer function to get desired gain and phase. Several different types of compensation network can be used for AOZ1012D. For most cases, a series capacitor and resistor network connected to the COMP pin sets the pole-zero and is adequate for a stable high-bandwidth control loop.

In AOZ1012D, FB pin and COMP pin are the inverting input and the output of internal transconductance error amplifier. A series R and C compensation network connected to COMP provides one pole and one zero. The pole is:

$$f_{p2} = \frac{G_{EA}}{2\pi \times C_C \times G_{VEA}}$$

Where G_{EA} is the error amplifier transconductance, which is $200 \cdot 10^{-6}$ A/V;
G_{VEA} is the error amplifier voltage gain, which is 500 V/V;
C_C is compensation capacitor;

The zero given by the external compensation network, capacitor C_C and resistor R_C, is located at:

$$f_{Z2} = \frac{1}{2\pi \times C_C \times R_C}$$

To design the compensation circuit, a target crossover frequency f_C for close loop must be selected. The system crossover frequency is where control loop has unity gain. The crossover frequency is the also called the converter bandwidth. Generally a higher bandwidth means faster response to load transient. However, the bandwidth should not be too high because of system stability concern. When designing the compensation

loop, converter stability under all line and load condition must be considered.

Usually, it is recommended to set the bandwidth to be less than 1/10 of switching frequency. The AOZ1012D operates at a fixed switching frequency range from 350kHz to 600kHz. It is recommended to choose a crossover frequency less than 30kHz.

$$f_C = 30kHz$$

The strategy for choosing R_c and C_c is to set the cross over frequency with R_c and set the compensator zero with C_c. Using selected crossover frequency, f_c, to calculate R_c:

$$R_C = f_C \times \frac{V_O}{V_{FB}} \times \frac{2\pi \times C_O}{G_{EA} \times G_{CS}}$$

where f_c is desired crossover frequency;
V_{FB} is 0.8V;
G_{EA} is the error amplifier transconductance, which is $200 \cdot 10^{-6}$ A/V;
G_{CS} is the current sense circuit transconductance, which is 6.68 A/V;

The compensation capacitor C_c and resistor R_c together make a zero. This zero is put somewhere close to the dominate pole f_{p1} but lower than 1/5 of selected crossover frequency. C_c can is selected by:

$$C_C = \frac{1.5}{2\pi \times R_C \times f_{p1}}$$

Equation above can also be simplified to:

$$C_C = \frac{C_O \times R_L}{R_C}$$

An easy-to-use application software which helps to design and simulate the compensation loop can be found at www.aosmd.com.

Thermal management and layout consideration

In the AOZ1012D buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the VIN pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the PGND pin of the AOZ1012D, to the LX pins of the AZO1012D. Current flows in the second loop when the low side diode is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is strongly recommended to connect input capacitor, output capacitor, and PGND pin of the AOZ1012D.

In the AOZ1012D buck regulator circuit, the two major power dissipating components are the AOZ1012D and output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total} = V_{IN} \cdot I_{IN} - V_O \cdot I_O$$

The power dissipation of inductor can be approximately calculated by output current and DCR of inductor.

$$P_{indcutor} = I_O{}^2 \cdot R_{inductor} \cdot 1.1$$

The actual AOZ1012D junction temperature can be calculated with power dissipation in the AOZ1012D and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total} - P_{inductor}) \cdot \Theta_{JA}$$

The maximum junction temperature of AOZ1012D is 150ºC, which limits the maximum load current capability. Please see the thermal de-rating curves for the maximum load current of the AOZ1012D under different ambient temperature.

The thermal performance of AOZ1012D is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

Several layout tips are listed below for the best electric and thermal performance. The figure 3 below illustrates a PCB layout example as reference.

1. Do not use thermal relief connection to the VIN and the PGND pin. Pour a maximized copper area to the PGND pin and the VIN pin to help thermal dissipation.

2. Input capacitor should be connected to the VIN pin and the PGND pin as close as possible.
3. A ground plane is preferred. If a ground plane is not used, separate PGND from AGND and connect them only at one point to avoid the PGND pin noise coupling to the AGND pin.
4. Make the current trace from LX pins to L to Co to the PGND as short as possible.
5. Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, GND or VOUT.
6. The two LX pins are connected to internal PFET drain. They are low resistance thermal conduction path and most noisy switching node. Connected a copper plane to LX pin to help thermal dissipation. This copper plane should not be too larger otherwise switching noise may be coupled to other part of circuit.

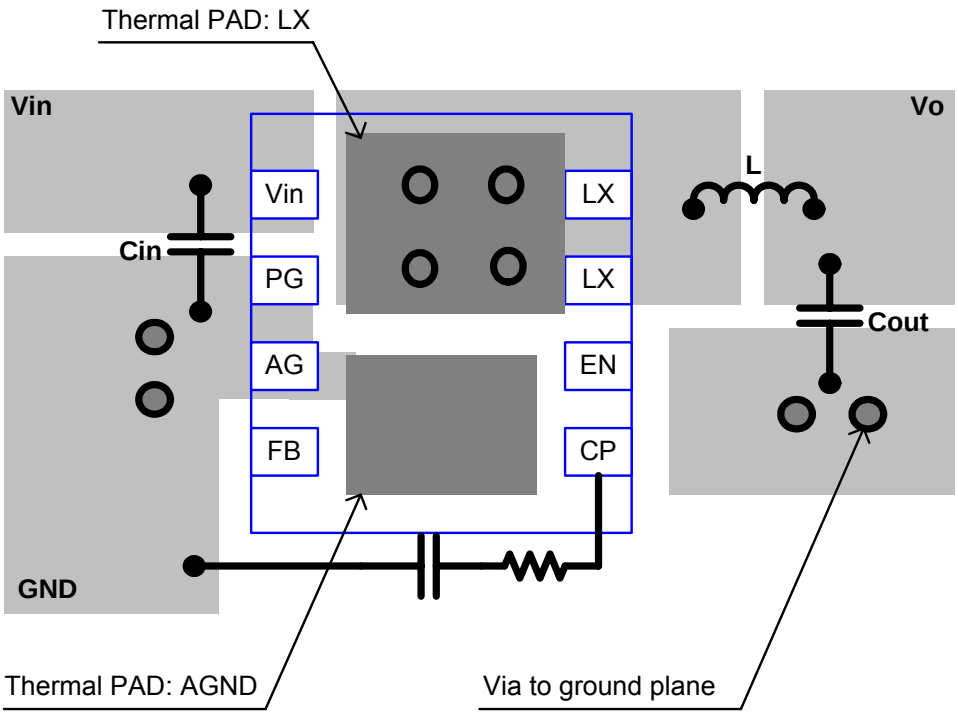
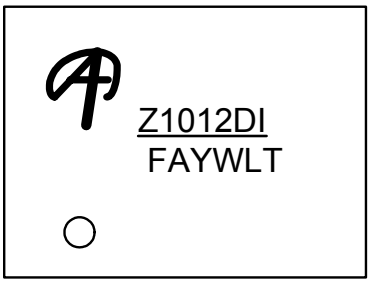


Figure 3. AOZ1012D PCB layout

DFN-8 Package Marking Description

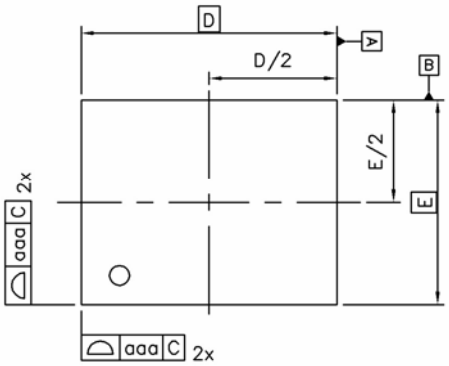


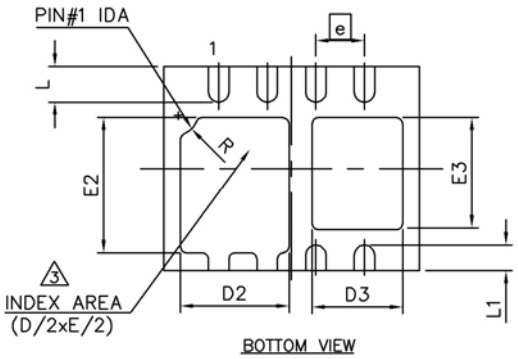
Note:	
Logo	AOS logo
Z1012DI	Part number code
F&A	Fab & Assembly location
Y	Year code
W	Week code
L&T	Assembly lot code

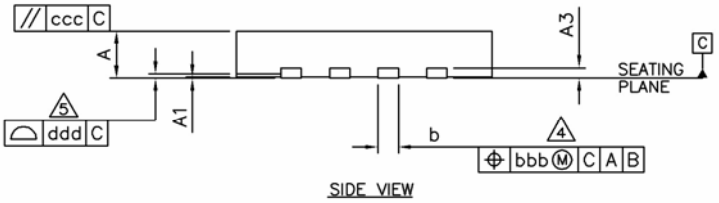
ALPHA & OMEGA SEMICONDUCTOR

Document No.	P0-00029
Version	rev B

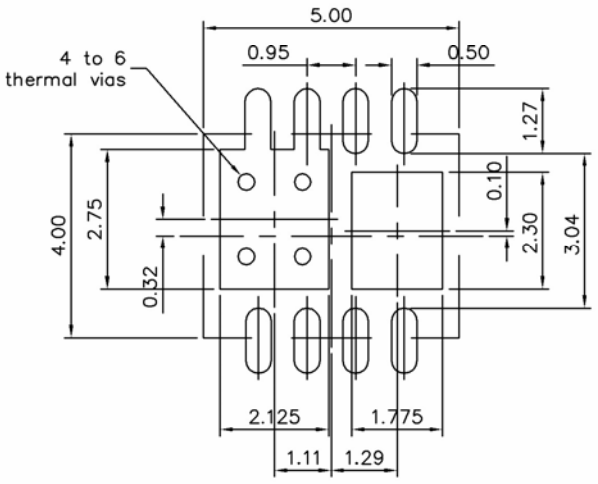
DFN 5x4 PACKAGE OUTLINE







RECOMMENDED LAND PATTERN (UNIT: mm)



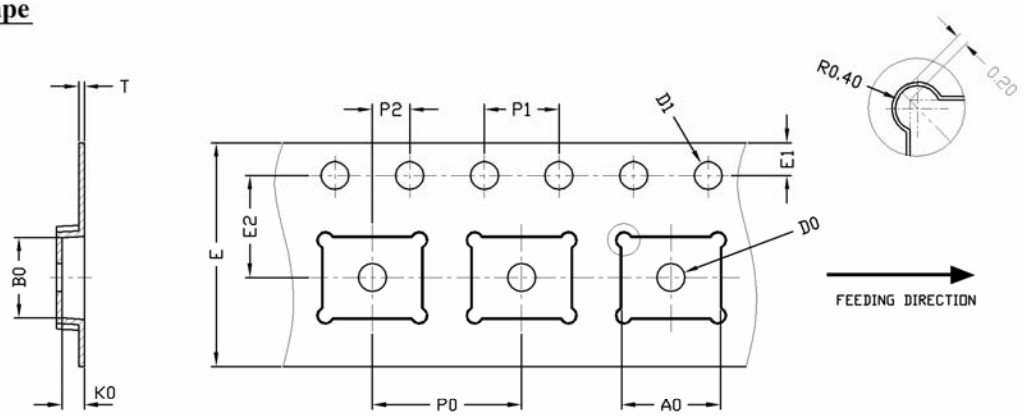
SYMBOL	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	---	0.20 ref	---	---	0.008 ref	---
b	0.35	0.40	0.45	0.014	0.016	0.018
D		5.00 BSC			0.197 BSC	
D2	1.975	2.125	2.225	0.078	0.084	0.088
D3	1.625	1.775	1.875	0.064	0.070	0.074
E		4.00 BSC			0.157 BSC	
E2	2.500	2.650	2.750	0.098	0.104	0.108
E3	2.050	2.200	2.300	0.081	0.087	0.091
e		0.95 BSC			0.037 BSC	
L	0.600	0.700	0.800	0.024	0.028	0.031
L1	0.400	0.500	0.600	0.016	0.020	0.024
R		0.30 REF			0.012 REF	
aaa		0.15			0.006	
bbb		0.10			0.004	
ccc		0.10			0.004	
ddd		0.08			0.003	

Note:
1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters.
3. The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SPP-002.
4. Dimension b appliers to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
5. Coplanarity applies to the terminals and all other bottom surface metallization.
6. Drawing shown are for illustration only.

ALPHA & OMEGA SEMICONDUCTOR

DFN5X4 Tape and Reel Data

DFN5X4 Tape

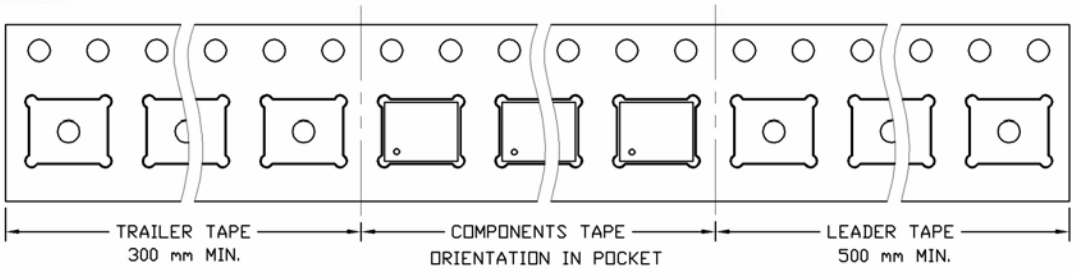


UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN 5x4 (12 mm)	5.30 ±0.10	4.30 ±0.10	1.20 ±0.10	1.50 MIN. TYP.	$1.50^{+0.10}_{-0}$	12.00 ±0.30	1.75 ±0.10	5.50 ±0.10	8.00 ±0.10	4.00 ±0.20	2.00 ±0.10	0.30 ±0.05

DFN5X4 Tape

Leader / Trailer
& Orientation

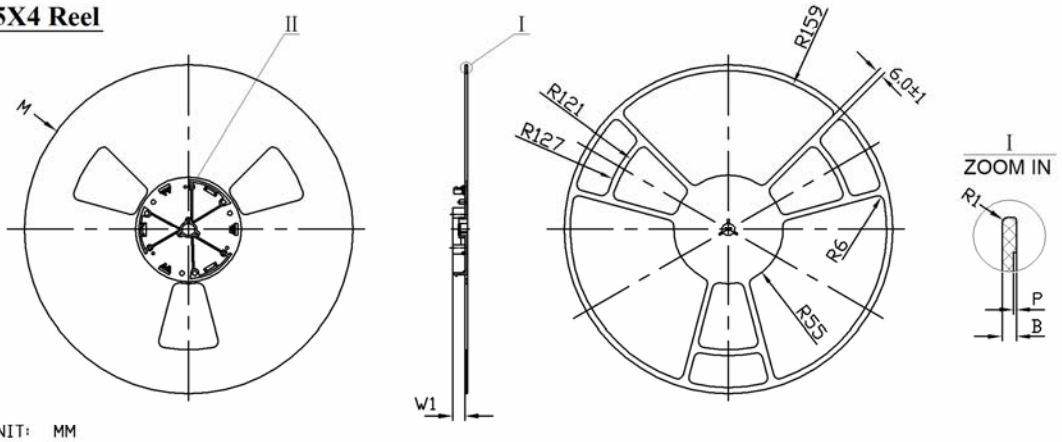


1 of 2

ALPHA & OMEGA SEMICONDUCTOR

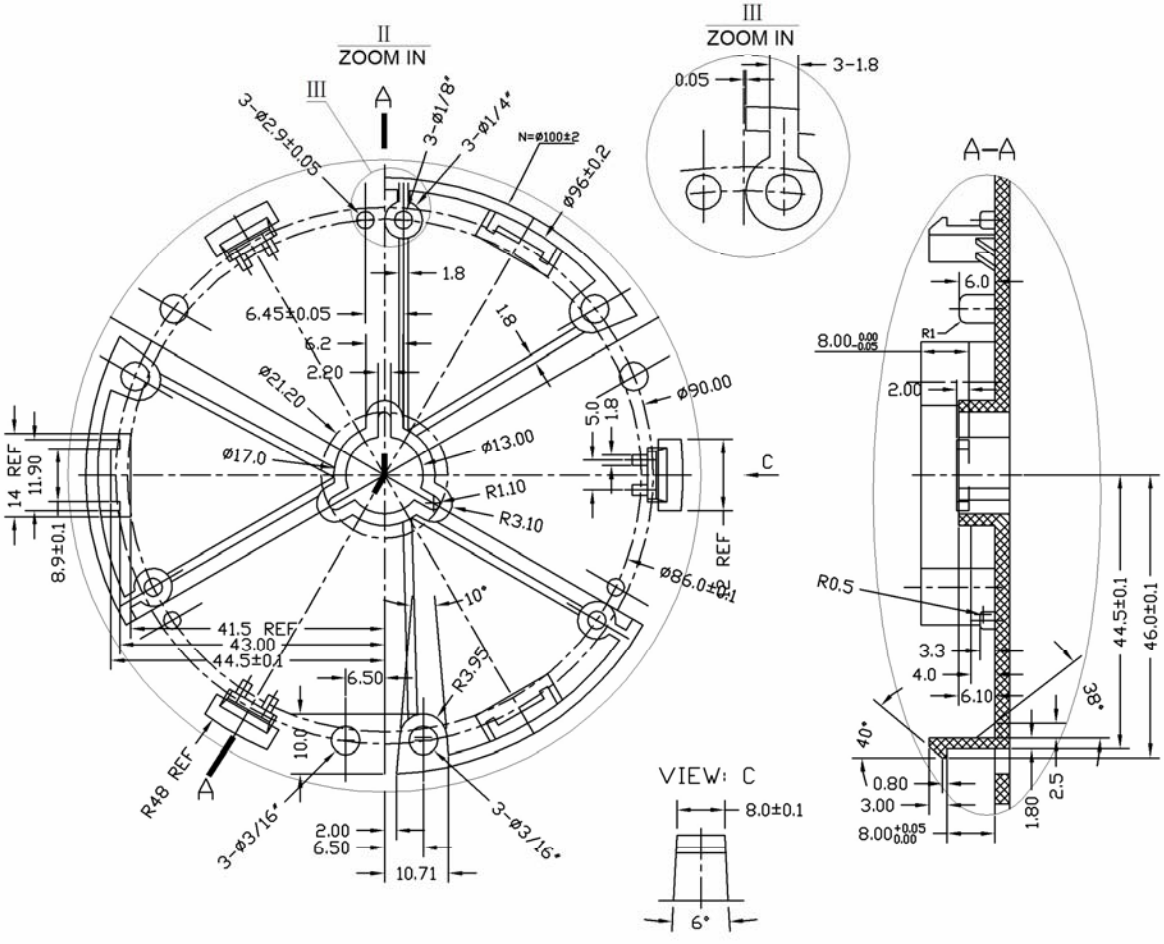
DFN5X4 Tape and Reel Data

DFN5X4 Reel



UNIT: MM

TAPE SIZE	REEL SIZE	M	W1	B	P
12	ø330	ø330.00 +0.3 −4.0	12.40 +2.0 −0.0	2.4 ±0.3	0.5



2 of 2