ALPHA & OMEGA
SEMICONDUCTOR

AOZ3054DI

EZBuck™ 6A Synchronous Buck Regulator

Not Recommended For New Designs

General Description

The AOZ3054DI is a high efficiency, easy to use, 6A synchronous buck regulator with a smart mode adoption function. The AOZ3054DI works from 4.5V to 18V input voltage range, and provides up to 6 A of continuous output current with an output voltage adjustable down to 0.8V.

The AOZ3054DI comes in a DFN5x6 package and is rated over a -40°C to +85°C operating ambient temperature range.

No Replacement

Features

- 4.5V to 18V operating input voltage range
- Synchronous Buck: 30mΩ internal high-side switch and 12mΩ internal low-side switch (at 12V)
- PEM (pulse energy mode) enables 80% plus efficiency with I_O = 10mA (V_{IN} = 12V, V_O = 5V)
- Up to 95% efficiency
- Internal soft start
- Output voltage adjustable to 0.8 V
- 6A continuous output current
- 500kHz PWM operation at heavy load
- Cycle-by-cycle current limit
- Pre-bias start-up
- Short-circuit protection
- Thermal shutdown
- DFN5x6 package

Applications

- LCD TV
- Set top boxes
- DVD and Blu-ray players/recorders
- Cable modems

Typical Application

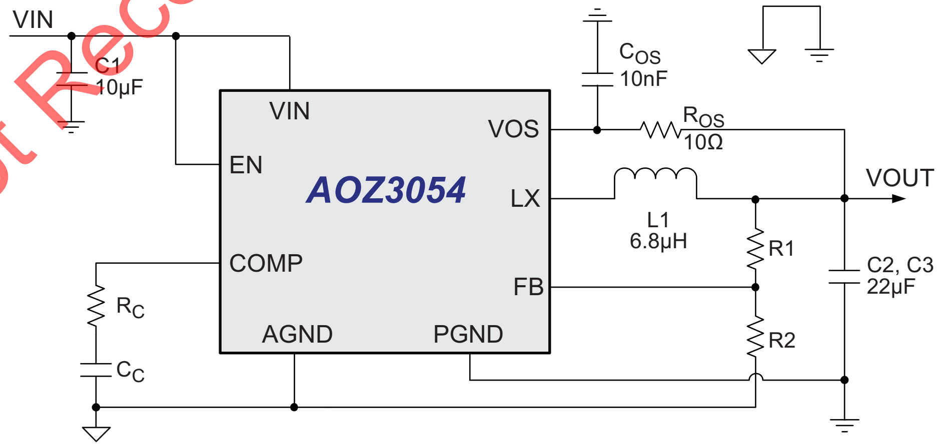


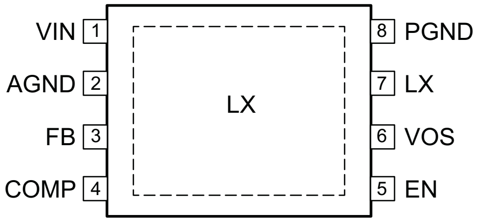
Figure 1. 5V, 6A Synchronous Buck Regulator, Fs = 500kHz

Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ3054DI	-40 °C to +85 °C	DFN5x6-8L	Green Product

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

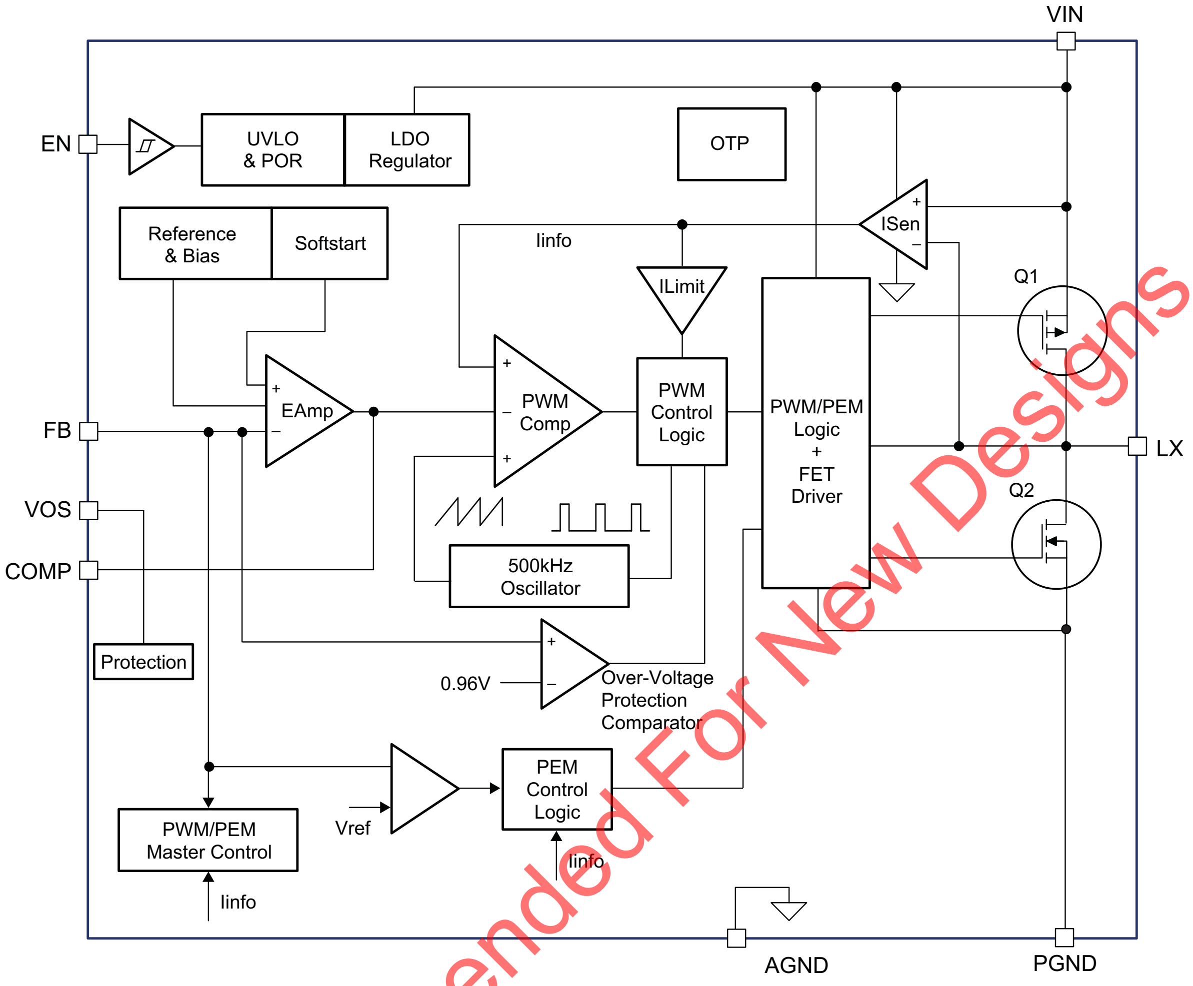


DFN5x6-8
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	VIN	Supply voltage input. When VIN rises above the UVLO threshold and EN is logic high, the device starts up.
2	AGND	Analog ground. AGND is the reference point for controller section. AGND needs to be electrically connected to PGND.
3	FB	Feedback input. The pin is used to set the output voltage via a resistive voltage divider between the output and AGND.
4	COMP	External loop compensation pin. Connect a RC network between COMP and AGND to compensate the control loop.
5	EN	Enable pin. Pull EN to logic high to enable the device. Pull EN to logic low to disable the device. If on/off control in not needed, connect EN to VIN and do not leave it open.
6	VOS	VO Sense pin for protection purpose and smart mode change adoption.
7	LX	Switching node.
8	PGND	Power ground. PGND needs to be electrically connected to AGND.
Exposed Pad	LX	Switching node. LX is the drain of the internal power PFET. LX is used as the thermal pad of the power stage.

Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
Supply Voltage (V_{IN})	20V
LX to AGND	-0.7V to V_{IN}+0.3V
LX to AGND (20 ns)	-5V to 22V
EN to AGND	-0.3V to V_{IN}+0.3V
VFB, VOS, COMP to AGND	-0.3V to 6V
PGND to AGND	-0.3V to +0.3V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating[1]	2.0kV

Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5 kΩ in series with 100 pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (V_{IN})	4.5V to 18V
Output Voltage Range	0.8V to 0.85*V_{IN}
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance DFN5x6 (Θ_{JA})	40°C/W

Electrical Characteristics

T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 5V unless otherwise specified$^{(2)}$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IN}	Supply Voltage		**4.5**		**18**	V
V_{UVLO}	Input Under-Voltage Lockout Threshold	V_{IN} Rising V_{IN} Falling		4.0 3.7		V V
I_{IN}	Supply Current (Quiescent)	V_{IN} = 12V, V_{FB} = 1.2 V, I_{OUT} = 0A		0.35	0.5	mA
I_{OFF}	Shutdown Supply Current	V_{EN} = 0 V		**1**	**2**	µA
V_{FB}	Feedback Voltage	T_A = 25 °C	0.788	0.8	0.812	V
R_O	Load Regulation			0.5		%
S_V	Line Regulation			1		%
I_{FB}	Feedback Voltage Input Current			10	200	nA
V_{EN}	EN Input Threshold	Off Threshold On Threshold	 **2**		**0.6**	V V
V_{HYS}	EN Input Hysteresis			200		mV
I_{EN}	EN Leakage Current			**0.1**	**1**	µA
t_{SS}	SS Time			6		ms
MODULATOR						
f_O	Frequency	Heavy Load	400	500	600	kHz
D_{MAX}	Maximum Duty Cycle			85		%
T_{MIN}	Controllable Minimum On-Time	Heavy Load		120		ns
g_{m_CS}	Current Sense Transconductance			8		A / V
g_{m_EA}	Error Amplifier Transconductance			200		µA / V
PROTECTION						
I_{LIM}	Current Limit		6.5	7.5		A
T_{OTP}	Over-Temperature Shutdown Limit	T_J Rising T_J Falling		150 100		°C °C
V_{OVP}	Over-Voltage Protection	Off Threshold On Threshold		960 860		mV mV
OUTPUT STAGE						
R_H	High-Side Switch On-Resistance	V_{IN} = 12 V		30		mΩ
R_L	Low-Side Switch On-Resistance	V_{IN} = 12 V		15		mΩ

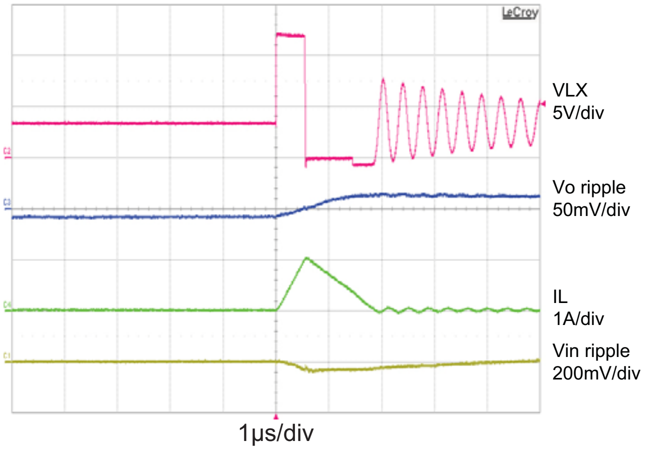
Note:

2. Specification in **BOLD** indicate an ambient temperature range of -40°C to +85°C. These specifications are not guaranteed to operate beyond the Maximum Operating ratings.

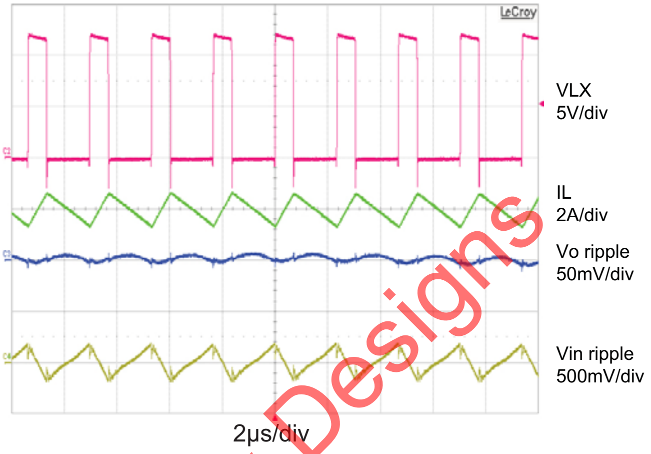
Typical Performance Characteristics

Circuit of Figure 1. T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3 V unless otherwise specified.

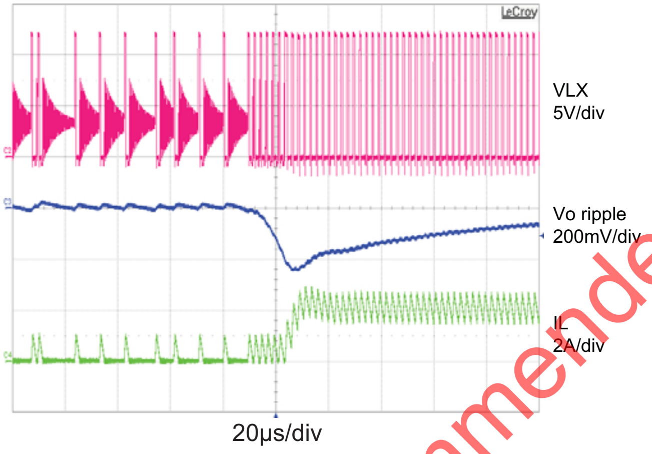
Light Load Operation



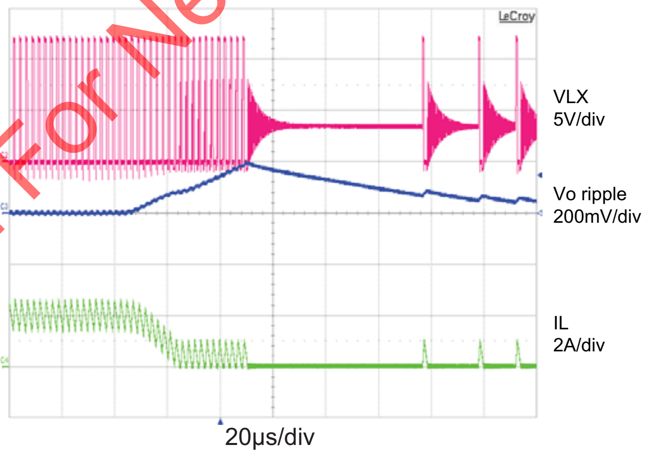
Full Load Operation



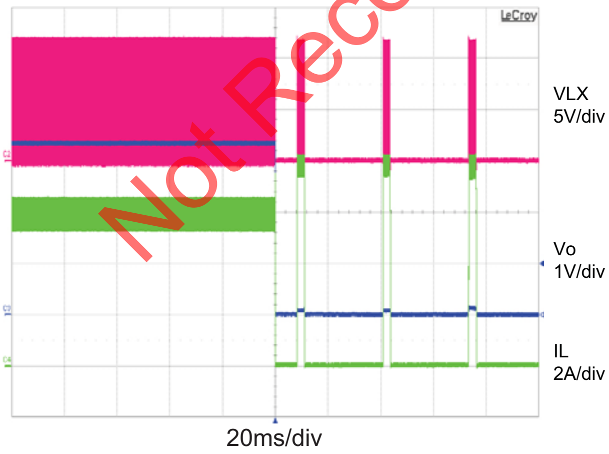
Light Load to Heavy Load Operation



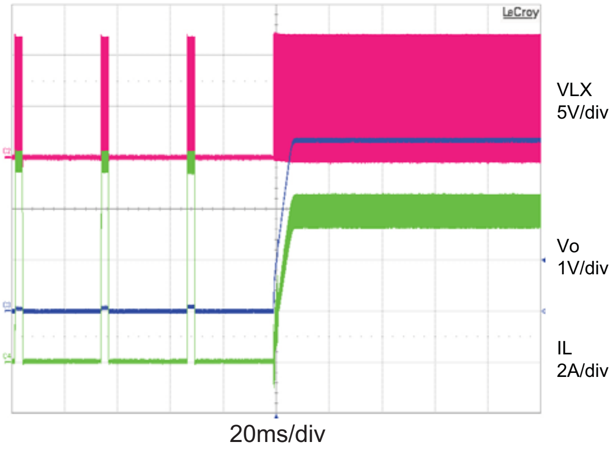
Heavy Load to Light Load Operation



Short Circuit Protection



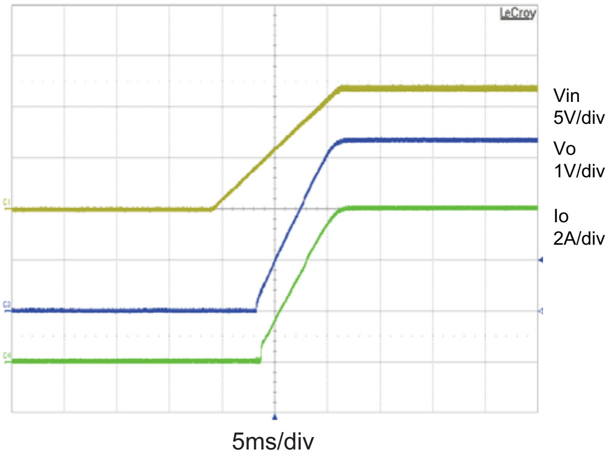
Short Circuit Recovery



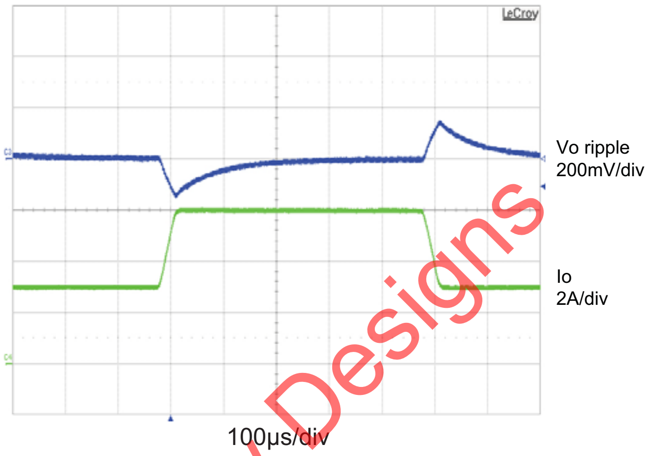
Typical Performance Characteristics *(Continued)*

Circuit of Figure 1. T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3 V unless otherwise specified.

Start Up to Full Load

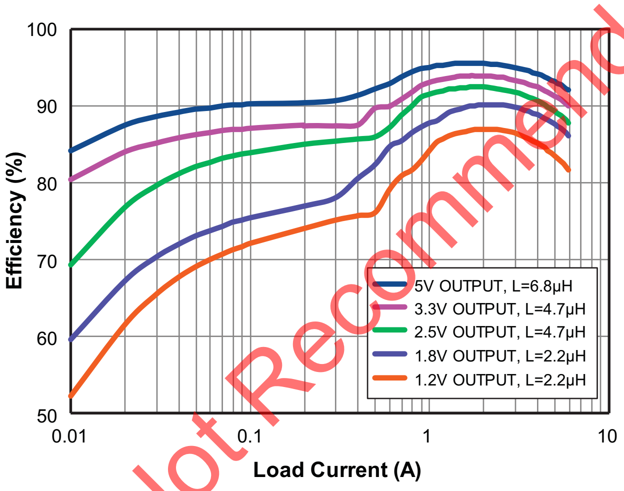


50 % to 100 % Load Transient

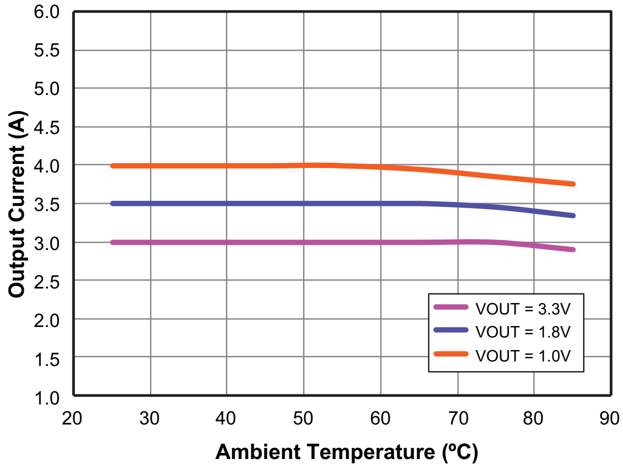


Efficiency

Efficiency (V_{IN} = 12V) vs. Load Current



Derating at 5V Input (V_{OS} = 0V) vs. Temperature



Detailed Description

The AOZ3054DI is a current-mode step down regulator with an integrated high-side PMOS switch and a low-side NMOS switch. The AOZ3054DI operates from a 4.5V to 18V input voltage range and supplies up to 6A of load current. Features include enable control, power-on reset, input under voltage lockout, output over voltage protection, external soft start and thermal shut down.

The AOZ3054DI is available in a DFN5x6 package.

Enable and Soft Start

The AOZ3054DI has an internal soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulation voltage. The soft start process begins when the input voltage rises to 4.1V and voltage on the EN pin is HIGH. In the soft start process, the output voltage is typically ramped to regulation voltage in 6ms. The 6ms soft start time is set internally.

The EN pin of the AOZ3054DI is active high. Connect the EN pin to VIN if the enable function is not used. Pulling EN to ground will disable the AOZ3054DI. Do not leave EN open. The voltage on the EN pin must be above 2V to enable the AOZ3054DI. When the EN pin voltage falls below 0.6V, the AOZ3054DI is disabled.

VOS Setting

V_O Sense pin can be set for protection purpose. COMP protection is active when $V_{OS} > 2.4V$, or else COMP protection will be disabled. V_O Sense pin can also be set for 2nd UVLO. When $V_{IN} > 8.3V$ and $V_{OS} > 2.4V$, the UVLO will be set to 7.2V rising and 6.5V falling, or else the UVLO is default to 4V rising and 3.7V falling.

The V_O Sense pin is suggested to connect to output or GND.

PEM Operation

When $V_{OS} > 2.4V$, AOZ3054DI will operate with pulse energy mode at light load to obtain high efficiency. When $V_{OS} < 2.4V$, PEM is active only when $V_{IN} > 8.3V$. In pulse energy mode, the PWM will not turn off until the inductor current reaches to 800mA and the current signal exceeds the error voltage.

PWM Operation

When $V_{IN} < 7V$ and $V_{OS} < 2.4V$, or under heavy load steady-state conditions, the converter operates in fixed frequency and Continuous Conduction Mode (CCM).

The AOZ3054DI integrates an internal PMOS as the high-side switch. Inductor current is sensed by amplifying the voltage drop across the drain to source of the high-side power MOSFET. Output voltage is divided down by the external voltage divider at the FB pin. The difference of the FB pin voltage and reference voltage is amplified by the internal transconductance error amplifier. The error voltage, which shows on the COMP pin, is compared against the current signal, which is the sum of inductor current signal and ramp compensation signal, at the PWM comparator input. If the current signal is less than the error voltage, the internal high-side switch is on. The inductor current flows from the input through the inductor to the output. When the current signal exceeds the error voltage, the high-side switch is off. The inductor current is freewheeling through the internal low-side NMOS switch to output. The internal adaptive FET driver guarantees no turn on overlap of both the high-side and the low-side switch.

Compared with regulators using freewheeling Schottky diodes, the AOZ3054DI uses a freewheeling NMOS to realize synchronous rectification. This greatly improves the converter efficiency and reduces power loss in the low-side switch.

The AOZ3054DI uses a P-Channel MOSFET as the high-side switch. This saves the bootstrap capacitor normally seen in a circuit using an NMOS switch.

Output Voltage Programming

Output voltage can be set by feeding back the output to the FB pin using a resistor divider network as shown in Figure 1. The resistor divider network includes R_1 and R_2. Usually, a design is started by picking a fixed R_2 value and calculating the required R_1 with the equation below:

$$V_O = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Some standard value of R_1 and R_2 for the most common output voltages are listed in Table 1.

Table 1.

V_O (V)	R_1 (kΩ)	R_2 (kΩ)
0.8	1.0	Open
1.2	4.99	10
1.5	10	11.5
1.8	12.7	10.2
2.5	21.5	10
3.3	31.1	10
5.0	52.3	10

The combination of R_1 and R_2 should be large enough to avoid drawing excessive current from the output, which will cause power loss.

Protection Features

The AOZ3054DI has multiple protection features to prevent system circuit damage under abnormal conditions.

Over Current Protection (OCP)

The sensed inductor current signal is also used for over current protection. Since the AOZ3054DI employs peak current mode control, the peak inductor current is automatically limited
cycle-by-cycle.

AOZ3054DI also has internal short-circuit protection to prevent catastrophic failure under output short conditions. When the FB pin voltage is below 0.2V after half soft start time, the short-circuit protection circuit is triggered and device will stop switching. The AOZ3054DI will enter hiccup mode if the over current or output short conditions continue.

AOZ3054DI. The measured inductor current is compared against a preset voltage which represents the current limit. When the output current is greater than the current limit, the high-side switch will be turned off. The converter will initiate a soft start once the over-current condition is resolved.

Power-On Reset (POR)

A power-on reset circuit monitors the input voltage. When the input voltage exceeds UVLO rising point, the converter starts operation. When input voltage falls below UVLO falling point, the converter will be shut down.

AOZ3054DI provides two kinds of UVLO threshold. When V_{IN} > 8.2V and V_{OS} > 2.4V, the UVLO will be set to 7.2V rising and 6.5V falling, or else the UVLO is default to 4V rising and 3.7V falling.

Thermal Protection

An internal temperature sensor monitors the junction temperature. The sensor shuts down the internal control circuit and high-side PMOS if the junction temperature exceeds 150 °C. The regulator will restart automatically under the control of the soft-start circuit when the junction temperature decreases to 100 °C.

Application Information

The basic AOZ3054DI application circuit is show in Figure 1. Component selection is explained below.

Input Capacitor

The input capacitor must be connected to the VIN and the PGND pins of AOZ3054DI to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}}\left(1 - \frac{V_O}{V_{IN}}\right)}$$

if we let *m* equal the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relationship between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure 2 below. It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is 0.5 x I_O.

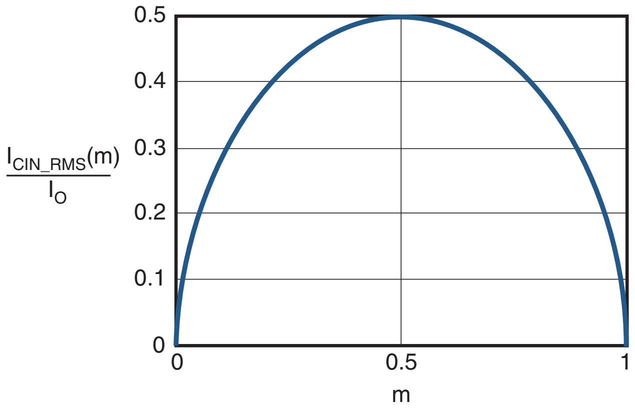


Figure 2. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have a current rating higher than I_{CIN_RMS} at the worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high current rating. Depending on the application circuits, other low ESR tantalum capacitors may be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors should be used for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures are based on a certain operating life time. Further de-rating may be necessary for practical design.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For a given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is:

$$\Delta I_L = \frac{V_O}{f \times L} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{Lpeak} = I_O + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on the inductor is designed to be 20% to 40% of output current.

When selecting the inductor, confirm it is able to handle the peak current without saturation at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on the inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. However, they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_O = \Delta I_L \times \left(ESR_{CO} + \frac{1}{8 \times f \times C_O}\right)$$

where,

C_O is output capacitor value, and

ESR_{CO} is the equivalent series resistance of the output capacitor.

When a low ESR ceramic capacitor is used as the output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = \Delta I_L \times \frac{1}{8 \times f \times C_O}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_O = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum capacitors are recommended as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, the output capacitor could be overstressed.

Loop Compensation

The AOZ3054DI employs peak current mode control for ease of use and fast transient response. Peak current mode control eliminates the double pole effect of the output L&C filter. It also greatly simplifies the compensation loop design.

With peak current mode control, the buck power stage can be simplified to be a one-pole and one-zero system in frequency domain. The pole is dominant pole can be calculated by:

$$f_{P1} = \frac{1}{2\pi \times C_O \times R_L}$$

The zero is a ESR zero due to the output capacitor and its ESR. It is can be calculated by:

$$f_{Z1} = \frac{1}{2\pi \times C_O \times ESR_{CO}}$$

where;

C_O is the output filter capacitor, R_L is load resistor value, and ESR_{CO} is the equivalent series resistance of output capacitor.

The compensation design shapes the converter control loop transfer function for the desired gain and phase. Several different types of compensation networks can be used with the AOZ3054DI. For most cases, a series capacitor and resistor network connected to the COMP pin sets the pole-zero and is adequate for a stable high-bandwidth control loop.

In the AOZ3054DI, FB and COMP are the inverting input and the output of the internal error amplifier. A series R and C compensation network connected to COMP provides one pole and one zero. The pole is:

$$f_{P2} = \frac{G_{EA}}{2\pi \times C_C \times G_{VEA}}$$

where;

G_{EA} is the error amplifier transconductance, which is 200 x 10^{-6} A/V, G_{VEA} is the error amplifier voltage gain, which is 500 V/V, and C_C is the compensation capacitor in Figure 1.

The zero given by the external compensation network, capacitor C_C and resistor R_C, is located at:

$$f_{Z2} = \frac{1}{2\pi \times C_C \times R_C}$$

To design the compensation circuit, a target crossover frequency f_C to close the loop must be selected. The system crossover frequency is where the control loop has unity gain. The crossover is the also called the converter bandwidth. Generally a higher bandwidth means faster response to load transients. However, the bandwidth should not be too high because of system stability concern. When designing the compensation loop, converter stability under all line and load condition must be considered.

Usually, it is recommended to set the bandwidth to be equal or less than 1/10 of the switching frequency.

The strategy for choosing R_C and C_C is to set the cross over frequency with R_C and set the compensator zero with C_C. Using selected crossover frequency, f_C, to calculate R_C:

$$R_C = f_C \times \frac{V_O}{V_{FB}} \times \frac{2\pi \times C_C}{G_{EA} \times G_{CS}}$$

where;

f_C is the desired crossover frequency. For best performance, f_C is set to be about 1/10 of the switching frequency, V_{FB} is 0.8V, G_{EA} is the error amplifier transconductance, which is 200 x 10^{-6} A/V, and G_{CS} is the current sense circuit transconductance, which is 8 A/V.

The compensation capacitor C_C and resistor R_C together make a zero. This zero is put somewhere close to the dominate pole f_{p1} but lower than 1/5 of the selected crossover frequency. C_C can is selected by:

$$C_C = \frac{1.5}{2\pi \times R_C \times f_{P1}}$$

The above equation can be simplified to:

$$C_C = \frac{C_O \times R_L}{R_C}$$

An easy-to-use application software which helps to design and simulate the compensation loop can be found at www.aosmd.com.

Thermal Management and Layout Considerations

In the AOZ3054DI buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the VIN pin, to the LX pad, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high-side switch is on. The second loop starts from inductor, to the output capacitors and load, to the low-side NMOS. Current flows in the second loop when the low-side NMOS is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is strongly recommended to connect input capacitor, output capacitor, and PGND pin of the AOZ3054DI.

In the AOZ3054DI buck regulator circuit, the major power dissipating components are the AOZ3054DI and the output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total\_loss} = V_{IN} \times I_{IN} - V_O \times I_O$$

The power dissipation of inductor can be approximately calculated by output current and DCR of inductor.

$$P_{inductor\_loss} = I_O^2 \times R_{inductor} \times 1.1$$

The actual junction temperature can be calculated with power dissipation in the AOZ3054DI and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total\_loss} - P_{inductor\_loss}) \times \Theta_{JA}$$

The maximum junction temperature of AOZ3054DI is 150ºC, which limits the maximum load current capability. Please see the thermal de-rating curves for maximum load current of the AOZ3054DI under different ambient temperatures.

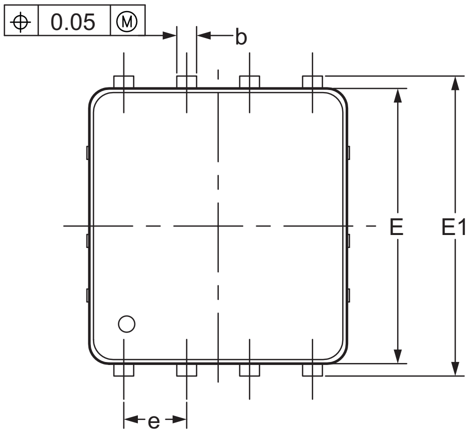
The thermal performance of the AOZ3054DI is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

Layout Considerations

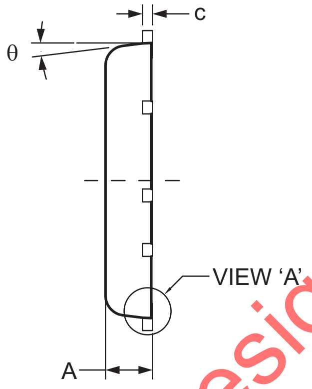
The AOZ3054DI is a DFN5x6 package. Layout tips are listed below for the best electric and thermal performance.

1. The exposed pad (LX) is connected to internal PFET and NFET drains. Connect a large copper plane to the LX pin to help thermal dissipation.
2. Do not use thermal relief connection to the VIN and the PGND pins. Pour a maximized copper area to the PGND and the VIN pins to help thermal dissipation.
3. Input capacitor should be connected as close as possible to the VIN and the PGND pins.
4. A ground plane is suggested. If a ground plane is not used, separate PGND from AGND and connect them only at one point to avoid the PGND pin noise coupling to the AGND pin.
5. Make the current trace from the LX pin to L to CO to the PGND as short as possible.
6. Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, GND or VOUT.
7. Keep sensitive signal traces far away from the LX pad.

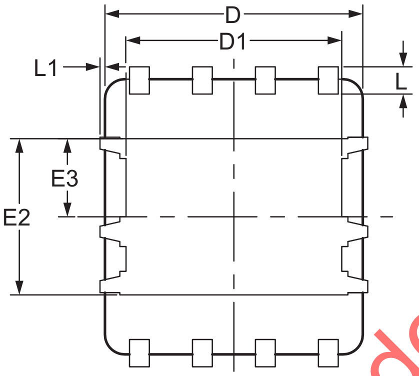
Package Dimensions, DFN5x6, 8L, EP1_P



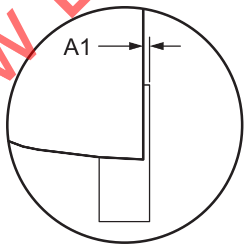
TOP VIEW



SIDE VIEW

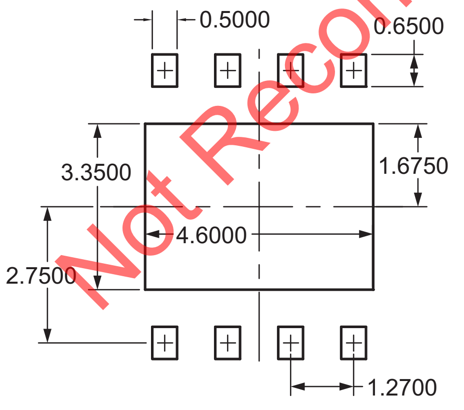


BOTTOM VIEW



VIEW 'A'
(SCALE 5:1)

RECOMMENDED LAND PATTERN



UNIT: mm

Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.85	0.95	1.00
A1	0.00	—	0.05
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	5.20 BSC		
D1	4.35 BSC		
E	5.55 BSC		
E1	6.05 BSC		
E2	3.15 BSC		
E3	1.575 BSC		
e	1.27 BSC		
L	0.45	0.55	0.65
L1	0	—	0.15
θ	0°	—	10°

Dimensions in inches

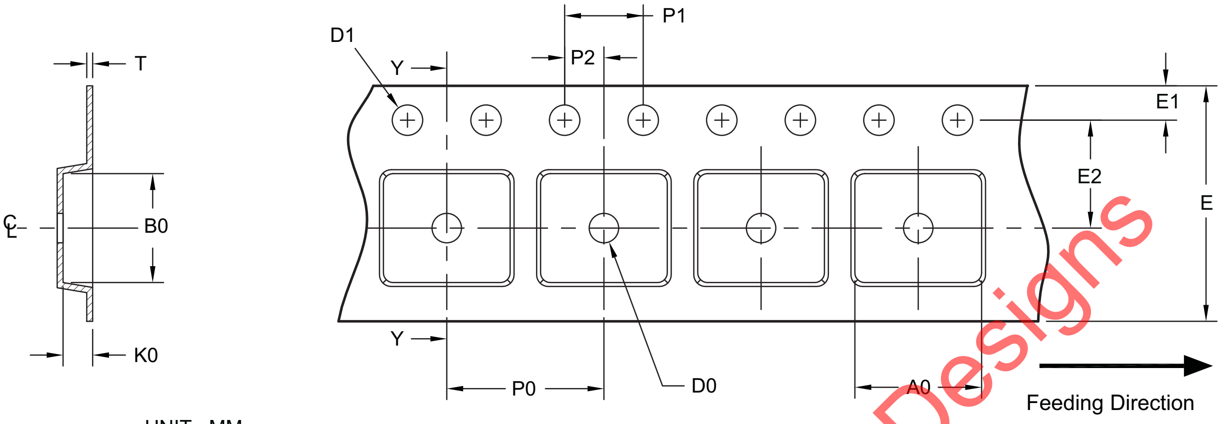
Symbols	Min.	Nom.	Max.
A	0.033	0.037	0.039
A1	0.000	—	0.002
b	0.012	0.016	0.020
c	0.006	0.008	0.010
D	0.205 BSC		
D1	0.171 BSC		
E	0.219 BSC		
E1	0.238 BSC		
E2	0.124 BSC		
E3	0.062 BSC		
e	0.050 BSC		
L	0.018	0.022	0.026
L1	0	—	0.006
θ	0°	—	10°

Notes:

1. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils each.
2. Controlling dimension is millimeter. Converted inch dimensions are not necessarily exact.

Tape and Reel Dimensions, DFN5x6

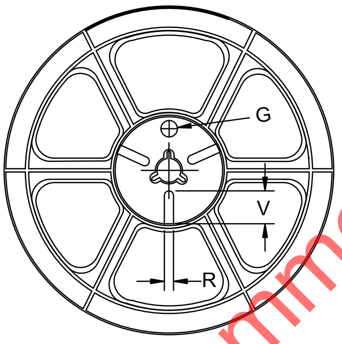
Carrier Tape

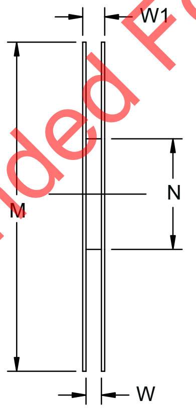


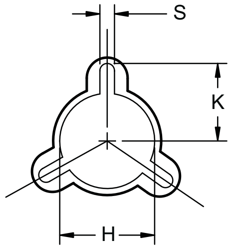
UNIT: MM

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN 5x6 (12mm)	6.30 ±0.10	5.45 ±0.10	1.30 ±0.10	1.50 Min.	1.55 ±0.05	12.00 ±0.30	1.75 ±0.10	5.50 ±0.10	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.30 ±0.05

Reel



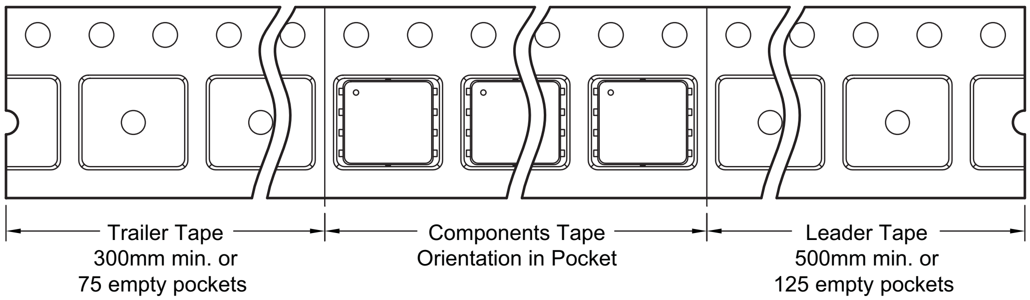




UNIT: MM

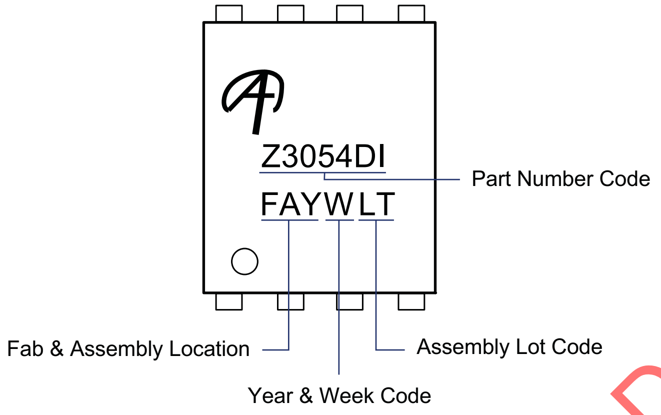
Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.0 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.0 +0.50/-0.20	10.60	2.0 ±0.5	—	—	—

Leader/Trailer and Orientation



Part Marking

AOZ3054DI
(DFN5x6, 8L)



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.