

# AOZ52371QI

High-Current, High-Performance Smart Power Stage

### **General Description**

The AOZ52371QI is a general-purpose Smart Power Stage (SPS) for computing notebook CPU power, consisting of two asymmetrical MOSFETs and an integrated driver for high current, high frequency, and DC-DC converter.

The AOZ52371QI provides an output current signal (IMON). The IMON signal can be directly used to replace inductor DCR sensing or resistor sensing in the multiphase voltage regulator systems without the need for temperature compensation.

The AOZ52371QI also includes an accurate module thermal monitor (TMON). TMON is a voltage sourced PTAT signal with a gain of 8 mV/°C.

The MOSFETs are individually optimized for operation in the synchronous buck configuration. The high side MOSFET is optimized to achieve low capacitance and gate charge for fast switching with low duty cycle operation. The low side MOSFET has ultra-low ON resistance to minimize conduction loss. The standard 5 mm × 5 mm QFN package is optimally designed to minimize parasitic inductance for minimal EMI signature.

### **Features**

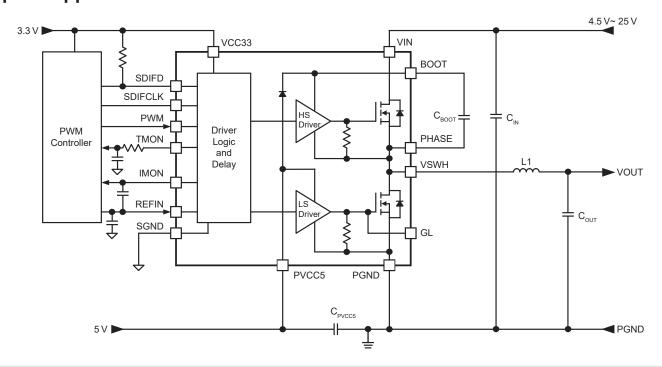
- 4.5 V to 25 V power supply range
- 60A continuous output current
  - Up to 80A for 10 ms on pulse
  - Up to 120A for 10 µs on pulse
- Optimized for switching frequency up to 1 MHz
- Integrated current monitor output signal
- Integrated temperature monitor output signal
- Fault Indicator
- VCC33 and PVCC5 Under-Voltage Lockout (UVLO)
- Zero Current Detect Function
- Over Temperature Protection
- Standard 5 mm x 5 mm QFN-30L package

### **Applications**

- Notebook computer
- Graphic card
- Communications Infrastructure



### **Typical Application**





# **Ordering Information**

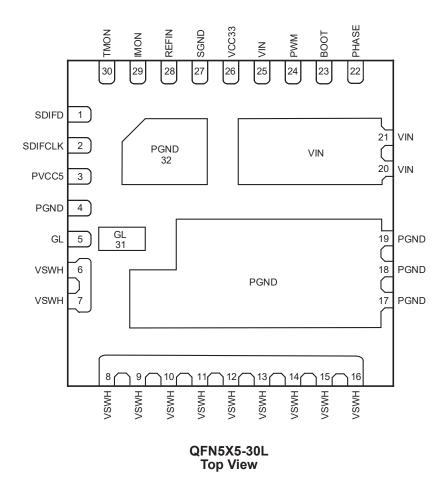
Part Number	AmbientTemperature Range	Package	Environmental
AOZ52371QI	-40°C to +125°C	QFN5x5-30L	RoHS

#### Contact local sales office for full product datasheet.



AOS products are offered in packages with Pb-free plating and compliant to RoHS standards. Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

### **Pin Configuration**



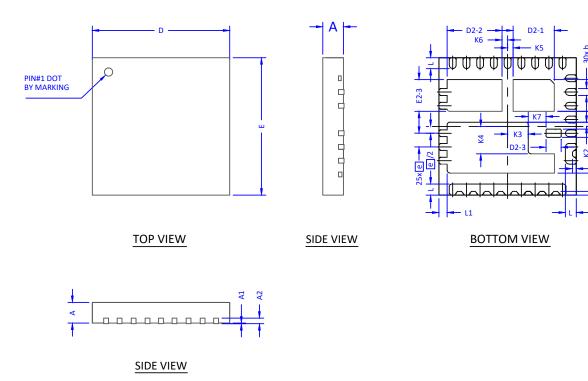


# **Pin Description**

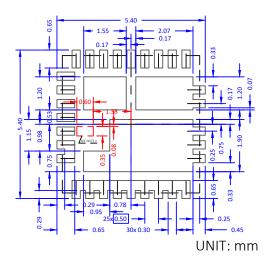
Pin Number	Pin Name	Pin Function			
1	SDIFD	Serial Digital Interface data input and output. Connect $1k\Omega$ to $3.3V$ .			
2	SDIFCLK	Serial Digital Interface clock input.			
3	PVCC5	5 V Power Rail for High-Side and Low-Side MOSFET. Place a high quality low ESR ceramic capacitor (~ 1 μF / X7R) directly between PVCC5 and PGND (Pin 4).			
4, 32	PGND	Power Ground for High-Side and Low-Side MOSFET Gate Drivers. Ensure to connect 1 µF directly between PGND and PVCC5 (Pin 3).			
5, 31	GL	Low-Side MOSFET Gate connection. This is for test purposes only.			
6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16	VSWH	Switching node connected to the Source of High-Side MOSFET and the Drain of Low-Side MOSFET.			
17, 18, 19	PGND	Power Ground pin for power stage (Source connection of Low-Side MOSFET).			
20, 21, 25	VIN	Power stage High Voltage Input (Drain connection of High-Side MOSFET).			
22	PHASE	This pin is dedicated for bootstrap capacitor AC return path connection from BOOT (Pin 23).			
23	воот	High-Side MOSFET Gate Driver supply rail. Connect a 100 nF ceramic capacitor between BOOT and the PHASE (Pin 22).			
24	PWM	PWM input signal from Controller IC. This input is compatible with 3.3 V Tri-State logic level.			
26	VCC33	3.3 V Bias for Internal Logic Blocks. Place a high quality low ESR ceramic capacitor (~ 1 µF / X7R) directly between VCC33 and SGND (Pin 27).			
27	SGND	Signal Ground.			
28	REFIN	Input for external reference voltage for IMON (Pin 28). This voltage should be between $0.8\mathrm{V}$ ar $1.3\mathrm{V}$ . Connect this pin to the appropriate current sense input of the controller. Place a low ESR ceramic capacitor ( $\sim 0.1\mu\mathrm{F}$ ) from REFIN to SGND (Pin 27).			
29	IMON	Current Monitor output signal referenced to REFIN (Pin 28). This pin is pulled high to VCC33 to indicate an over-temperature and/or PVCC5 UVLO fault. This pin is pulled to REFIN (Pin 28) to indicate VCC33 UVLO condition. Connect the IMON output to the appropriate current sense input of the controller. No more than 56 µF capacitance can be directly connected across the IMON and REFIN.			
30	TMON	Temperature Monitor output signal. For multiphase, the TMON pins can be connected together as a common bus. The highest voltage indicating highest temperature is sent to the controller. No more than 470 pF total capacitance can be directly connected across TMON and SGND (Pin 27). Higher capacitance is allowed with a series resistor, such as $1\mathrm{k}\Omega$ for a $100\mathrm{n}\mathrm{F}$ load.			



# Package Dimensions, QFN5x5-30L



#### **RECOMMENDED LAND PATTERN**



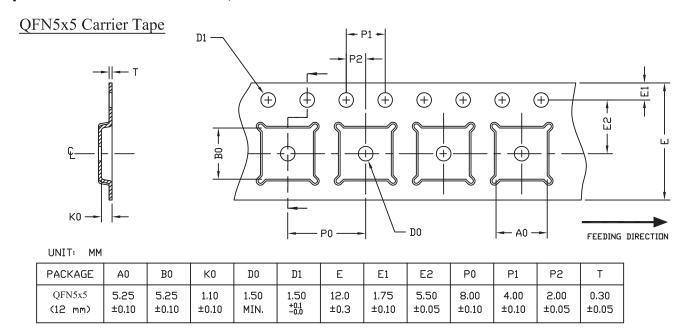
SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
Α	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2	0.20 REF			0.008REF		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	4.90	5.00	5.10	0.193	0.197	0.201
D2-1	1.45	1.50	1.55	0.057	0.059	0.061
D2-2	1.95	2.00	2.05	0.077	0.079	0.081
D2-3	0.50	0.55	0.60	0.020	0.022	0.024
е	0.50 BSC			0.020 BSC		
Е	4.90	5.00	5.10	0.193	0.197	0.201
E2-1	1.10	1.15	1.20	0.043	0.045	0.047
E2-2	1.80	1.85	1.90	0.071	0.073	0.075
E2-3	1.10	1.15	1.20	0.043	0.045	0.047
E2-4	0.25	0.30	0.35	0.010	0.012	0.014
F1	0.11	0.14	0.17	0.004	0.006	0.007
K1	0.55 ref.			0.022 ref.		
K2	0.15 ref.			0.006 ref.		
К3	0.75 ref.			0.030 ref.		
К4	1.00 ref.			0.039 ref.		
K5	0.20 ref.			0.008 ref.		
K6	0.20 ref.			0.008 ref.		
K7	0.65 ref.			0.026 ref.		
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.25	0.30	0.35	0.010	0.012	0.014

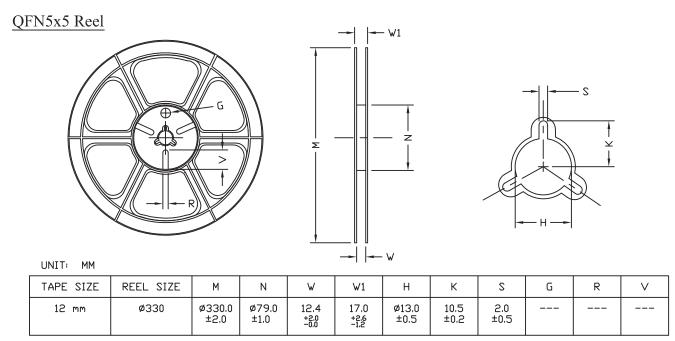
#### NOTE:

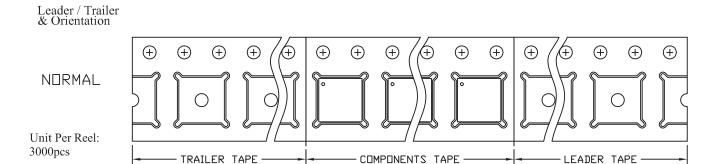
- 1. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
- 2. DOTTED OUTLINE IS GUIDELINE TO BE COMPATIBLE WITH INDUSTRY COMMON LAYOUT BUT NOT RECOMMENDED BY AOS.



# Tape and Reel Dimensions, QFN5x5-30L







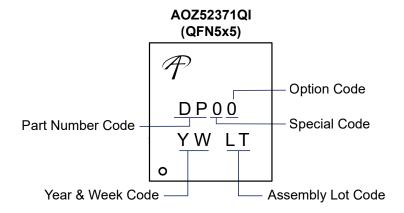
DRIENTATION IN POCKET

500 mm MIN. □R

300 mm MIN. □R



### **Part Marking**



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- 2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Rev. 1.0 June 2022 **www.aosmd.com** Page 6 of 6