AOZ5473QE

80A High-Performance Smart Power Stage (SPS)

General Description

The AOZ5473QE is a high efficiency synchronous buck smart power stage module consisting of two asymmetrical MOSFETs and an integrated driver. The MOSFETs are individually optimized for operation in the synchronous buck configuration. The high-side MOSFET is optimized to achieve low capacitance and gate charge for fast switching with low duty cycle operation. The low-side MOSFET has ultra-low ON resistance to minimize conduction loss.

Highly accurate current (IMON) and temperature (TMON) monitors are integrated in AOZ5473QE. AOS digital controllers, when used with AOZ5473QE, can digitize IMON and TMON to provide fault protection and telemetry via the digital communication bus. A dual functionality TMON/FLT pin reports temperature information during normal operating conditions and also reports OC, OT, HS-short, LS-short faults. When a fault is detected, the TMON/FLT pin is pulled high.

Dual-layer OC Protection includes a fixed 80 A detection level which enable an OC fault flag and a 100 A cycle-by-cycle current limit. This second-level protection turns off the high-side MOSFET, disabling the output. The AOZ5473QE protection also includes thermal shutdown.

The bootstrap switch, with auto boot refresh feature, is integrated into the driver. The low-side MOSFET can be driven into diode emulation mode to provide asynchronous operation when required. The pin-out is optimized for low inductance routing of the converter, keeping the parasitic effects to a minimum.

Features

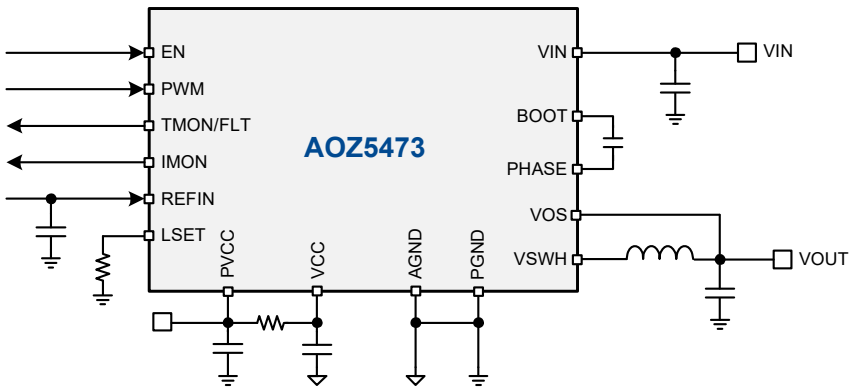
- 4.5V to 20V power supply range
- 80A of current handling capability
- Integrated bootstrap with auto refresh
- Up to 1 MHz switching operation
- 3.3V Tri-state PWM input compatible
- Fault detection
  - Under-Voltage Lockout (UVLO) on VCC
  - Over Current (OC)
  - Over Temperature (OT)
  - High-Side and Low-Side Short
- Thermal shutdown
- Cycle-by-cycle over current protection
- Integrated Current Monitor (IMON)
- Integrated Temperature Monitor (TMON)
- Low profile QFN5x6-39L package

Applications

- Server including processor and memory power
- Communications infrastructure systems
- High-current rails in server/cloud and storage systems
- Artificial intelligence and deep learning systems
- Single phase and multiphase POL
- GPU and gaming regulation

Green Product

Typical Application Circuit

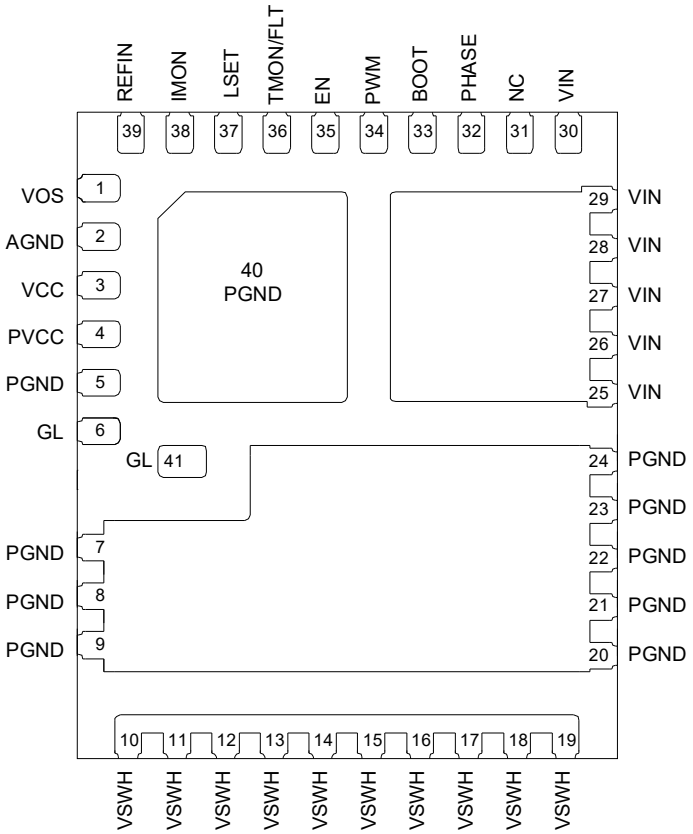


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ5473QE	-40°C to 125°C	QFN5x6-39L	RoHS

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.

Pin Configuration

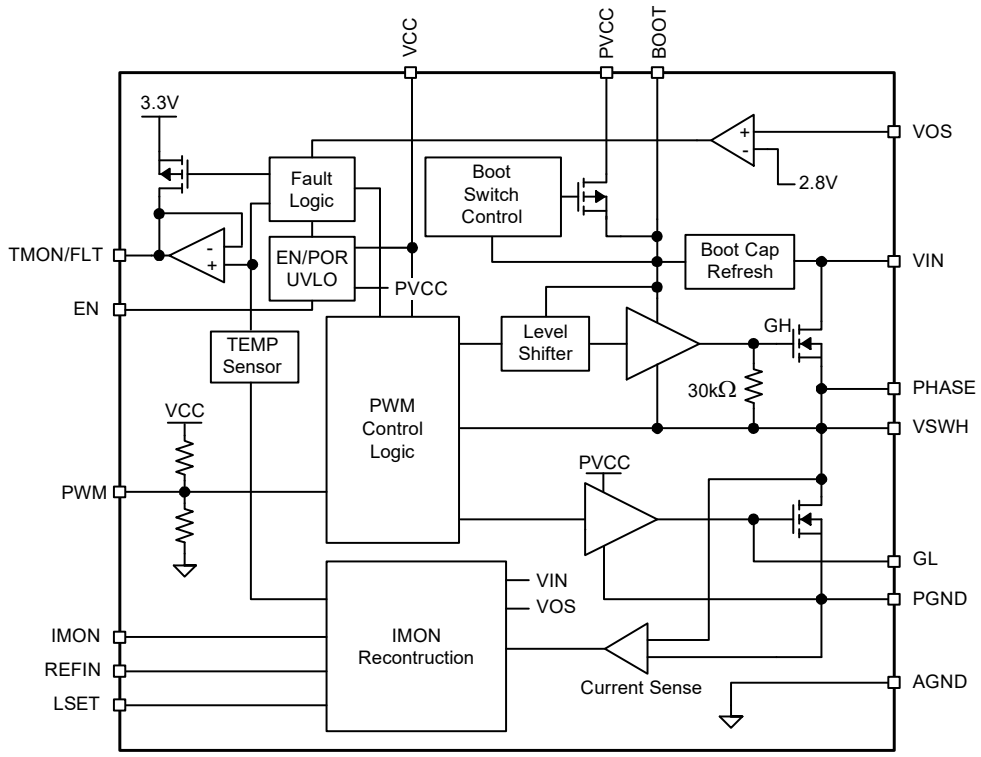


QFN5x6-39L
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	VOS	Connect this pin to output of the converter. VOUT voltage is used for a reconstruction of the IMON signal. This pin also supports pre-OV functionality when EN is low.
2	AGND	Reference Ground for 5 V Bias (VCC).
3	VCC	5V Bias for Internal Logic Blocks. Ensure to position a low ESR ceramic capacitor (~1 µF) MLCC directly between VCC (Pin 3) and AGND (Pin 2).
4	PVCC	5V Power Rail for high-side and low-side MOSFET Drivers. Ensure to position a low ESR ceramic capacitor (~1 µF) MLCC directly between PVCC (Pin 4) and PGND.
5, 40	PGND	Power Ground pin for 5 V Power Rail (Pin 4). Connect directly to system ground plane.
6, 41	GL	Low-side MOSFET Gate connection. This is for test purposes only.
7-9, 20-24	PGND	Power stage ground return and source connection of low-side MOSFET. Connect directly to system ground plane with as many thermal VIAs to the power ground exposed pad.
10-19	VSWH	Switching node connected to the source of high-side MOSFET and the drain of low-side MOSFET.
25-30	VIN	Input voltage connected to Drain pin of the high-side MOSFET. Connect Input bypass MLCC capacitor as close as possible to this pin.
31	NC	No Connect. This is for test purposes only. Pin is internally tied to PHASE
32	PHASE	This pin is dedicated for bootstrap capacitor connection to BOOT (pin 33).
33	BOOT	Floating bootstrap supply pin for the upper gate drive. Place a low ESR ceramic capacitor in close proximity across BOOT and PHASE (pin 32).
34	PWM	PWM input of gate driver. Compatible with 3.3V tri-state PWM signal.
35	EN	Enable pin for all MOSFET Driver functionality. When pulled low, the GH (Internal) and GL Outputs will be pulled low.
36	TMON/FLT	Temperature Monitor and FAULT Flag Pin. TMON/FLT will be pulled high (~3.3 V) to indicate a fault. For multi-phase, the TMON/FLT pin can be connected together as a common bus. The highest voltage (representing the highest temperature) will be sent to the PWM controller. No more than 470 pF total capacitance can be directly connected across TMON/FLT and AGND pin. A higher capacitance load is allowed with a series resistor (~1 kΩ) for 100 nF load. At 25°C and in normal operation, this pin should have an output voltage of 800 mV, having a gain of 8 mV/°C.
37	LSET	Connect a resistor to AGND to properly program the Inductor value for the reconstruction of IMON signal. Refer to current monitoring section in page 12 for recommended LSET resistor values.
38	IMON	Current Monitor Output. The pin provides a 5 mV/A signal, referenced to REFIN, proportional to the current delivered by the Power Stage.
39	REFIN	Reference Voltage Input for Current Reporting. Connect an external reference to offset the Current Monitor Output (IMON). Recommended REFIN range is 1.0 V to 2.0 V.

Functional Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameters	Ratings
Supply Voltage (PVCC, VCC)	-0.3V to 7V
Supply Voltage DC (VIN)	-0.3V to 25V
Switch Voltage AC < 20ns (VIN)	-0.3V to 32V
Switch Node Voltage DC (VSWH/PHASE)	-0.3V to 25V
Switch Node Voltage AC < 20ns (VSWH/PHASE)	-7V to 32V
Bootstrap Voltage (VBOOT-PGND)	-0.3V to 32V
Bootstrap Voltage (VBOOT-VSWH)	-0.3V to 7V
Control Pins (PWM, EN, TMON/FAULT, IMON, REFIN, LSET,VOS)	-0.3V to 7V
Output Current (I_{OUT_MAX})	80A
Low-Side Gate (GL)	-0.3V to PVCC + 0.3V
Pulsed Output Current ($I_{OUT-PEAK}$)	150A (<10 µs)
Storage Temperature (T_S)	-55°C to +150°C
Max Junction Temperature (T_J)	150°C
ESD Rating(1)	2.0kV

Notes:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1kΩ in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameters	Ratings
Supply Voltage (PVCC, VCC)	4.5V to 5.5V
Supply Voltage (VIN)	4.5V to 20V
Supply Voltage (REFIN)	1.0V to 2V
Operating Frequency (FSW)	100kHz to 1MHz
Operating Junction Temperature (T_J)	-40°C to +125°C
Package Thermal Resistance (θ_{JA}) Junction Ambient(2) (θ_{JC-PCB}) Junction Case PCB(2) (θ_{JC-TOP}) Junction Case TOP(3)	 12.0°C/W 1.5°C/W 10.4°C/W

Notes:

2. Measured in free air with device mounted on high thermal conductivity PCB.
3. Simulated in free air with device mounted on high thermal conductivity PCB.
4. Simulated with highly effective heat sink attached to the top of the package and no PCB on the bottom side.

Electrical Characteristics[4]

T_A = -40°C to 125°C. V_{IN} = 12V, P_{VCC} = V_{CC} = 5.0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.[5]	Typ.	Max.[5]	Units
I_{VCC} + I_{PVCC}	Supply Current	Non-Switching, EN=5V		6.8	8.4	mA
V_{CC_UVLO}	VCC UVLO Threshold	V_{CC} Rising	3.8	4.1	4.4	V
V_{CC_HYST}	VCC UVLO Hysteresis	V_{CC} Hysteresis, PVCC=VCC		0.3		V
Enable Input						
V_{EN_H}	Enable High Voltage	EN Rising	2.7			V
V_{EN_L}	Enable Low Voltage	EN Falling			0.6	V
t_{PD_ENH}	Propagation Delay	PWM = 0V, EN=V_{EN_H} to GL = 1V		1.7	2.7	µs
t_{PD_ENL}		PWM = 0V, EN=V_{EN_L} to GL = 4V		50		ns
R_{EN}	EN Pull-Down Resistance	EN=V_{EN_H} to GL = 4V		150		kΩ
PWM Input						
V_{PWM_H}	PWM Input High Threshold		2.7			V
V_{PWM_L}	PWM Input Low Threshold				0.6	V
V_{PWM_HiZ}	3-State Open Voltage	PWM Input Floating	1.35		1.65	V
V_{PWM_TRI}	PWM 3-Stage Window		1.25		1.95	
R_{PWM_UP}	PWM Pull-Up Resistance			82		kΩ
R_{PWM_DOWN}	PWM Pull-Down Resistance			35		kΩ
PWM Propagation Delays and Dead Time (f_{SW} = 500 kHz, I_{OUT} = 20A)						
t_{PDLL}	PWM High Propagation Delay	PWM High to GL Low		25		ns
t_{PDLU}	PWM Low Propagation Delay	PWM Low to VSWH Low		25		ns
t_{TSEXIT}	Existing 3-State Propagation Delay	PWM 3-State à High to GH(internal) High		30		ns
		PWM 3-State → Low to GL High		30		ns
t_{PDHU}	GL Low to VSWH High Deadtime	Note - 4	9	11.5	14	ns
t_{PDHL}	VSWH Low to GL High Deadtime		10	13	16	ns
t_{TSHO}	3-State Hold-Off Time			40		ns
$t_{PWM\_HIGH\_MIN}$	Forced Minimum PWM High			30		ns
$t_{PWM\_LOW\_MIN}$	Forced Minimum PWM Low			40		ns
Internal Bootstrap Switch						
V_{F_BOOT}	Bootstrap Diode Forward Voltage	PVCC to BOOT, I_{BOOT} = -20mA		725		mV
High-Side Driver						
R_{H_SRC}	Output Impedance, Sourcing	V_{BOOT}-V_{PHASE} = 5V, I_{GH}= -500mA		0.9		Ω
I_{H_SRC}	Peak Source Current			2		A
R_{H_SNK}	Output Impedance, Sinking	V_{BOOT}-V_{PHASE} = 5V, I_{GH} = 500mA		0.5		Ω
I_{H_SNK}	Peak Sink Current			3		A
RGH	Gate Pull Down Resister			30		kΩ
Low-Side Driver						
R_{L_SRC}	Output Impedance, Sourcing	PVCC = 5V, I_{GL} = -500mA		0.75		Ω
I_{L_SRC}	Peak Source Current			3		A
R_{L_SNK}	Output Impedance, Sinking	PVCC = 5V, I_{GL} = 500mA		0.4		Ω
I_{L_SNK}	Peak Sink Current			5		A

Electrical Characteristics[4]

T_A = -40°C to 125°C. V_{IN} = 12V, P_{VCC} = V_{CC} = 5.0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.[5]	Typ.	Max.[5]	Units
Temperature Sense Output and Fault Communications (TMON/FLT)						
V_{TMON_SLOPE}	TMON Voltage Slope	0°C ≤ T_J ≤ 150°C	7.8	8	8.2	mV/°C
V_{TMON}	TMON Voltage	T_A = T_J = 25°C	776	800	824	mV
I_{TMON_SRC}	TMON Source Current		1.2			mA
I_{TMON_SNK}	TMON Sink Current			20		µA
V_{FLT_HIGH}	Fault Mode Active High	Refer to Table 1 for the list of fault events	3			V
t_{D_FAULT}	Fault Reporting Delay				100	ns
Current Sense Output (IMON) Accuracy (PVCC = VCC = 5V, T_A= T_J = 25°C to 85°C)						
I_{MON_SLOPE}	IMON Slope	I_{OUT} = -20A to 50A	4.75	5	5.25	mV/A
	IMON Reporting Accuracy	I_{OUT} = 50 A (T_A = T_J = 25 °C to 105 °C)	237.5	250	262.5	mV
		I_{OUT} = 40 A (T_A = T_J = 25 °C to 125 °C)	190	200	210	mV
		I_{OUT} = 30 A (T_A = T_J = 25 °C to 125 °C)	142.5	150	157.5	mV
		I_{OUT} = 20 A (T_A = T_J = 25 °C)	95	100	105	mV
I_{MON_RANGE}	(IMON - REFIN) Range	REFIN + IMON ≤ 2.64V	-200		750	mV
FET-Short Fault Detection						
V_{HS_SHORT}	HS MOSFET Short Threshold	PWM = Low, VSWH Rising	375	500	625	V
V_{LS_SHORT}	LS MOSFET Short Threshold	PWM = High, VSWH Falling	1.5	2	1.5	V
Over-Temperature Protection						
T_{OTP_RISING}	Over Temp Rising Threshold	Driver IC Temperature		150		°C
T_{OTP_HYS}	OTP Hysteresis	Driver IC Temperature		20		°C
Preliminary Over-Voltage Protection						
V_{PREOVP}	OVP Reference Threshold			2.8		V
Over-Current Protection						
I_{OCP}	Constant Peak Over-current Threshold for a Fault Flag		74	80	86	A
$t_{D\_OCP\_FLT}$	OCP Fault Blanking Delay	PWM High → Low Cycles to TMON/ FLT High		10		cycle
I_{OCP_LIMIT}	Constant Peak Cycle-by-Cycle Over-Current Threshold for a Current Limit	Turn off HS MOSFET and turn on LS MOSFET		100	120	A

Notes:

5. Compliance to datasheet limits is assured by one or more methods: Production test, characterization, and/or design.

Timing Diagram

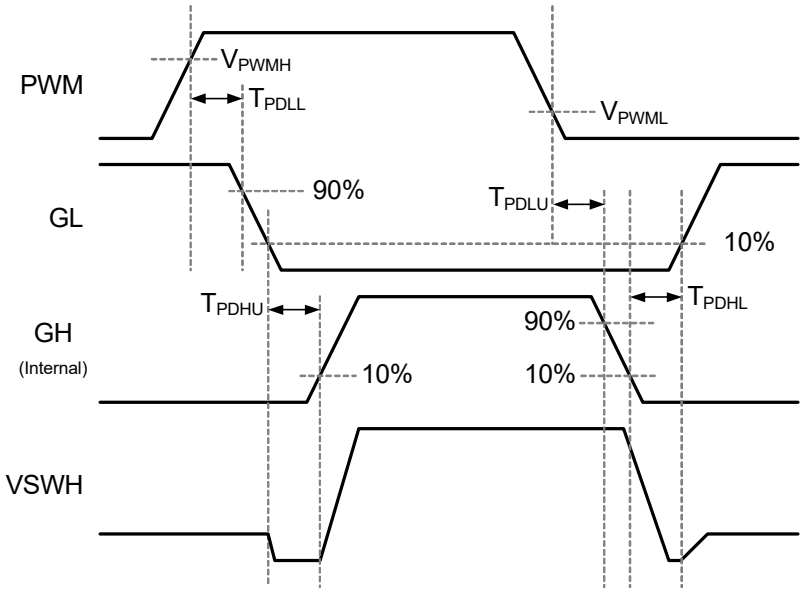


Figure 1. PWM Logic Input Timing Diagram

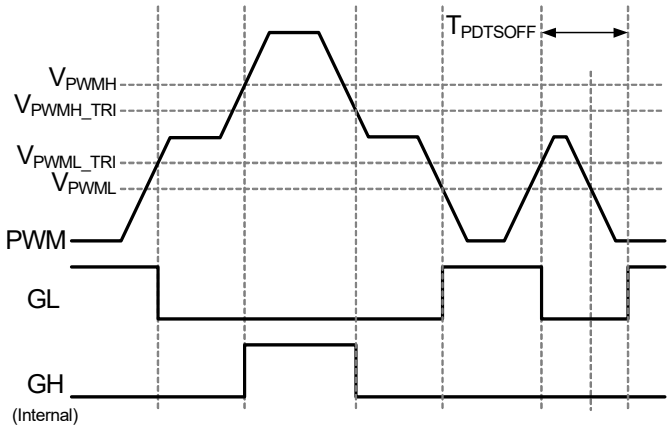


Figure 2. Tri-State Input Logic Timing Diagram

Typical Performance Characteristics

T_A = 25°C, V_{IN} = 12V, PV_{CC} = V_{CC} = 5V, unless otherwise specified. Inductor (180 nH, DCR = 0.18 mΩ) is not included in efficiency and power loss curves.

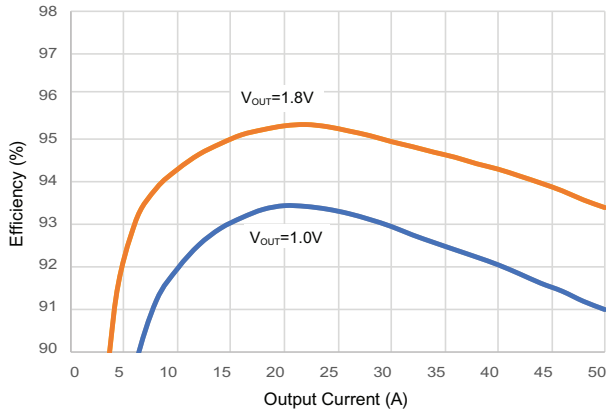


Figure 3. Power Efficiency vs. Output Current (fsw= 500 kHz)

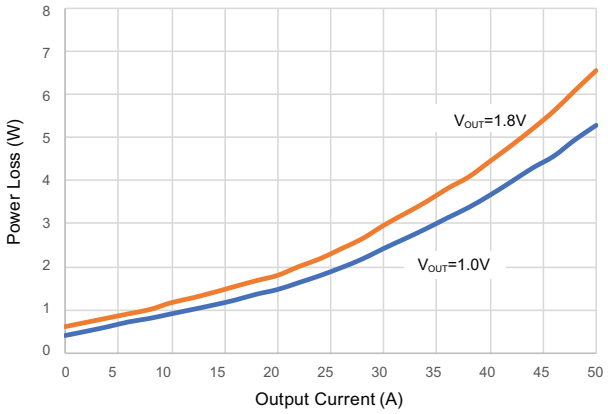


Figure 4. Power Loss vs. Output Current (fsw = 500 kHz)

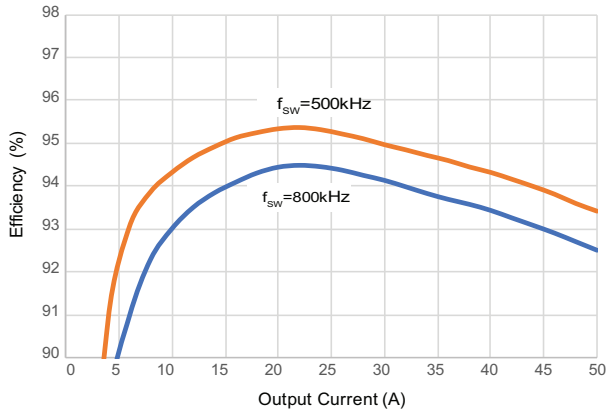


Figure 5. Power Efficiency vs. Output Current (VOUT = 1.8 V)

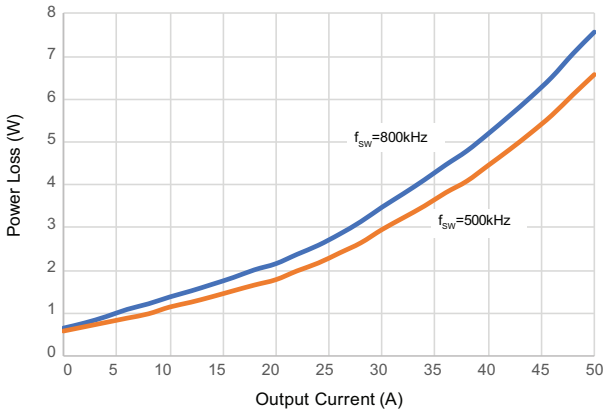


Figure 6. Power Loss vs. Output Current (VOUT = 1.8 V)

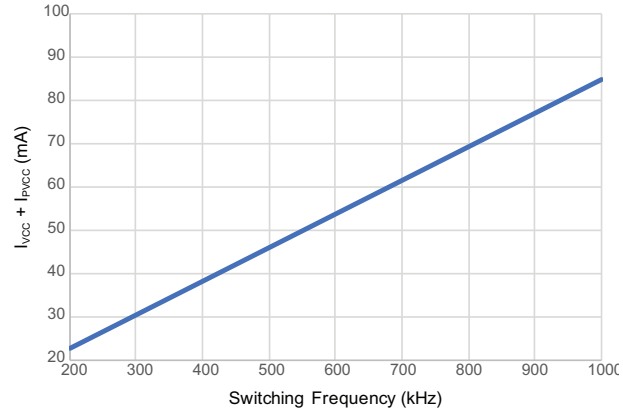


Figure 7. Supply Current (I_{PVCC} + I_{VCC}) vs. Switching Frequency

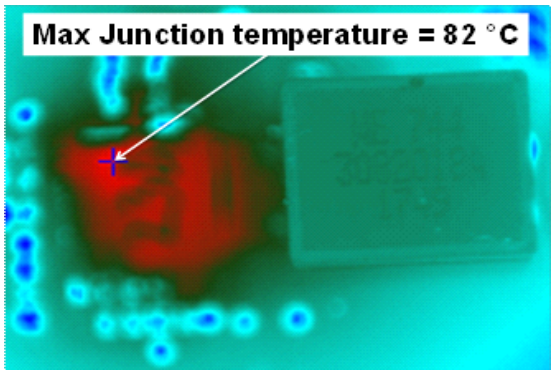


Figure 8. Thermal Image Captured on AOS Eval Board (V_{IN} = 12 V, V_{OUT} = 1 V, I_{OUT} = 40A, fsw = 500 kHz, L = 180 nH), T_A = 25 °C, No airflow

Typical Performance Characteristics

T_A = 25°C, V_{IN} = 12V, PV_{CC} = V_{CC} = 5V, unless otherwise specified. Inductor (180 nH, DCR = 0.18 mΩ) is not included in efficiency and power loss curves.

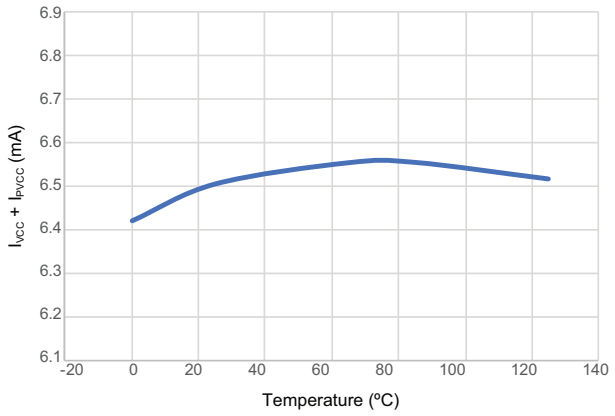


Figure 9. Supply Current (I_{VCC} + I_{PVCC} vs Temperature (non-switching)

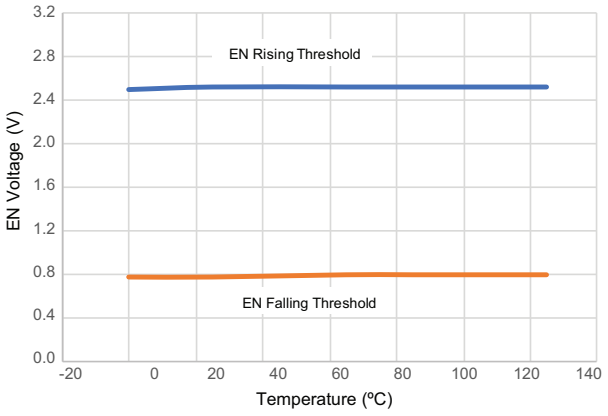


Figure 10. EN Threshold Voltage vs Temperature

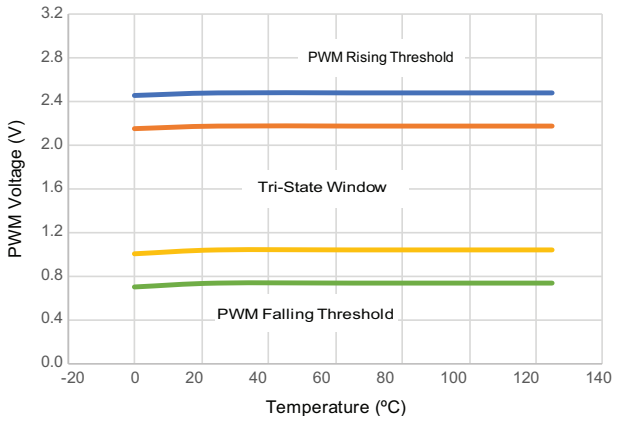


Figure 11. PWM Threshold Voltage vs Temperature

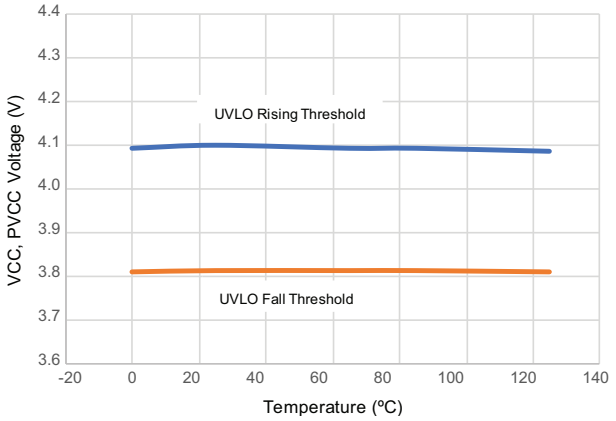


Figure 12. UVLO Threshold Voltage vs Temperature

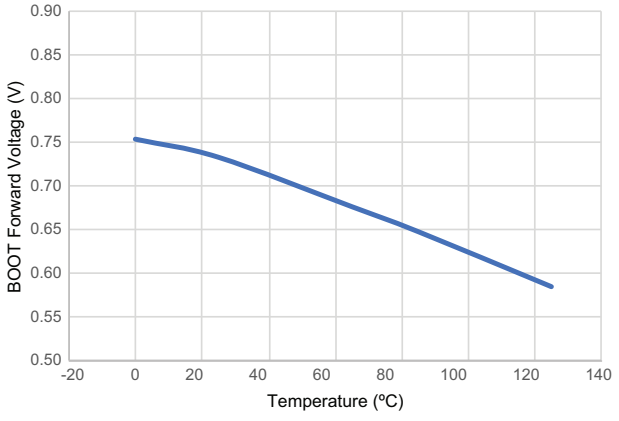


Figure 13. BOOT Forward Voltage vs Temperature

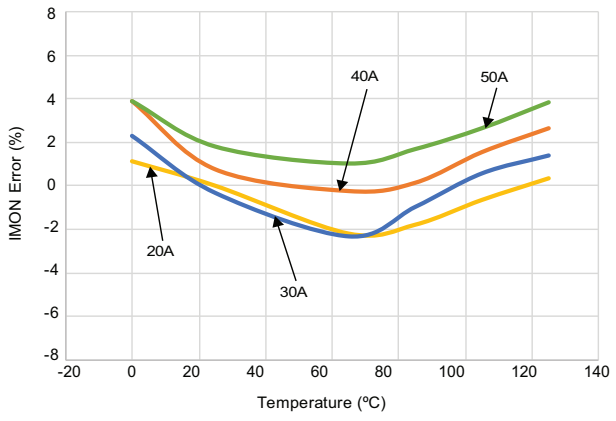


Figure 14. IMON Error vs Temperature

Application Information

AOZ5473QE is a fully integrated smart power module designed to work over an input voltage range of 4.5V to 20V with 5V supplies for gate drive and internal control circuits. A number of industry leading features are employed in this smart power stage module such as temperature compensated integrated current monitoring (IMON). Other features such as thermal reporting, high-side and low-side MOSFETs device short, Bias Voltage (VCC) under-voltage lockout (UVLO) and tri-state operation control for light load efficiency, are what makes the AOZ5473QE a highly versatile power module. The high-side and low-side power MOSFETs are combined in one package with the pinouts optimized for power routing with minimum parasitic inductance. The MOSFETs are individually tailored for efficient operation as either high-side or low-side switches in a low duty cycle synchronous buck converter. In addition, a high current driver is also included in the package which minimizes the gate drive loop resulting to extremely fast switching.

Powering the Module and the Gate Drives

An external supply PVCC of 5V is required for driving the MOSFETs. The MOSFETs are designed with low gate thresholds so that lower drive voltage can be used to reduce the switching and driving losses without compromising the conduction losses. The integrated gate driver is capable of supplying several amperes of peak current into the low-side MOSFET to achieve extremely fast switching. A ceramic bypass capacitor of 1uF or higher is recommended from PVCC to PGND. For effective filtering it is strongly recommended to have a direct connection from this capacitor to PGND (pin 5).

The boost supply for driving the High-Side MOSFET is generated by connecting a small capacitor between BOOT pin and the switching node PHASE. It is recommended that this capacitor C_{BOOT} should be connected as close as possible to the device across pins 32 and 33. Bootstrap diode is integrated into the package. R_{BOOT} is an optional resistor used by designers to slow down the turn-on speed of the high-side MOSFET. The value is a compromise between the need to keep both the switching time and VSWH node spikes as low as possible and are typically 1Ω to 5Ω.C

Under-voltage Lockout

During initial start-up, both the VCC and PVCC voltage rise is monitored. The PWM signals are passed through to the gate drivers, the TMON output is valid and the IMON output starts at zero, and becomes valid on the first GL signal. If either VCC or PVCC drops below the falling threshold of 3.8V (typical), operation of the driver is disabled.

VCC is monitored for UVLO conditions and both outputs are actively held low unless adequate gate supply is available. The under-voltage lockout is set at 4.1V with a 300mV hysteresis. Since the PWM control signals are provided typically from an external controller or a digital processor extra care must be taken during start up.

The AOZ5473QE must be powered up before the PWM input is applied. It should be ensured that PWM signal goes through a proper soft start sequence to minimize inrush current in the converter during start up. Powering the module with a full duty cycle PWM signal already applied may lead to a number of undesirable consequences as explained below.

Tri-State PWM Input

The AOZ5473QE supports a 3.3V PWM tri-level input and is compatible with AOS' digital multiphase controllers as well as other control IC's utilizing 3.3V PWM logic. Should the pin be pulled into and remain in the tri-state window for a set hold-off time, the driver will force both MOSFETs to their off states. When the PWM signal moves outside the shutdown window, the driver immediately resumes driving the MOSFETs according to the PWM commands.

This feature is utilized by AOS' PWM controllers as a method of forcing both MOSFETs off. Should the PWM input be left floating, the pin will be pulled into the tri-state window internally and thus force both MOSFETs to a safe off state. Although the PWM input can sustain a voltage as high as VCC, the AOZ5473QE is not compatible with a controller that drives its mid-level in tri-state higher than 1.7V.

Bootstrap Capacitor Refresh

If the AOZ5473QE remains in a tri-state condition for an extended period of time, the bootstrap capacitor voltage may discharge. AOZ5473QE monitors the bootstrap voltage and automatically replenishes the bootstrap capacitor from VIN, through a PMOS switch.

Shoot-Through Protection

The AOZ5473QE utilizes fixed 16ns dead time that optimizes the dead time for high efficiency and guarantees that simultaneous conduction of both FETs cannot occur.

Temperature Monitoring and Fault Reporting (TMON/FLT)

TMON/FLT is a dual function pin that reports internal junction temperature during normal operation and will be pulled high (~ 3.3V) in the event of a fault.

TMON/FLT has a offset voltage of 800mV at 25°C and junction temperature further scales at the gain of 8mV/°C as defined in equation (1). The TMON/FLT pin is configured internally such that TMON from multiple SPS can connected together externally. TMON pin is designed to have much higher sourcing capability but weak sinking ability so SPS with higher junction temperature takes the preceding.

$$T_J(°C) = [(TMON(V) – 0.8) / 0.008] + 25 \quad (1)$$

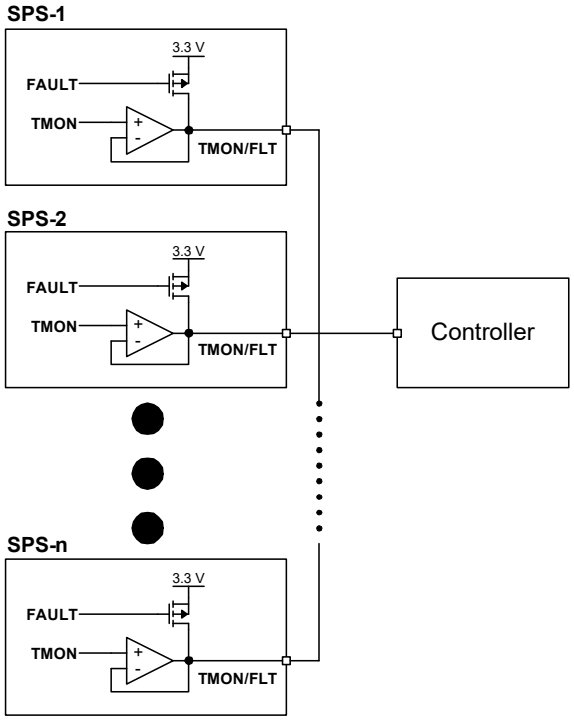


Figure 15. TMON/FLT from multiple SPS

SPS can be connected together. Sourcing capability at TMON pin is much higher than sinking capability so SPS with higher junction temperature takes preceding.

AOZ5473QE pulls TMON/FLT pin high (~ 3.3V) if it detects Over-Current (OC), Over-Temperature (OT), HS-FET short, and LS-FET short faults. Other than OT fault, AOZ5473QE continue to respond to PWM signal command. Table 1 summarizes how AOZ5473QE responses to each fault.

Table 1. Fault Reporting Summary

FAULT EVENT	Response
OC	• Fault is flagged after 10 successive count • Continues to respond to PWM • The FAULT flag is clear when OC event is removed
OT	• Fault is flagged • Thermal Shutdown at TJ ≥ 150 °C • Fault is cleared at TJ ≤ 130 °C
HS-FET Short	• Fault is flagged • Continues to respond to PWM • E-Fuse trips when GL is high if E-fuse is used in the system
LS-FET Short	• Fault is flagged • Continues to respond to PWM • E-Fuse trips when GH is high if E-fuse is used in the system

Current Monitoring

The AOZ5473QE precisely senses the current delivered through the low-side MOSFET. The signal is reported through the IMON pin scaled with a 5 mV/A gain and is referenced to an externally supplied voltage (applied to REFIN). It is expected the controller to supply the REFIN reference and to sense the current signal (IMON) differentially between IMON and REFIN pins. The current information delivered to the controller (IMON) is internally compensated for the temperature drifts thus removing the necessity for temperature compensation into the controller itself. The current is sensed during low-side conduction time and estimated during high-side conduction time to reconstruct entire inductor current waveform. A resistor connected to LSET pin programs the inductor value used in the application to construct the current waveform during high-side MOSFET conduction. RLSET can be selected as defined in Equation (2).

$$R_{LSET} = L/(10x10^{-12})\ \Omega \quad (2)$$

Table 2. LSET Values for Widely Used Inductances

Inductance (nH)	LSET (kΩ)
100	10
120	12
180	18
220	22
300	30

Input Voltage VIN

AOZ5473QE operates over a wide input range of 4.5V to 20V. As with any other synchronous buck converter, large pulse currents at high frequency and extremely high di/dt rates will be drawn by the module during normal operation. It is strongly recommended to place a bypass capacitor for input voltage very close to package lead with X7R or X5R quality ceramic capacitors.

The high-side MOSFET in AOZ5473QE is optimized for fast switching with low duty cycle. It has ultra-low gate charge which has been achieved as a trade-off with a higher on-resistance value. When the module is operated at low VIN the duty ratio will be higher and conduction losses in the high-side MOSFET will also be correspondingly higher. This will be compensated to some extent by reduced switching losses. The total power loss in the module may appear to be low even though in reality the high-side MOSFET losses may be disproportionately high. Since the two MOSFETs have their own exposed pads and PCB copper areas for heat dissipation, the high-side MOSFET may be much hotter than the low-side MOSFET. It is recommended that worst case junction temperature be measured and ensured to be within safe limits when the module is operated with high duty ratios.

PWM Input

AOZ5473QE is offered with PWM input compatible with 3.3V logic. The PWM is also a tri-state compatible input. When the input is high impedance or left open, both the gate drive outputs will be off and the gates are held actively low. As shown in Figure 2, there is a hold off delay between the time PWM signal enters the tri-state window and the corresponding gate drive is pulled low. This delay is typically 30ns and intended to prevent spurious triggering of the tri-state mode which may be caused either by noise induced glitches in the PWM waveform or slow rise and fall times.

Gate Driver

AOZ5473QE has an on-board high current high-speed driver for the high-side MOSFET and a complementary driver for the low-side MOSFET. Propagation delays between transitions of the PWM waveform and corresponding gate drives are kept to the minimum. An internal shoot through protection scheme ensures that neither MOSFET would turn on while the other one is still conducting current, thereby preventing shoot through condition of the input current. When the PWM signal makes a transition from High to Low or Low to High, the corresponding gate drive GH or GL begins to turn off. There is a fixed dead time that insures no shoot through and that the efficiency remains high. The complementary gate driver is then turned on. The dead times on both the rising and falling edges between the two switches are minimized, at the same time preventing cross conduction across the input bus, even under transient and abnormal conditions of operation. The GL is brought out on pin 6. However this connection is not made directly to the MOSFET gate pad and its voltage measurement may not reflect the actual gate voltage applied inside the package. The gate connections are primarily for functional tests during manufacturing and no connections should be made to them in the application.

Layout Guideline

Good PCB layout practice helps lower PCB losses and in the same time achieve stable. Please follow these guidelines to achieve optimal performance.

- Connect VIN, VOUT and PGND to a large copper area and use vias to cool the chip to improve thermal performance and long-term reliability. Place ceramic capacitors between VIN and PGND closer to the device to minimize high frequency noise as shown in Figure 16.
- Effect of noise generated at VSW node can be minimized by reducing area of copper used to make VSW node connection.
- Power traces and load connections should be kept short to minimize PCB parasitic resistance and stray inductance.
- PVCC can be noisy. 1 Ω resistor is recommended to be placed between PVCC and VCC and decouple both PVCC and VCC with ceramics 1 µF capacitor.

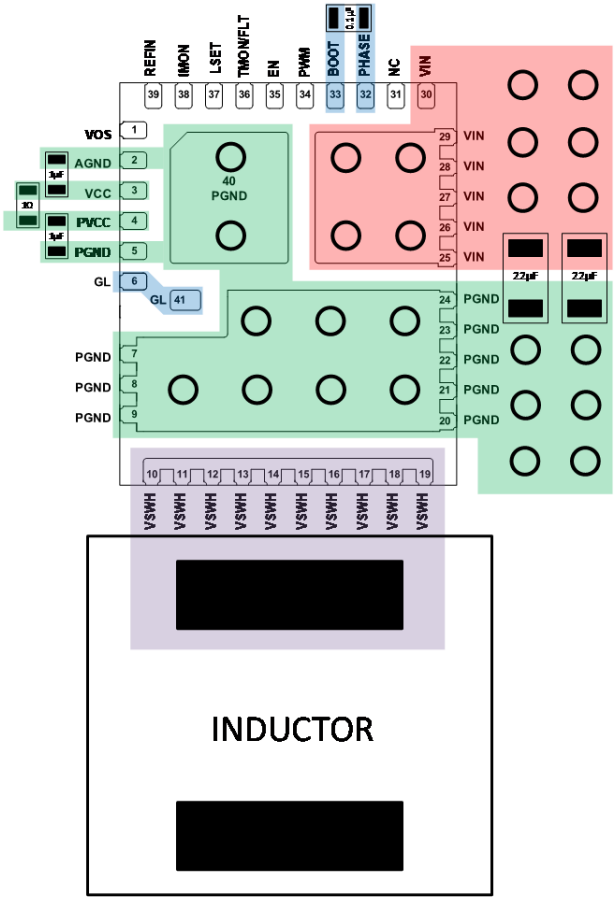
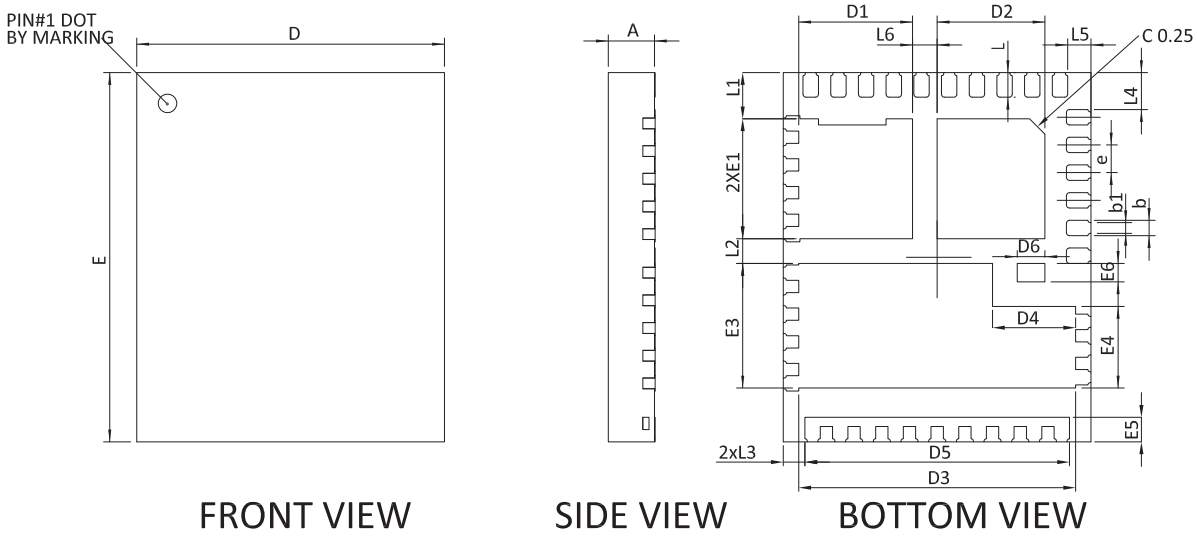
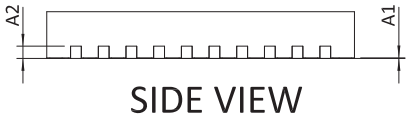


Figure 16. Recommended Layout

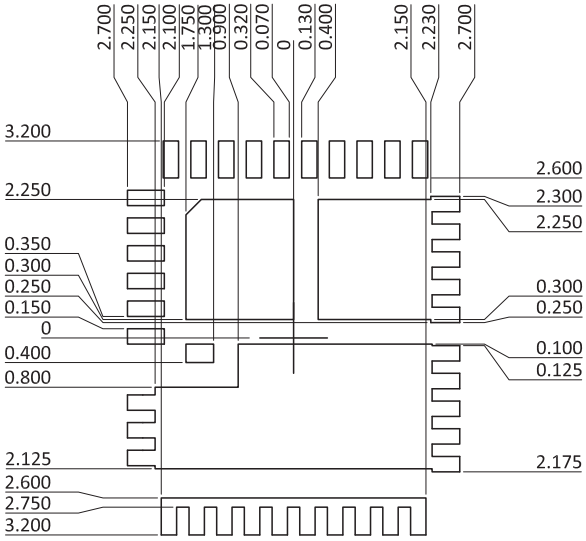
Package Dimensions, QFN5x6-39L, EP3_S



FRONT VIEW SIDE VIEW BOTTOM VIEW



SIDE VIEW



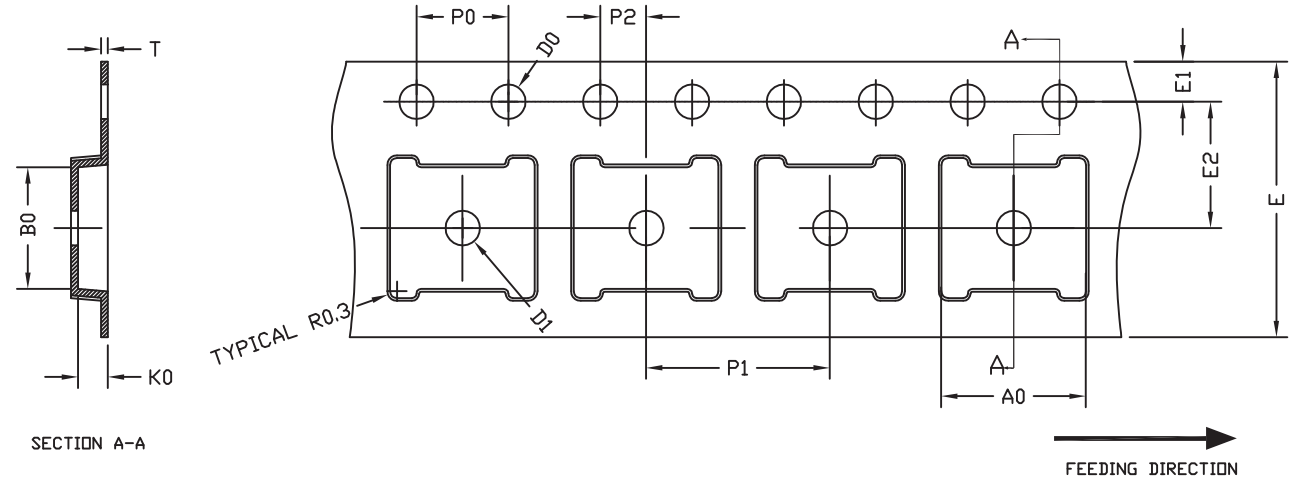
SYMBOLS	DIMENSION IN MM.			DIMENSION IN INCH.		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2	0.20REF			0.008REF		
D	4.90	5.00	5.10	0.193	0.197	0.201
D1	1.75	1.85	1.95	0.069	0.073	0.077
D2	1.65	1.75	1.85	0.065	0.069	0.073
D3	4.40	4.50	4.60	0.173	0.177	0.181
D4	1.25	1.35	1.45	0.049	0.053	0.057
D5	4.20	4.30	4.40	0.165	0.169	0.173
D6	0.35	0.45	0.55	0.014	0.018	0.022
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	1.85	1.95	2.05	0.073	0.077	0.081
E3	1.925	2.025	2.125	0.076	0.080	0.084
E4	1.225	1.325	1.425	0.048	0.052	0.056
E5	0.3	0.4	0.5	0.012	0.016	0.020
E6	0.2	0.3	0.4	0.008	0.012	0.016
L	0.3	0.4	0.5	0.012	0.016	0.020
L1	0.65	0.75	0.85	0.026	0.030	0.033
L2	0.3	0.4	0.5	0.012	0.016	0.020
L3	0.25	0.35	0.45	0.010	0.014	0.018
L4	0.5	0.6	0.7	0.020	0.024	0.028
L5	0.28	0.38	0.48	0.011	0.015	0.019
L6	0.3	0.4	0.5	0.012	0.016	0.020
b	0.15	0.25	0.35	0.006	0.010	0.014
b1	0.075	0.175	0.275	0.003	0.007	0.011
e	0.45BSC			0.018BSC		

RECOMMANDED LAND PATTERN

NOTE

1.CONTROLLING DIMENSION IS MILLIMETER.
2.CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

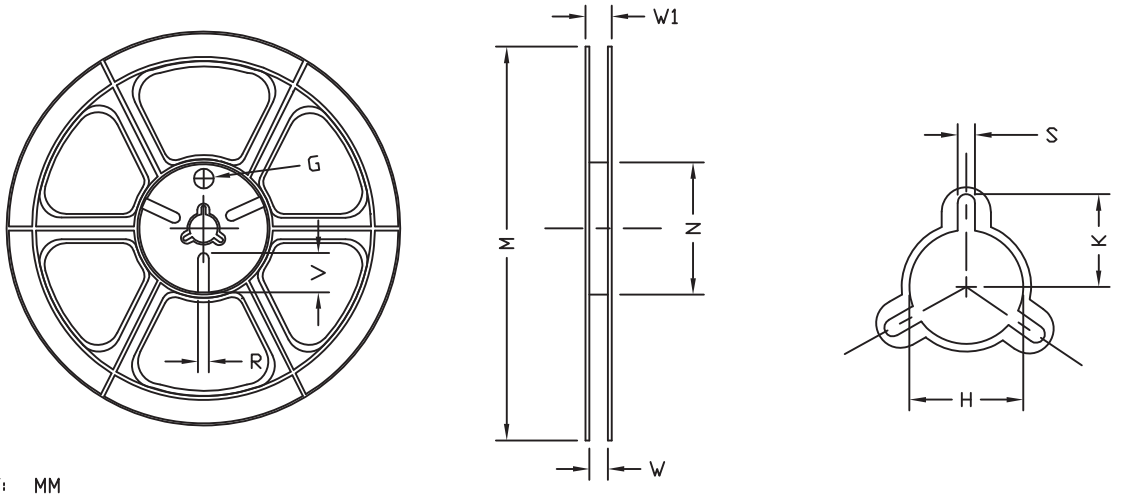
Tape and Reel Dimensions, QFN5x6-39L, EP3_S



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN5X6	6.30 ±0.1	5.30 ±0.1	0.9 ±0.1	1.55 ±0.05	ø1.50 MIN	12.00 ±0.3	1.75 ±0.1	5.50 ±0.05	4.00 ±0.1	8.00 ±0.1	2.00 ±0.05	0.3 ±0.05

Reel



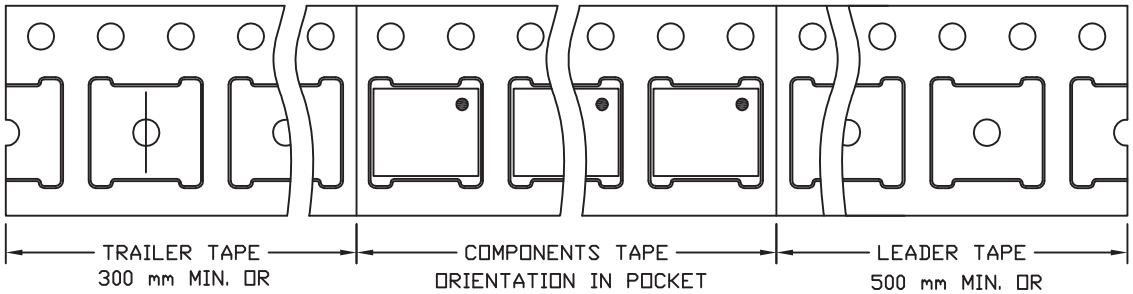
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50 −0.20	10.60	2.00 ±0.50	---	---	---

Tape

Leader / Trailer & Orientation

Unit Per Reel: 3000pcs



Part Marking

AOZ5473
(5mm x 6mm QFN)