

General Description

AOZ7523 is a series of current mode controllers with a 650V integrated power MOSFET, and a X-capacitor discharge function (Bleeding Resistor Removal, BRR), Brown-In/Brown-Out (Lossless Brown-Out, LBO) plus a high voltage start-up circuitry. The series also provides frequency foldback and skip mode during light load conditions to achieve excellent light load efficiency and low power standby mode. As well as a digital Spread Spectrum Clock Generator (SSCG) to improve EMI emissions. In addition, AOZ7523 includes cycle-by-cycle current limit, Under Voltage Lockout (UVLO), VDD OVP, DMAG pin OVP, Over Load Protection (OLP), CS pin protection, Secondary-Side Diode Short protection (SSDS).

Applications

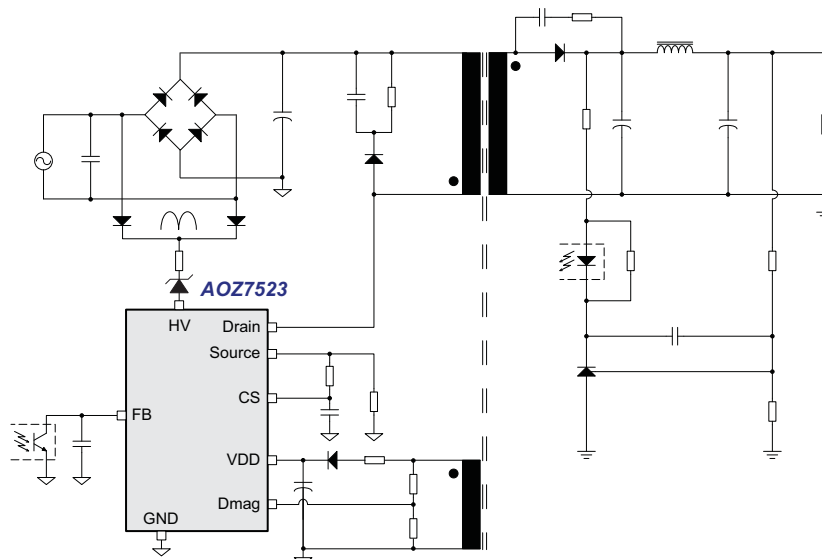
- SMPS
- NB Adapter
- Charger

Features

- Integrated with 650V HV MOSFET
- Integrated bleeding resistor removal function
- Integrated brown-in/brown-out function
- Integrated HV start-up circuitry
- Under-voltage lockout: 7V/15V
- Low operation current
- Lower operation current in skip mode (<450 μ A)
- Built-in 65kHz/130kHz operation frequency
- Current mode control
- Soft-start
- Leading edge blanking function on current sense
- Built-in slope compensation
- Cycle-by-cycle current limit
- Minimum on time modulation to minimize acoustic noise
- Frequency foldback mode and skip mode operation
- Frequency spread by spread spectrum clock generator (SSCG)
- VDD over-voltage protection
- Dmag pin over-voltage protection
- Secondary-side diode short protection
- CS pin protection
- Internal over-temperature protection



Typical Application



Ordering Information

| Part Number | Ambient Temperature Range | Package | Environmental |
|-------------|---------------------------|---------|---------------|
| AOZ7523XAI | -40°C to +125°C | SO-13 | Green Product |



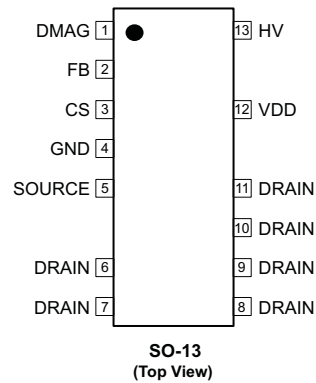
AOS Green Products use reduced levels of Halogens, and are also RoHS compliant. Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.



| Part Number | AOZ7523GAI | AOZ7523LAI | AOZ7523AAI | AOZ7523RAI | AOZ7523HAI |
|---------------------|---------------|---------------|---------------|---------------|---------------|
| Switching Frequency | 65kHz | 65kHz | 65kHz | 65kHz | 130kHz |
| OLP / SSDS | Auto Recovery | Auto Recovery | Latch | Auto Recovery | Auto Recovery |
| VDD OVP | Auto Recovery | Latch | Latch | Auto Recovery | Auto Recovery |
| DMAG OVP | Latch | Latch | Latch | Auto Recovery | Latch |
| DMAG Low | Auto Recovery | Latch | Latch | Latch | Auto Recovery |
| Internal OTP | Auto Recovery | Auto Recovery | Auto Recovery | Auto Recovery | Auto Recovery |

Table 1. Protection Version

Pin Configuration



Pin Description

| Pin Number | Pin Name | Pin Function |
|------------|----------|--|
| 1 | DMAG | Demagnetize pin for voltage sense. |
| 2 | FB | Feedback pin for voltage loop. |
| 3 | CS | Current sense pin for current loop. |
| 4 | GND | Ground. |
| 5 | SOURCE | Source pin of MOSFET. |
| 6~11 | DRAIN | Drain pin of MOSFET. |
| 12 | VDD | Power supply pin for controller. |
| 13 | HV | High voltage start-up current supply and input AC voltage detection. |

Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

| Parameter | Rating |
|---|-----------------|
| V _{HV} | 0V to 500V |
| V _{DRAIN} | 0V to 650V |
| V _{VDD} | 0.3V to 30V |
| V _{DMEG} , V _{FB} , V _{CS} | -0.3V to 6V |
| GND | -0.3V to +0.3V |
| Package Power Dissipation | 1.4W |
| Junction Temperature (T _J) | +150°C |
| Storage Temperature (T _S) | -65°C to +150°C |
| ESD HBM ⁽¹⁾ (Except HV Pin) | 4kV |
| ESD CDM ⁽¹⁾ (Except HV Pin) | 1kV |

Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Electrical Characteristics

T_A = -25°C to 85°C, V_{DD} = 15V, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------|--|---|-----|-----|-----|-------|
| HV MOSFET | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | I _D = 250μA, V _{GS} = 0V, T _J = 25°C | 650 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} = 650V, V _{GS} = 0V, | | | 1 | μA |
| R _{DS(ON)} | Static Drain-Source On-Resistance | | | | 1.8 | Ω |
| I _D | Continuous Drain Current | T _C = 25°C | | | 3.5 | A |
| I _{DM} | Pulse Drain Current | | | | 16 | A |
| HV | | | | | | |
| I _{HV} | Supply Current from HV Pin | V _{HV} = 100V, V _{DD} = 0V, Controller Off | | 1.5 | | mA |
| I _{HV-LC} | Leakage Current from HV Pin | V _{HV} = 500V, V _{DD} = 15V, Controller On | | 0.8 | | μA |
| V _{BNI} | Brown-In Voltage | With 51V Zener in HV Pin | | 80 | | Vac |
| V _{BNO} | Brown-Out Voltage | With 51V Zener in HV Pin | | 70 | | Vac |
| T _{SENSE} | V _{IN} Sensing Period | | | 300 | | ms |
| D _{SENSE} | V _{IN} Sensing Duty | | | 10 | | % |
| T _{BNO} | Brown-Out De-Bounce Time | | | 300 | 600 | ms |
| T _{DIS-Xcap} | X-Cap Discharge De-Bounce Time | | 30 | | 450 | ms |
| VDD | | | | | | |
| V _{DD-OVP} | VDD Over-Voltage Protection | | 26 | 27 | 28 | V |
| | VDD Over-Voltage Protection De-Bounce Time | | | 20 | | μs |
| V _{DD-ON} | Turn-On Threshold Voltage | | 14 | 15 | 16 | V |
| V _{DD-UVLO} | Turn-Off and Under-Voltage Lock-Out | | 6.5 | 7 | 7.5 | V |
| V _{DDM-E} | VDD Hold-Up Mode Entry Level | | | 7.5 | | V |

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

| Parameter | Rating |
|---|-----------------|
| Supply Voltage (V _{DD}) | 7.5V to 25V |
| Ambient Temperature (T _A) | -40°C to +105°C |
| Package Thermal Resistance SO-13 (θ _{JA}) | 65°C/W |

Electrical Characteristics (Continued)
 $T_A = -25^{\circ}\text{C}$ to 85°C , $V_{DD} = 15\text{V}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-------------------|--|---|------|---------|------|---------------|
| V_{DDM-D} | VDD Hold-Up Mode Depart Level | | | 8 | | V |
| $V_{DDM-BNH}$ | VDD Hold-Up HI Level in Brown-Out | | | 14 | | V |
| $V_{DDM-BNL}$ | VDD Hold-Up LO Level in Brown-Out | | | 12 | | V |
| V_{DD-L} | VDD in Latch Mode | Option for Latch Mode | | 9 | | V |
| I_{ST} | Start-Up Current | | | 150 | 200 | μA |
| I_{DD-OP} | Operation Current | $V_{DD} = 15\text{V}$, Controller On, $C_L = 1\text{nF}$ | | 3.5 | 4 | mA |
| $I_{DD-SKIP}$ | Skip Mode Operation Current | $V_{DD} = 9\text{V}$, $\text{FB} < 1\text{V}$ | | 350 | 450 | μA |
| FREQUENCY | | | | | | |
| F_{OSC} | General Continuous Operation Frequency | | 61 | 65 | 69 | kHz |
| | | For AOZ7523H | 122 | 130 | 138 | kHz |
| F_{MIN} | Minimum Continuous Operation Frequency | | | 20 | | kHz |
| F_{SSCG} | Spread Spectrum Clock Generator | | | ± 6 | | % |
| D_{MAX} | Minimum Duty Cycle | | | 75 | | % |
| FB | | | | | | |
| Z_{FB} | FB Pin Impedance | | 36 | 40 | 44 | k Ω |
| $V_{FB-OPEN}$ | FB Pin Pull-Up Voltage | FB Pin Open | | 4.4 | | V |
| G_{FC} | Gain-to-CS | | | 0.5 | | V/V |
| V_{FB-E} | Entry FR Threshold Voltage | | | 2.1 | | V |
| V_{FB-D} | Depart FR Threshold Voltage | | | 1.8 | | V |
| V_{SK-E} | Skip Mode Entry Level | | | 0.7 | | V |
| V_{SK-D} | Skip Mode Depart Level | | | 0.82 | | V |
| DMAG | | | | | | |
| V_{CLAMP} | Minimum Clamp Voltage | | 0.7 | 1 | 1.3 | V |
| T_{MIN} | Minimum On Time | Sourcing = $180\mu\text{A}^{(2)}$ | | 3 | | μs |
| | | Sourcing = $750\mu\text{A}^{(2)}$ | | 0.8 | | μs |
| $T_{MIN-MAX}$ | Maximum T_{MIN} Clamp | Sourcing = $100\mu\text{A}^{(2)}$ | | 3.2 | | μs |
| $T_{MIN-MIN}$ | Minimum T_{MIN} Clamp | Sourcing = $900\mu\text{A}^{(2)}$ | | 0.7 | | μs |
| $I_{DMAG-MAX}$ | Maximum Sourcing Current | | 1 | | | mA |
| V_{D-OVP} | DMAG Over-Voltage Protection | | 2.95 | 3 | 3.05 | V |
| T_{D-OVP} | V_{D-OVP} De-Bounce Time | 5 Clock Cycles, $F_s = 130\text{kHz}$ | | 30 | 40 | μs |
| | | 5 Clock Cycles, $F_s = 65\text{kHz}$ | | 60 | 100 | μs |
| V_{DIS} | Disable Protection | | 0.25 | 0.3 | 0.35 | V |
| T_{DIS} | Disable De-Bounce Time | 2 Clock Cycles, $F_s = 130\text{kHz}$ | | 15 | 20 | μs |
| | | 2 Clock Cycles, $F_s = 65\text{kHz}$ | | 30 | 40 | μs |
| SOFT-START | | | | | | |
| T_{SS} | Soft-Start Time | $F_s = 65\text{kHz}$ | | 4 | | ms |
| $F_{SS-SKIP}$ | Soft-Start Skip Frequency | $V_{CS} > 1\text{V}$, $F_s = 130\text{kHz}$ | | 65 | | kHz |
| | | $V_{CS} > 1\text{V}$, $F_s = 65\text{kHz}$ | | 32.5 | | kHz |

Electrical Characteristics (Continued)

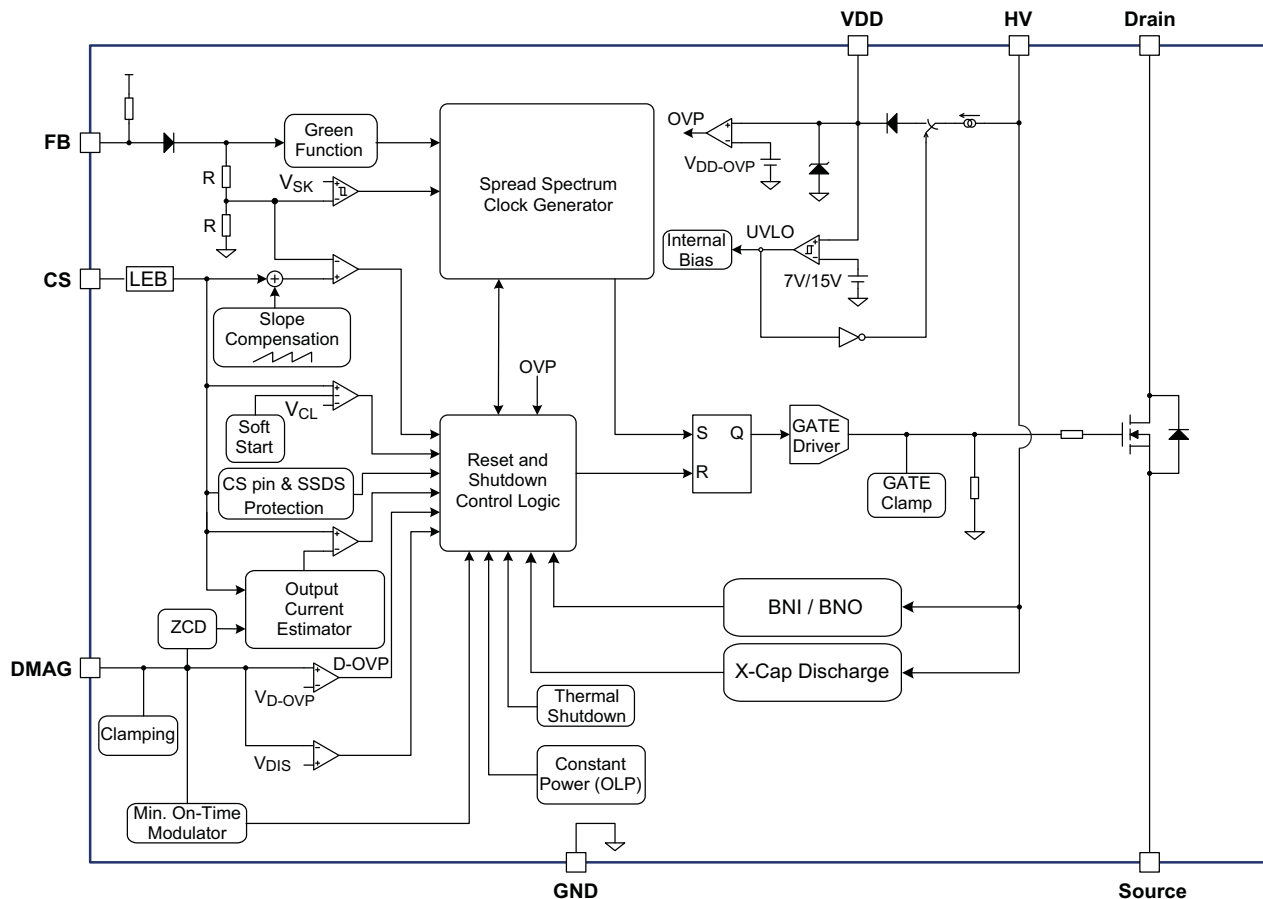
$T_A = -25^{\circ}\text{C}$ to 85°C , $V_{DD} = 15\text{V}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------------------------------|--|--|------|-----|------|--------------------|
| CURRENT SENSE | | | | | | |
| V_{CL} | General Continuous Operation Limited Current Sense Level | | 0.85 | 0.9 | 0.95 | V |
| T_{OLP} | Over Load Protection De-Bounce Time | | | 60 | 80 | ms |
| V_{CL2} | SSDS Level | | | 1.5 | | V |
| T_{CL2} | De-Bounce Time for V_{CL2} | Continuous 5 Clock Cycles, $F_s = 65\text{kHz}$ | | 75 | 100 | μs |
| T_{LEB} | Leading Edge Blanking Time | | | 250 | 400 | ns |
| T_P | Propagation Delay Time | | | 50 | 100 | ns |
| OVER TEMPERATURE PROTECTION | | | | | | |
| OTP | Internal Over Temperature Protection | T_J Rising | | 145 | | $^{\circ}\text{C}$ |
| OTP _{REC} | Thermal Shutdown Recovery Threshold | T_J Falling | | 125 | | $^{\circ}\text{C}$ |

Note:

- Guaranteed by design.

Functional Block Diagram



Typical Characteristics

Figure 1. Supply Current From HV Pin vs. Temperature

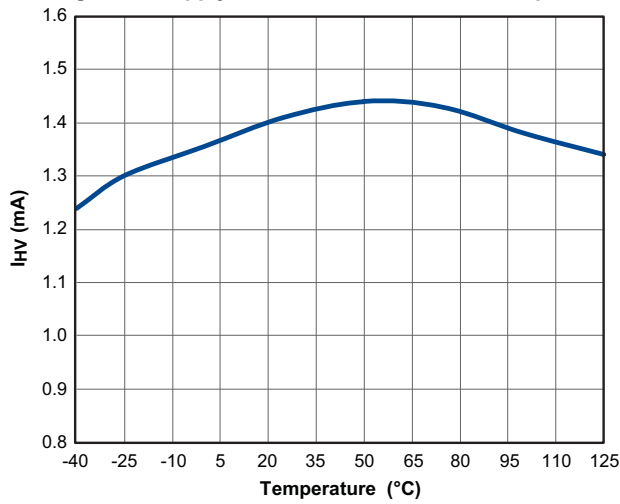


Figure 2. Turn-On Threshold Voltage vs. Temperature

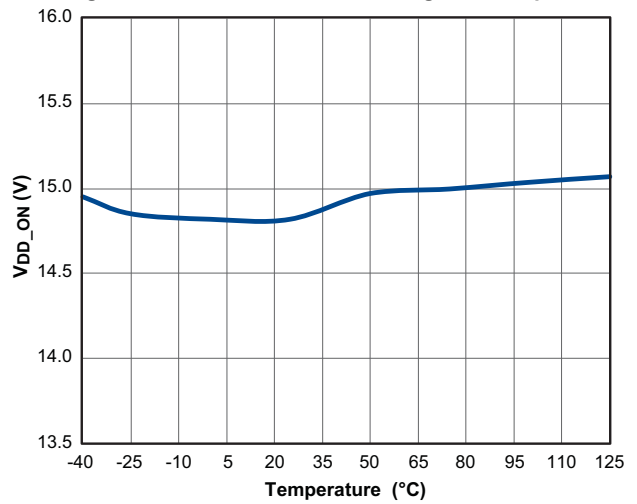


Figure 3. Operating Current vs. Temperature

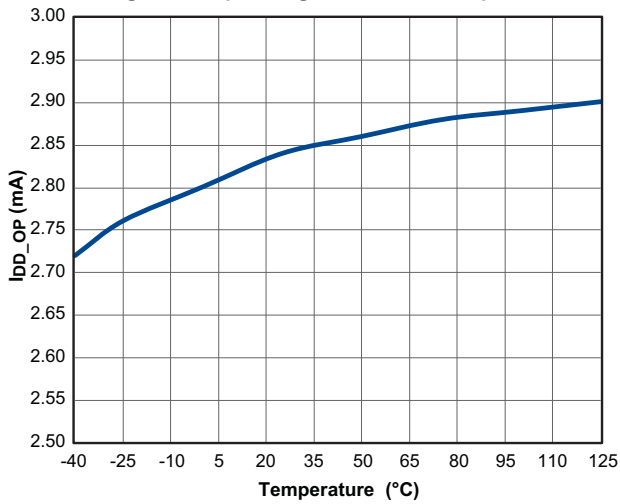


Figure 4. Under-Voltage Lockout Voltage vs. Temperature

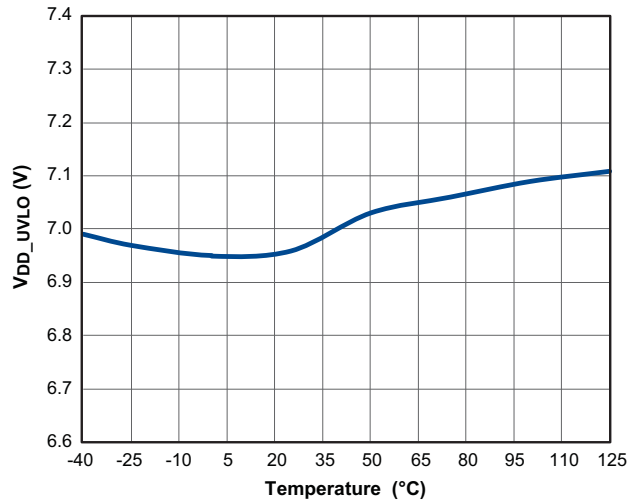


Figure 5. VDD OVP Level vs. Temperature

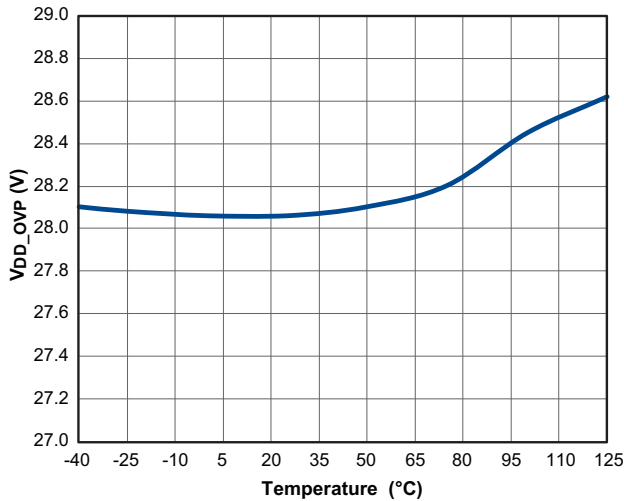
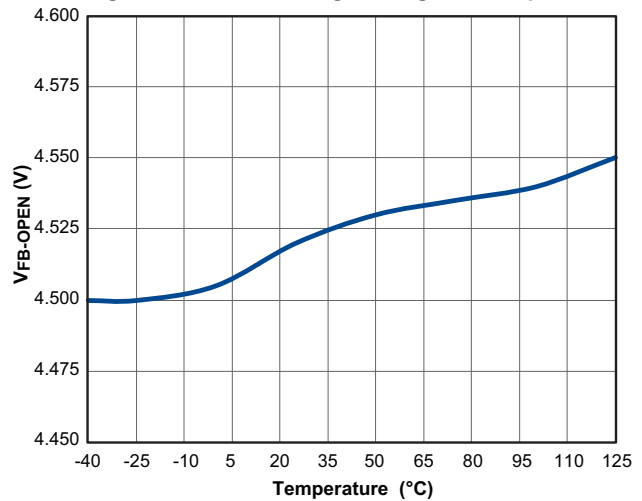


Figure 6. FB Pin Pull High Voltage vs. Temperature



Typical Characteristics (Continued)

Figure 7. FB Pin Impedance vs. Temperature

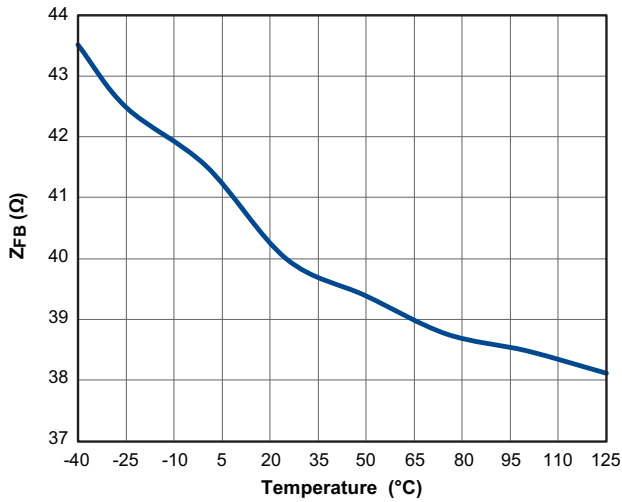


Figure 8. Entry FR Threshold Voltage vs. Temperature

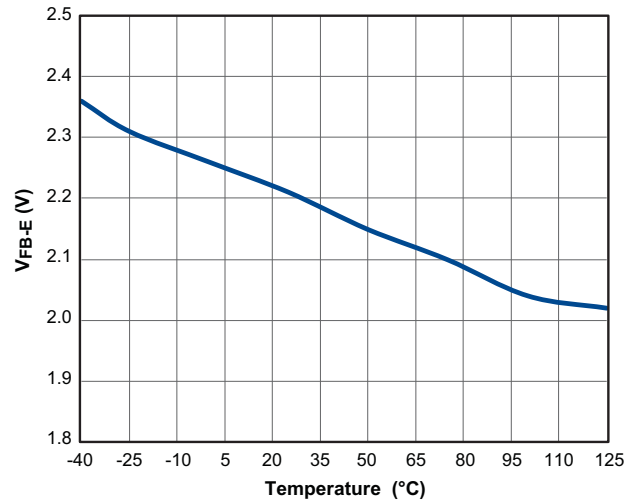


Figure 9. Depart FR Threshold Voltage vs. Temperature

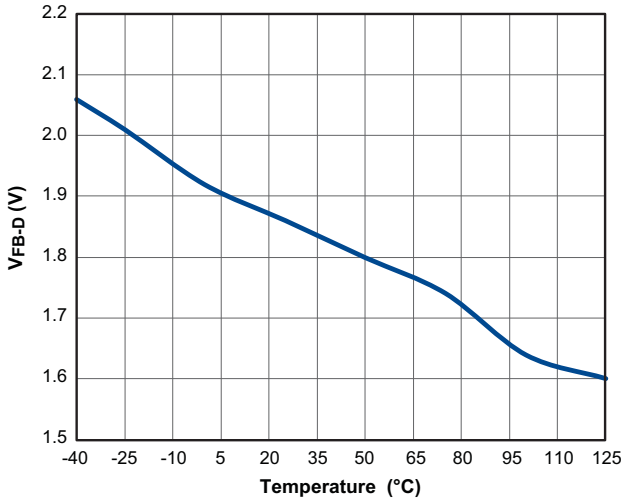


Figure 10. Skip Mode Entry Level vs. Temperature

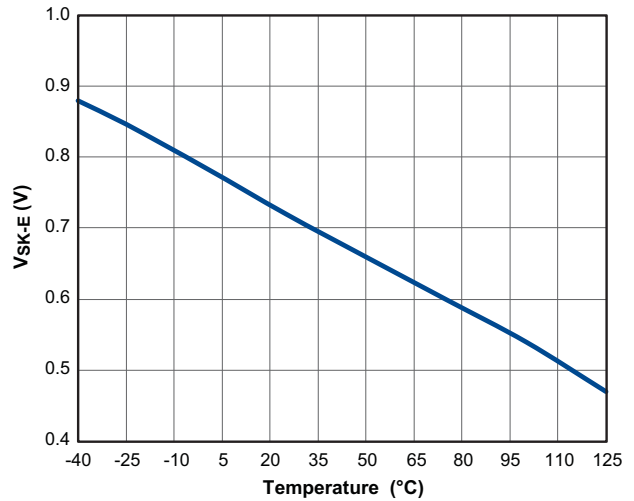


Figure 11. Skip Mode Depart Level vs. Temperature

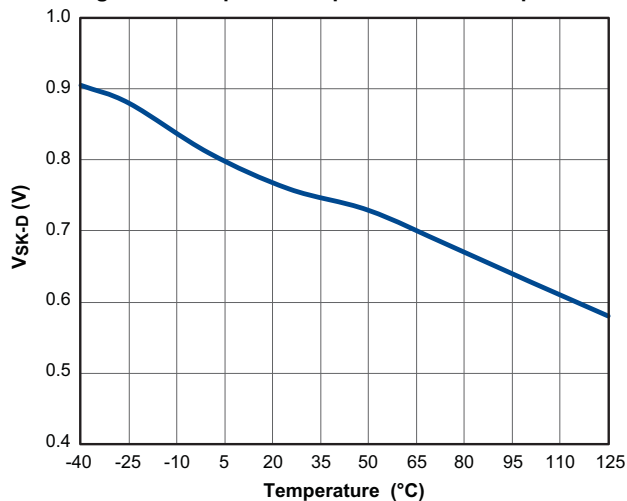
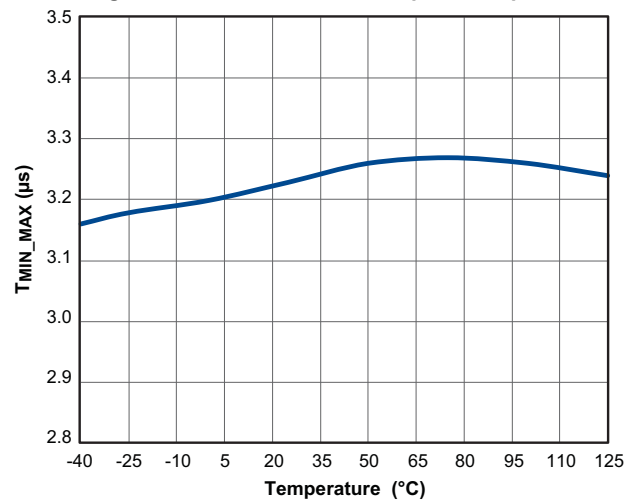


Figure 12. Maximum TMIN Clamp vs. Temperature



Typical Characteristics (Continued)

Figure 13. Minimum T_{MIN} CLAMP vs. Temperature

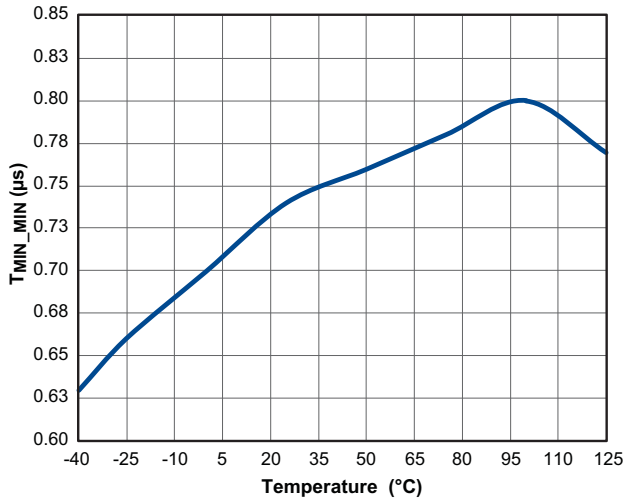


Figure 14. General Continuous Operation Frequency vs. Temperature

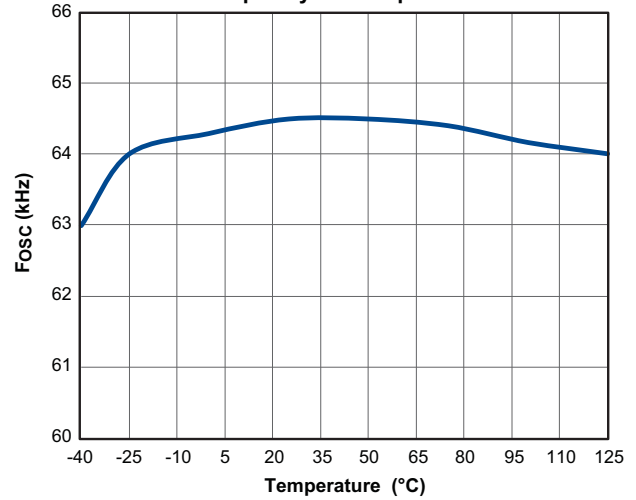


Figure 15. Minimum Continuous Operation Frequenc vs. Temperature

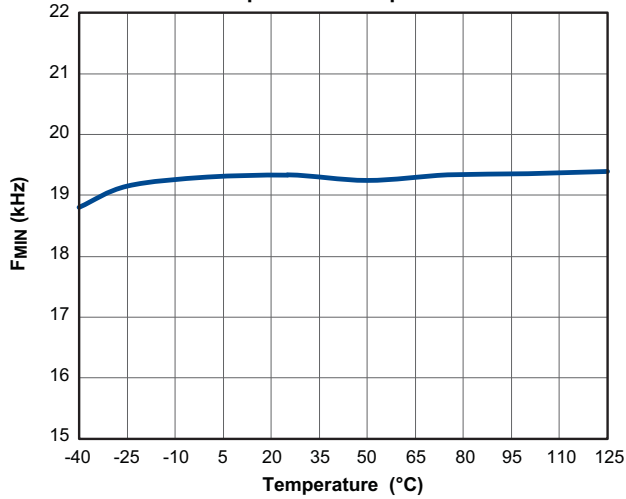


Figure 16. Maximum Duty Cycle vs. Temperature

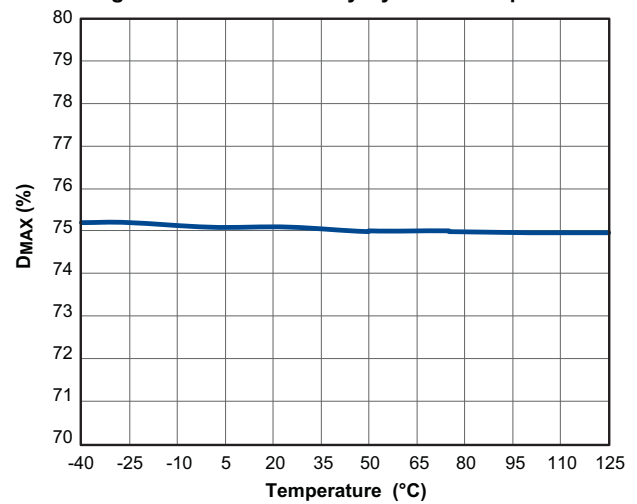


Figure 17. Current Limit vs. Temperature

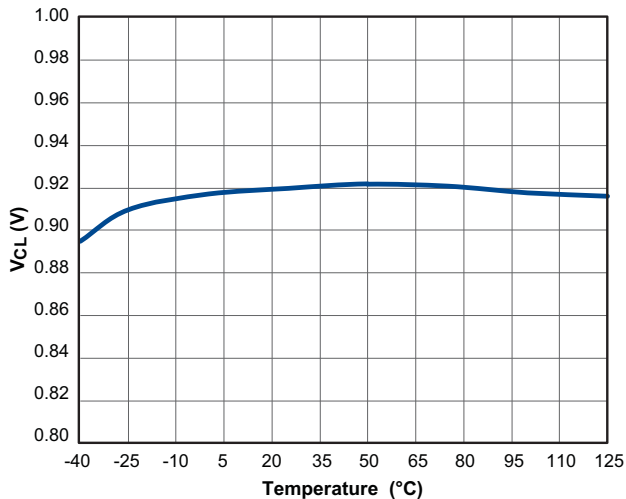
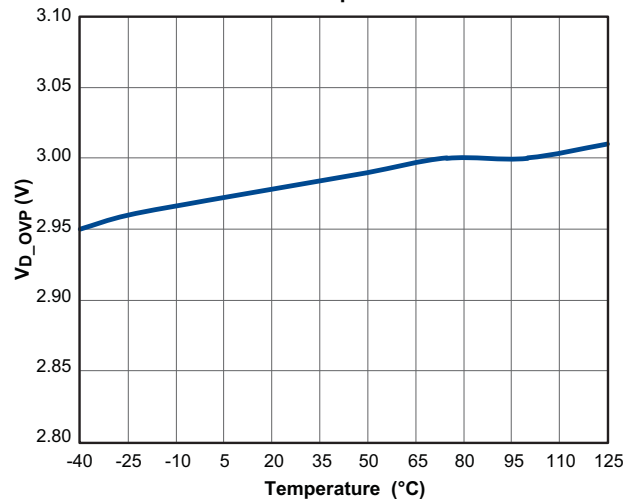


Figure 18. DMAG Pin Over Voltage Level vs. Temperature



Typical Characteristics (Continued)

Figure 19. DMAG Sourcing Current 0.5mA vs. Temperature

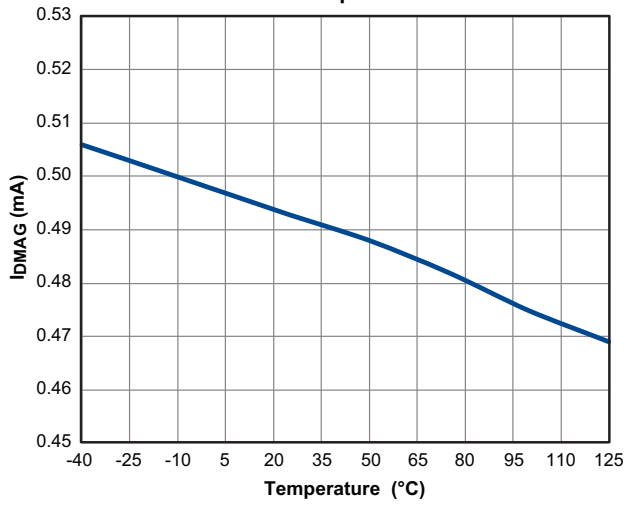
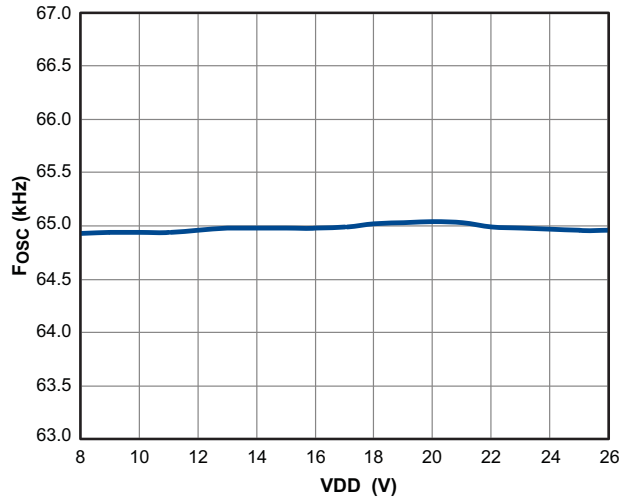


Figure 20. General Continuous Operation Frequency vs. VDD



Typical Operation Description

Start-Up

During the start-up period, the HV device acts as a current source and charges the VDD capacitor until its voltage is higher than that of the turn-on threshold V_{DD-ON} , at that point the AOZ7523 will start to operate but it will enter standby mode to wait brown-in signal. The VDD voltage of AOZ7523 will be kept between 12V~14V until brown-in is triggered. After brown-in, PWM signal will start to drive the MOSFET and the peak current of MOSFET will be increased linearly during the soft-start period.

Normal Mode Operation

In normal mode operation, if the output is in heavy load, the controller is switching with maximum frequency (130kHz or 65kHz) and operated with current-mode control.

Frequency Foldback Mode Operation

AOZ7523 provides green mode operation to reduce switching loss and improve system efficiency by frequency foldback function during light load condition. When the voltage of FB pin is decreased below V_{FB-E} . The controller will enter green mode and the switching frequency starts foldback according to load condition. The minimum switching frequency will be clamped to F_{MIN} when the voltage of FB pin is below V_{FB-D} .

Skipping Mode Operation

Under very light load condition, the voltage of FB will be decreased to a very low level. When the voltage of FB is dropped below the threshold (V_{SK-E}) that is the hysteresis voltage of internal PWM comparator, the PWM signal will be blanked and stop to drive MOSFET. After the output voltage dropped and FB voltage increased higher than V_{SK-D} , the PWM signal will be resumed.

VDD Hold-Up Mode Operation

During load transient or ultra light load conditions, FB voltage will drop deeply and enter into skipping cycle mode to stop PWM signal. In some conditions, VDD voltage will drop below controller's turn-off threshold (UVLO) and then the system will be restarted. If another load occurred, the system cannot respond immediately and the output voltage will drop deeply. This mode is very useful to prevent system restarting during ultra light load condition and has a quick response for load transients. It doesn't require a two-stage VDD circuit to keep VDD voltage higher than UVLO.

Minimum On Time Modulation

In order to reduce switching loss and minimize acoustic noise, AOZ7523 provides Modulate On-Time to limit the minimum turn-on time ($T_{on,min}$). The modulate on-time is inversely proportional to input voltage. In the condition of low line input voltage, PWM on-time will be enlarged to reduce switching cycles and increase the efficiency of light load. In the condition of high line input voltage, PWM on time will be tighten to minimize acoustic noise and make the ripple of output voltage close in every line input.

Protection Features

Over Voltage Protection (OVP)

It's critical that over voltage protection (OVP) prevents the output voltage from exceeding the ratings of converter's components. The Over-Voltage Protection (OVP) is embedded by the information at the VDD pin. That information comes from the output voltage through the turn-ratio from auxiliary winding to secondary-side winding. When the voltage further rises and exceeds the comparator's reference voltage of static OVP (27V typ), the OVP comparator will shut down the output PWM pulse. The OVP logic also includes 20 μ s de-glitch time for false triggering by noise.

DMAG Over Voltage Protection (DOVP)

AOZ7523 provides a more accurate OVP function from DMAG pin that is to protect system component when the output is over voltage. DMAG pin detect the voltage across the auxiliary winding during MOSFET turn-off period with another 1 μ s de-glitch time. The DMAG pin voltage is proportional to the output voltage. The DMAG OVP will be triggered when the DMAG voltage over 3V continuously with 5 PWM cycles. This DMAG OVP is more accurate and faster than the VDD OVP function. A bypass capacitance (15~100pF) in DMAG pin is needed to avoid false trigger DOVP and malfunction.

DMAG pin Pull Low Protection

AOZ7523 provides a useful protection function in DMAG pin, when DMAG pin is pulled low below 0.3V and continuous with two switching cycles. The pull low current must be larger than 2mA. AOZ7523 will trigger DMAG pin pull low protection to protect system for user defined protection applications.

Cycle-by-Cycle Current Limit

The cycle-by-cycle current-limit protection circuit detects the inductor current and protects power MOSFET by turning off the output driver each cycle when the CS voltage becomes larger than preset voltage level. The voltage across the current detection resistor R_{CS} connected to the GND is fed to the CS pin for current limit detection.

There are two levels for current limit. The slow one, reference voltage set point is $V_{CL} = 0.9V$. AOZ7523 offers 60ms de-bounce timer for counting to enter Over Load Protection (OLP) mode and the system will be auto-recovery. The fast one, reference voltage set point is $V_{CL2} = 1.5V$. This protection function will be triggered, if the fast one comparator is continuously triggered by five times. This condition will be happened during transformer short or Secondary Side Diode Short (SSDS), and the circuit will induce large current in the primary-side.

Over Load Protection (OLP)

AOZ7523 provides Over Load Protection function to prevent the device of power supply system from operating with high stress. The OLP level was set by current sense resistor (R_{CS}). OLP will be triggered when load condition is larger than preset level and continuous with 60ms (4096 clock cycles).

CS Pin Open Protection

The CS pin features open-loop protection to pass the CS pin single fault testing. When CS pin was opened, CS pin voltage will be pulled high by internal circuit. The pull high voltage was higher than $V_{CL2} = 1.5V$, such that SSDS protection will be triggered to protect system.

CS Pin Short Protection

CS pin features short to GND protection to pass the CS pin single fault testing. When CS pin is shorted to GND, it means the CS pin voltage is zero. When CS pin voltage is lower than 80mV with modulate minimum on-time and continuous triggered with 5 cycles, the CS pin short protection will be triggered to protect the power supply system. The detection duration are different between high line input voltage and low line input voltage to protect the component in high line input and detect precisely in low line input voltage.

Thermal Shutdown

AOZ7523 provides internal thermal shutdown protection for controller thermal run away. If the temperature of controller is higher than internal set point, the controller will stop PWM until the temperature cools down, below hysteresis of thermal shutdown set point.

Application Information

Alpha and Omega Semiconductor provides an EXCEL based design tool, an application note and a demonstration board to help the design of AOZ7523 and reduce the R&D cycle time. All the tools can be download from: www.aosmd.com.

PCB Layout Guide

A good PCB layout can minimize EMI and reduce unknown noise, which is helpful during ESD or lightning surge tests. The followings are good PCB layout guideline for an AC/DC adaptor:

1. Bridge rectifier output should directly connect to C_{BULK} first, and use a neck layout to ensure the current flows into C_{BULK} to get better EMI and reduce line frequency ripple.
2. Loop (a), $C_{BULK} \rightarrow$ Transformer \rightarrow MOSFET $\rightarrow R_{CS} \rightarrow C_{BULK}$ (2), this loop is a high frequency and high current loop. The trace return to C_{BULK} should be kept as short as possible and directly connect to C_{BULK} ground.
3. Loop (b), the primary-side RCD snubber acts as a high frequency noise tank, it should be kept far away from the controller. The loop should be as short as possible.
4. Loop (c), the secondary-side snubber is a high frequency switching noise, too. The loop should be kept as short as possible.
5. The VDD decoupling capacitor C_{VDD} needs to be placed close to IC, VDD and GND pin as much as possible.
6. Loop (d), Switching current sense (CS pin) is very important for a stable operation. Normally, a RC filter is recommended to reduce the noise applied to the CS pin.
7. If there's a heat sink for the MOSFET, it should be connected to ground.
8. All ground for controller (4, 5, 6, 7, 8, 9, 10) should connect together first and then use a trace connect to C_{BULK} ground (2) by a neck layout.
9. Loop (e), auxiliary power loop still needs to be kept short. C_{VDD} should be placed close to the controller. This one also needs to use a trace to directly connect to C_{BULK} ground (2) by neck layout.
10. Primary-side ground of Y-Cap (11), it needs to use a trace to directly connect to C_{BULK} ground (2) by neck layout.

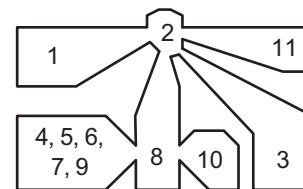


Figure 24. Ground Group of Layout Recommended

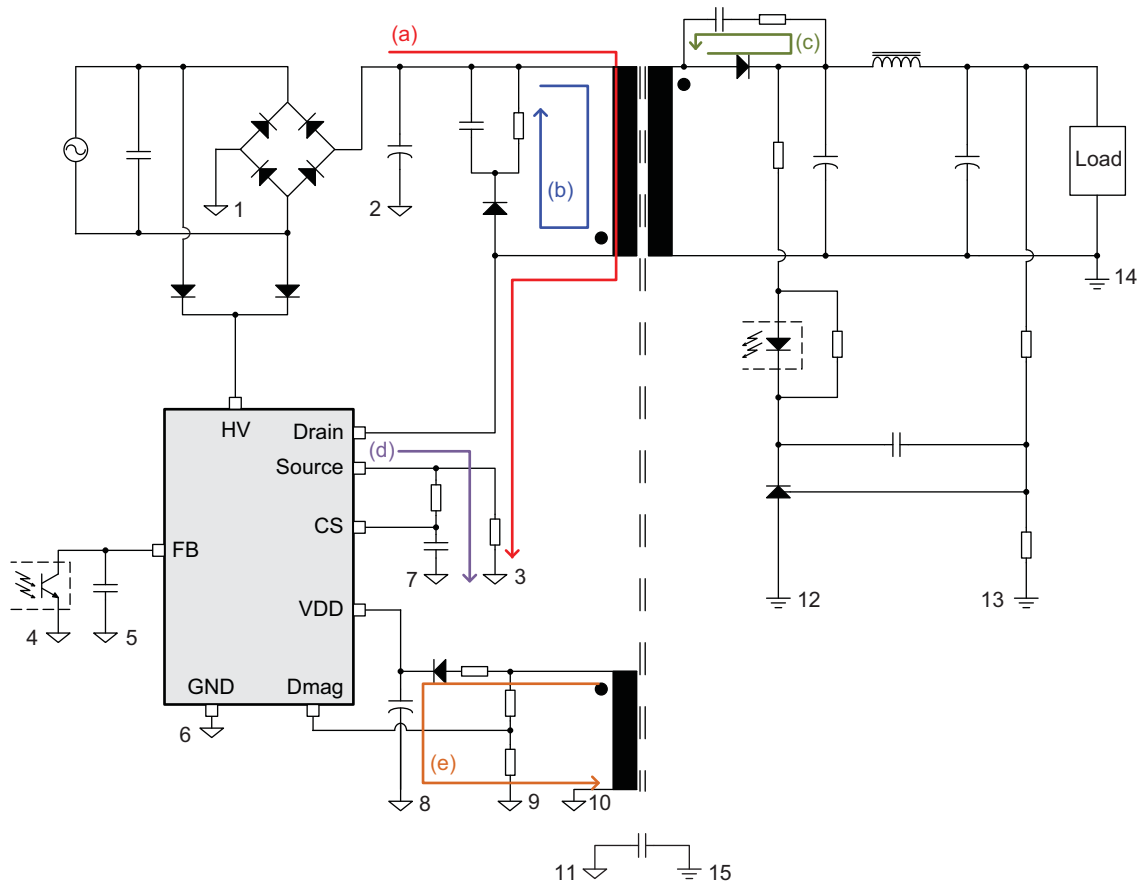


Figure 25. Main Loops for PCB Layout Considerations

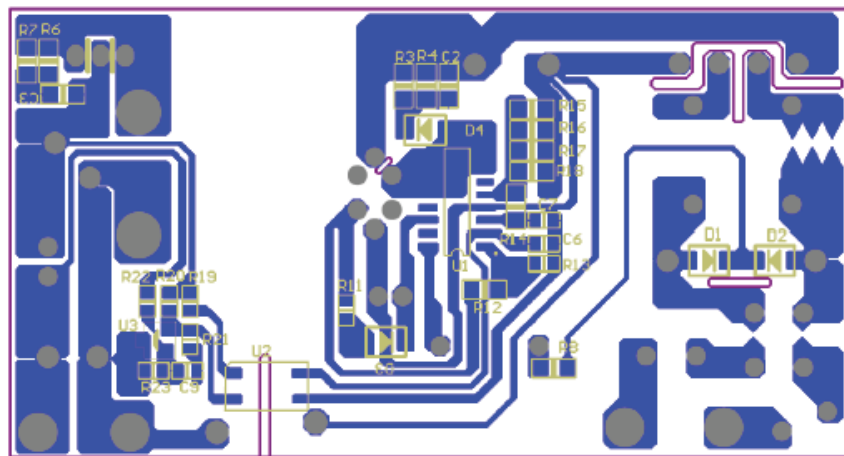
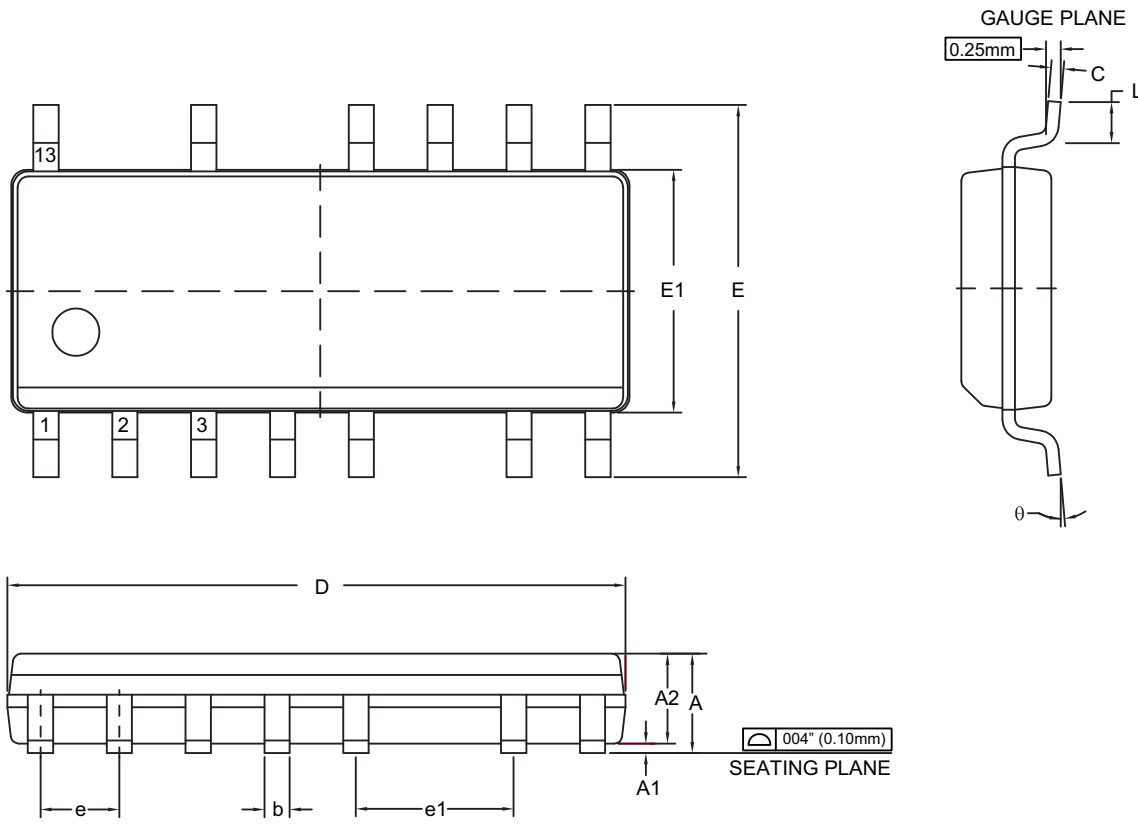
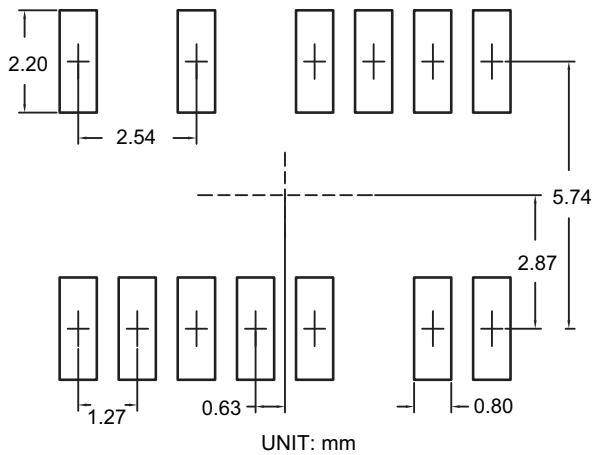


Figure 26. Recommended PCB Layout

Package Dimensions, SO-13L



RECOMMENDED LAND PATTERN



Dimensions in millimeters

| Symbols | Min. | Nom. | Max. |
|---------|----------|------|-------|
| A | 1.35 | 1.60 | 1.75 |
| A1 | 0.10 | — | 0.25 |
| A2 | — | 1.45 | — |
| b | 0.33 | — | 0.51 |
| c | 0.19 | — | 0.25 |
| D | 9.80 | — | 10.00 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | 1.27 TYP | | |
| E | 5.80 | 6.00 | 6.20 |
| L | 0.40 | — | 1.27 |
| θ | 0° | — | 8° |
| e1 | 2.54 TYP | | |

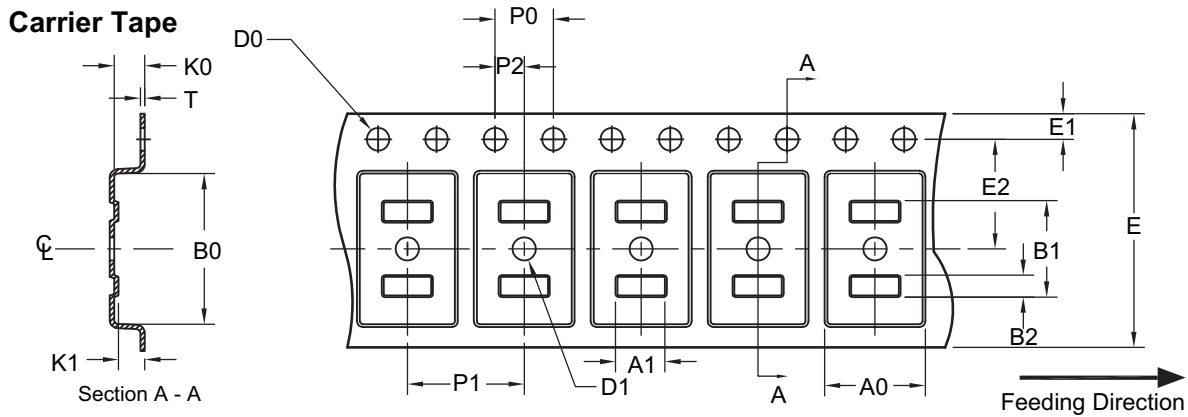
Dimensions in inches

| Symbols | Min. | Nom. | Max. |
|---------|-----------|-------|-------|
| A | 0.053 | 0.063 | 0.069 |
| A1 | 0.004 | — | 0.010 |
| A2 | — | 0.057 | — |
| b | 0.013 | — | 0.020 |
| c | 0.007 | — | 0.010 |
| D | 0.386 | — | 0.394 |
| E1 | 0.150 | 0.154 | 0.157 |
| e | 0.050 TYP | | |
| E | 0.228 | 0.236 | 0.244 |
| L | 0.016 | — | 0.050 |
| θ | 0° | — | 8° |
| e1 | 0.100 TYP | | |

Notes:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating.
3. Package body size exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils each.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.
5. Paddle exposed on bottom.

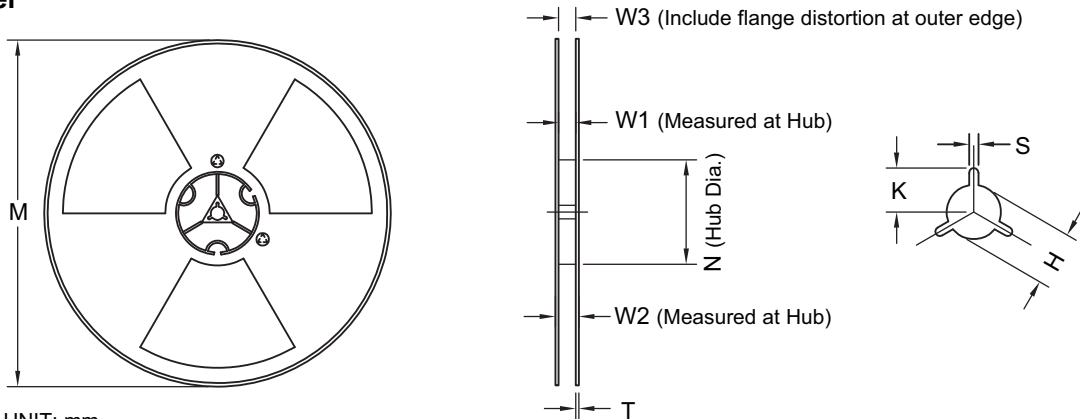
Tape and Reel Dimensions, SO-13L



UNIT: mm

| Package | A0 | B0 | K0 | K1 | D0 | D1 | E | E1 | E2 | P0 | P1 | P2 | T | B1 | B2 | A1 |
|-----------------|---------------|----------------|---------------|---------------|---------------|---------------|----------------|---------------|---------------|---------------|---------------|---------------|---------------|-------------|-------------|-------------|
| SO-13 (16mm) | 6.50 ±0.10 | 10.30 ±0.10 | 2.30 ±0.10 | 1.80 ±0.10 | 1.55 ±0.05 | 1.60 ±0.10 | 16.00 ±0.30 | 1.75 ±0.10 | 7.50 ±0.10 | 4.00 ±0.10 | 8.00 ±0.10 | 2.00 ±0.10 | 0.30 ±0.05 | REF. 6.6 | REF. 1.5 | REF. 3.5 |

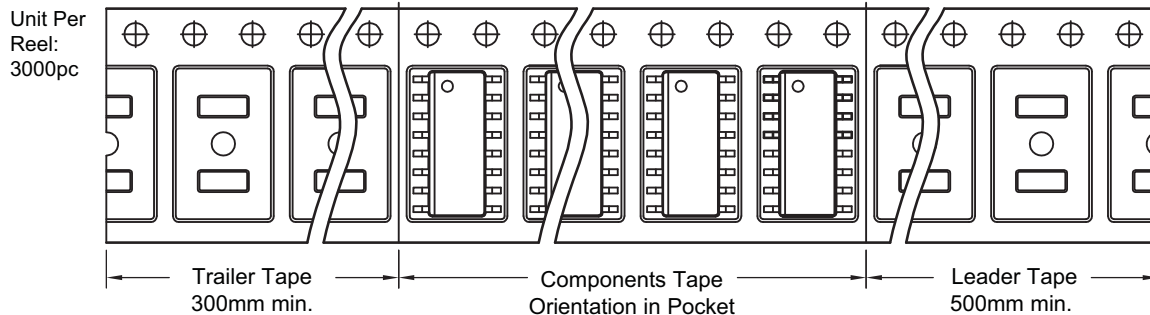
Reel



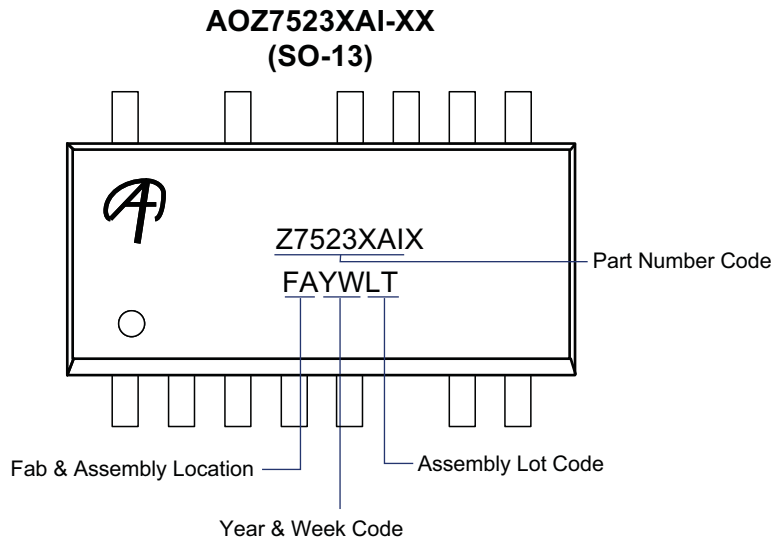
UNIT: mm

| Tape Size | M | N | T | W1 | W2 | W3 | S | K | H |
|-----------|--------------|------------------|---------------|----------------------|---------------|-----------|--------------|---------------|-----------------|
| 16mm | ø332 MAX. | ø100.00 ±2.00 | 2.00 ±0.05 | 16.40 +0.50/-0.20 | 22.40 MAX. | 15.9~19.4 | 2.20 TYP. | 10.10 MIN. | ø13.00 ±2.00 |

Leader/Trailer and Orientation



Part Marking



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|---|---|