

General Description

The AOZ8001 is a transient voltage suppressor array designed to protect high speed data lines from ESD and lightning.

This device incorporates four surge rated, low capacitance steering diodes and a TVS in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4. The TVS diodes provide effective suppression of ESD voltages: $\pm 15\text{kV}$ (air discharge) and $\pm 8\text{kV}$ (contact discharge).

The AOZ8001 comes in RoHS compliant, SOT-143 and SC-89 package and is rated over a -40°C to $+85^{\circ}\text{C}$ ambient temperature range. They are compatible with both lead free and SnPb assembly techniques.

The very small $1.7 \times 1.7 \times 0.6\text{mm}$ SC-89 package makes it ideal for applications where PCB space is a premium. The SC-89 has a flow through package design for an optimal and user friendly PCB layout design. The small size, low capacitance and high ESD protection makes it ideal for protecting high speed video and data communication interfaces.

Features

- ESD protection for high-speed data lines:
 - IEC 61000-4-2, level 4 (ESD) immunity test
 - $\pm 15\text{kV}$ (air discharge) and $\pm 8\text{kV}$ (contact discharge)
 - IEC 61000-4-5 (Lightning) 5A (8/20 μs)
 - Human Body Model (HBM) $\pm 15\text{kV}$
- Small package saves board space
- Low insertion loss
- Protects four I/O lines
- Low capacitance between I/O lines: 0.9pF
- Low clamping voltage
- Low operating voltage: 5.0V

Applications

- USB 2.0 power and data line protection
- Video graphics cards
- Monitors and flat panel displays
- Digital Video Interface (DVI)
- 10/100/1000 Ethernet
- Notebook computers

Typical Application

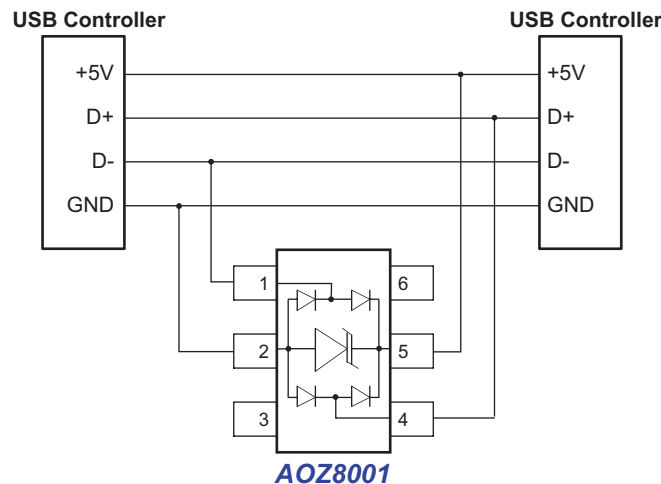


Figure 1. USB 2.0 High Speed Port

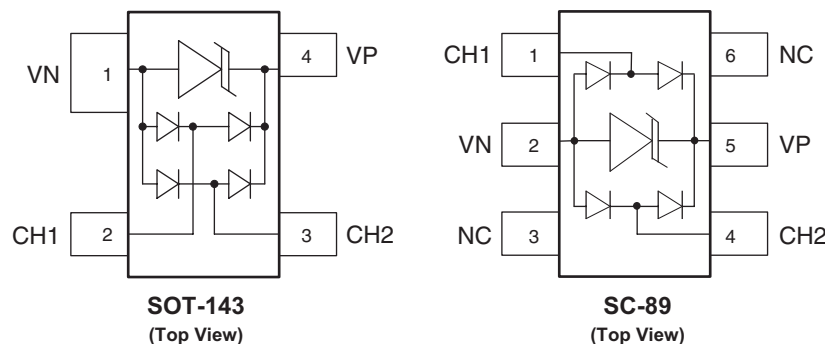
Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ8001KI	-40°C to +85°C	SC-89	RoHS Compliant
AOZ8001JI		SOT-143	



All AOS Products are offering in packaging with Pb-free plating and compliant to RoHS standards. Please visit www.aosmd.com/web/rohs_compliant.jsp for additional information.

Pin Configuration



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
VP – VN	6V
Peak Pulse Current (I_{PP}), $t_p = 8/20\mu s$	5A
Peak Power Dissipation (TBD @ 25°C)	
SOT-143	TBD
SC-89	TBD
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating per IEC61000-4-2, Contact ⁽¹⁾	±8kV
ESD Rating per IEC61000-4-2, Air ⁽¹⁾	±15kV
ESD Rating per Human Body Model ⁽²⁾	±15kV

Notes:

- IEC 61000-4-2 discharge with $C_{Discharge} = 150pF$, $R_{Discharge} = 330\Omega$.
- Human Body Discharge per MIL-STD-883, Method 3015 $C_{Discharge} = 100pF$, $R_{Discharge} = 1.5k\Omega$.

Maximum Operating Ratings

Parameter	Rating
Junction Temperature (T_J)	-40°C to +85°C

Electrical Characteristics

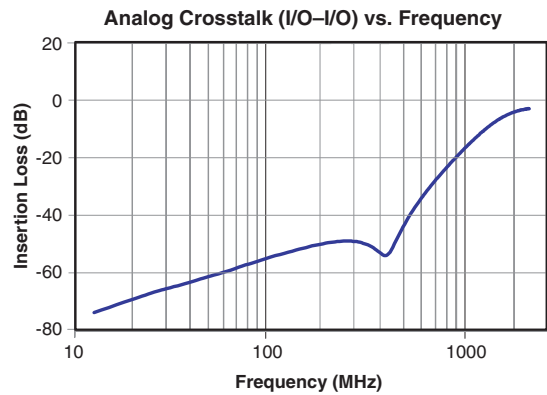
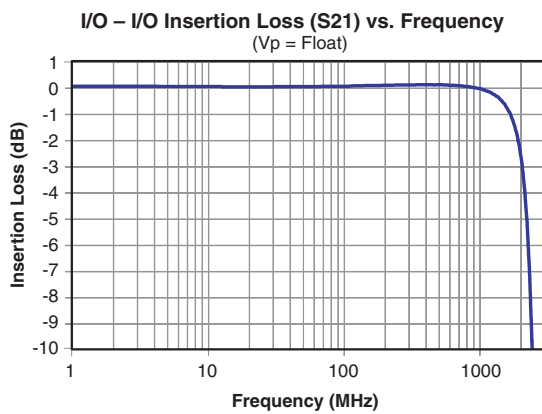
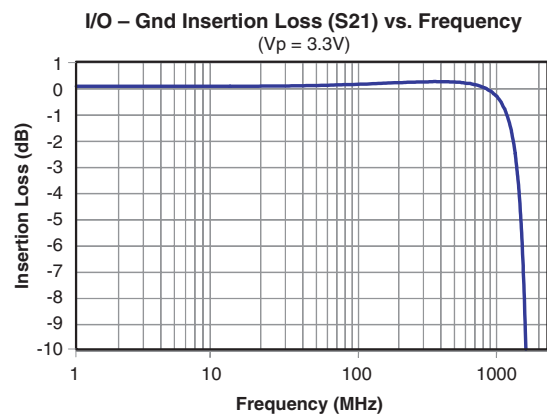
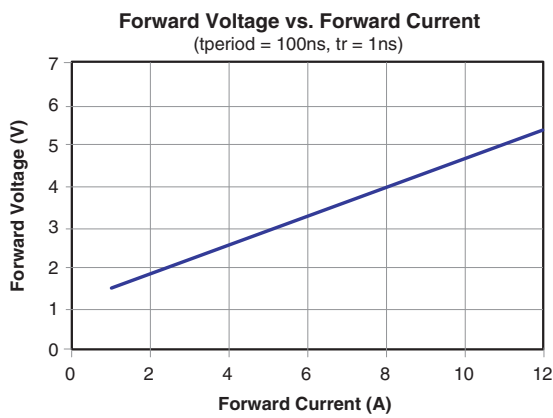
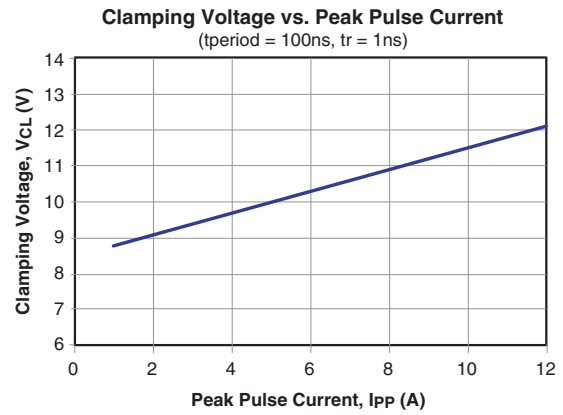
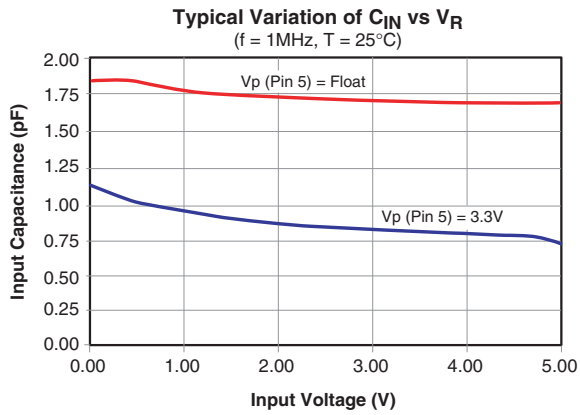
$T_A = 25^\circ\text{C}$ unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to $+85^\circ\text{C}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{RWM}	Reverse Working Voltage	Between pin 5 and 2 ⁽³⁾			5.5	V
V_{BR}	Reverse Breakdown Voltage	$I_T = 1\text{mA}$, between pins 5 and 2 ⁽⁴⁾	6.6			V
I_R	Reverse Leakage Current	$V_{RWM} = 5\text{V}$, between pins 5 and 2			0.1	μA
V_F	Diode Forward Voltage	$I_F = 15\text{mA}$	0.70	0.85	1	V
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transient	$I_{PP} = 1\text{A}$, $t_p = 100\text{ns}$, any I/O pin to Ground ⁽⁵⁾⁽⁷⁾			9.75 -1.52	V V
	Channel Clamp Voltage Positive Transients Negative Transient	$I_{PP} = 5\text{A}$, $t_p = 100\text{ns}$, any I/O pin to Ground ⁽⁵⁾⁽⁷⁾			10.42 -2.94	V V
	Channel Clamp Voltage Positive Transients Negative Transient	$I_{PP} = 12\text{A}$, $t_p = 100\text{ns}$, any I/O pin to Ground ⁽⁵⁾⁽⁷⁾			13 -5.75	V V
C_j	Junction Capacitance	$V_R = 0\text{V}$, $f = 1\text{MHz}$, any I/O pin to Ground ⁽⁵⁾		1.85	1.94	pF
		$V_R = 0\text{V}$, $f = 1\text{MHz}$, between I/O pins ⁽⁵⁾		0.9	0.94	pF
		$V_R = 0\text{V}$, $f = 1\text{MHz}$, any I/O pin to Ground ⁽⁶⁾		1.0	1.17	pF
ΔC_j	Channel Input Capacitance Matching	$V_R = 0\text{V}$, $f = 1\text{MHz}$, between I/O pins ⁽⁵⁾			0.03	pF

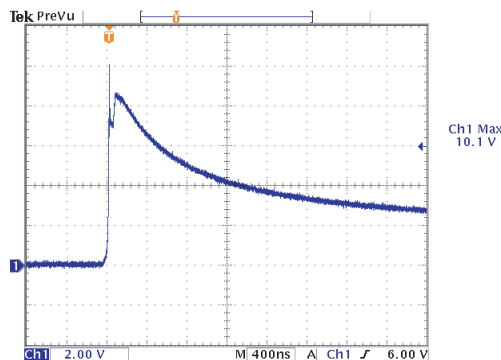
Notes:

- The working peak reverse voltage, V_{RWM} , should be equal to or greater than the DC or continuous peak operating voltage level.
- V_{BR} is measured at the pulse test current I_T .
- Measurements performed with no external capacitor on V_P (pin 5 floating).
- Measurements performed with V_P biased to 3.3 Volts (pin 5 @ 3.3V).
- Measurements performed using a 100ns Transmission Line Pulse (TLP) system.

Typical Performance Characteristics



ESD Response (8kV Contact per IEC61000-4-2)



Application Information

The AOZ8001 TVS is design to protect two data lines from fast damaging transient over-voltage by clamping it to a reference. When the transient on a protected data line exceed the reference voltage the steering diode is forward bias thus, conducting the harmful ESD transient away from the sensitive circuitry under protection.

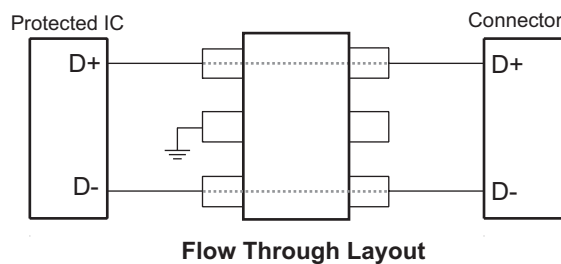
PCB Layout Guidelines

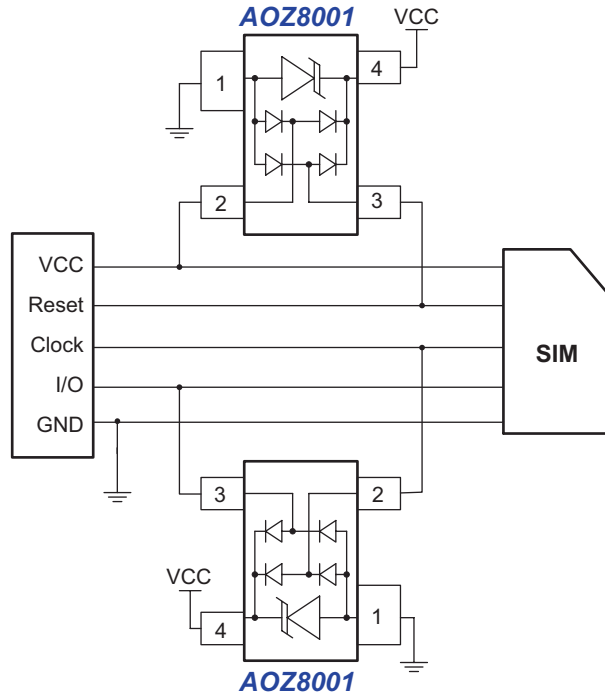
Printed circuit board layout is the key to achieving the highest level of surge immunity on power and data lines. The location of the protection devices on the PCB is the simplest and most important design rule to follow. The AOZ8001 devices should be located as close as possible to the noise source. The placement of the AOZ8001 devices should be used on all data and power lines that enter or exit the PCB at the I/O connector. In most systems, surge pulses occur on data and power lines that enter the PCB through the I/O connector. Placing the AOZ8001 devices as close as possible to the noise source ensures that a surge voltage will be clamped before the pulse can be coupled into adjacent PCB traces. In addition, the PCB should use the shortest possible traces. A short trace length equates to low impedance, which ensures that the surge energy will be dissipated by the AOZ8001 device. Long signal traces will act as antennas to receive energy from fields that are produced by the ESD pulse. By keeping line lengths as short as possible, the efficiency of the line to act as an antenna for ESD related fields is reduced. Minimize inter-connecting line lengths by placing devices with the most interconnect as close together as possible. The protection circuits should shunt the surge voltage to either the reference or chassis ground. Shunting the surge voltage directly to the IC's signal ground can cause ground bounce. The clamping performance of TVS diodes on a single ground PCB can be improved by minimizing the impedance with relatively short and wide ground traces. The PCB layout and IC package parasitic inductances can cause significant overshoot to the TVS's clamping voltage. The inductance of the PCB can be reduced by

using short trace lengths and multiple layers with separate ground and power planes. One effective method to minimize loop problems is to incorporate a ground plane in the PCB design. The AOZ8001 ultra-low capacitance TVS is designed to protect four high speed data transmission lines from transient over-voltages by clamping them to a fixed reference. The low inductance and construction minimizes voltage overshoot during high current surges. When the voltage on the protected line exceeds the reference voltage the internal steering diodes are forward biased, conducting the transient current away from the sensitive circuitry.

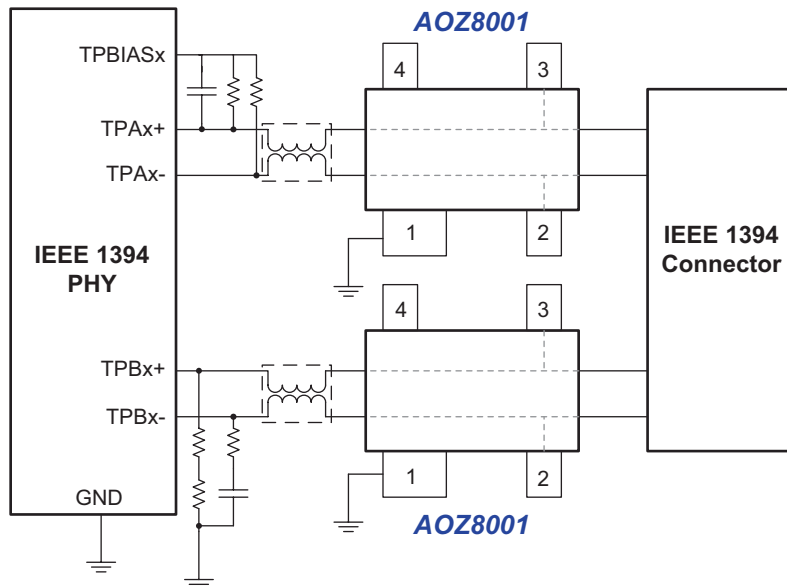
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

1. Place the TVS near the IO terminals or connectors to restrict transient coupling.
2. Fill unused portions of the PCB with ground plane.
3. Minimize the path length between the TVS and the protected line.
4. Minimize all conductive loops including power and ground loops.
5. The ESD transient return path to ground should be kept as short as possible.
6. Never run critical signals near board edges.
7. Use ground planes whenever possible.
8. Avoid running critical signal traces (clocks, resets, etc.) near PCB edges.
9. Separate chassis ground traces from components and signal traces by at least 4mm.
10. Keep the chassis ground trace length-to-width ratio <5:1 to minimize inductance.
11. Protect all external connections with TVS diodes.

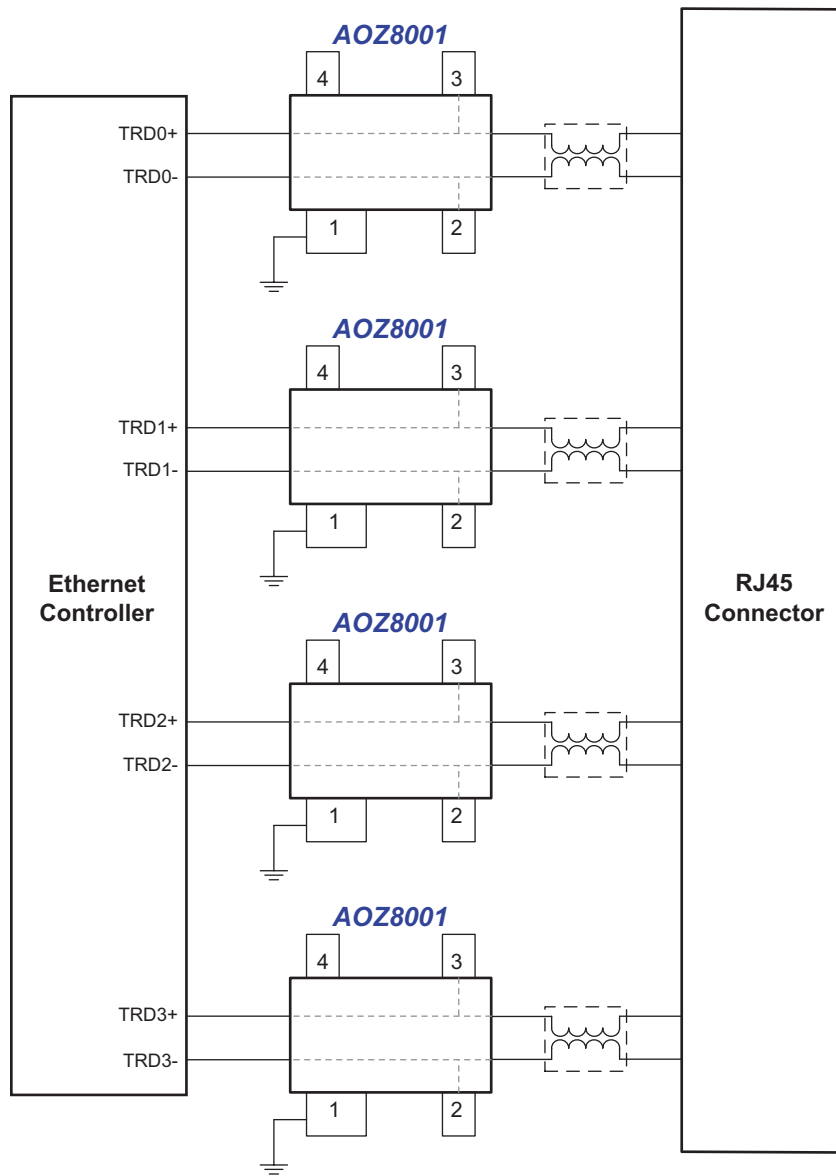




SIM Card Port Connection

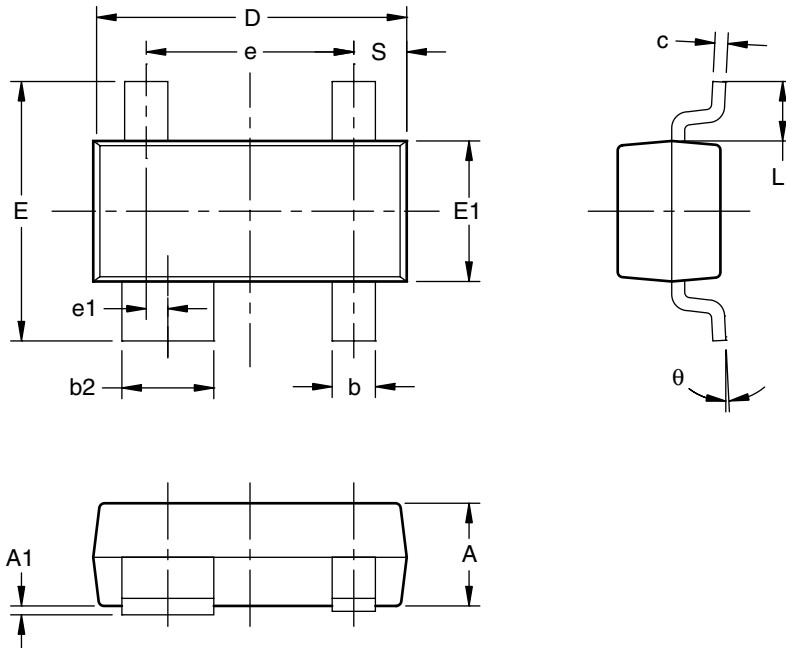


IEEE1394 Port Connection

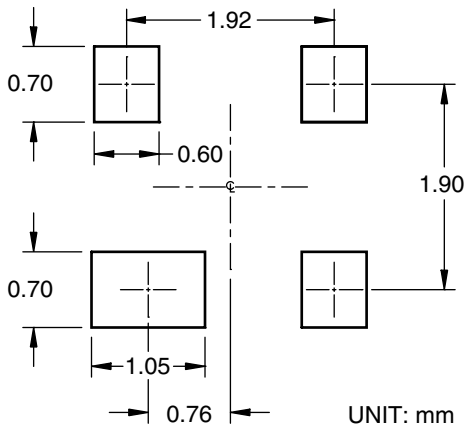


10/100 Ethernet Port Connection

Package Dimensions, SOT143-4L



RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.890	—	1.120
A1	0.013	—	0.100
b	0.370	—	0.510
b2	0.760	—	0.940
c	0.085	—	0.180
D	2.800	—	3.040
E	2.100	—	2.640
E1	1.200	—	1.400
e	1.920 BSC		
e1	0.200 BSC		
L1	0.550 REF		
S	0.450	—	0.600
θ	0°	—	8°

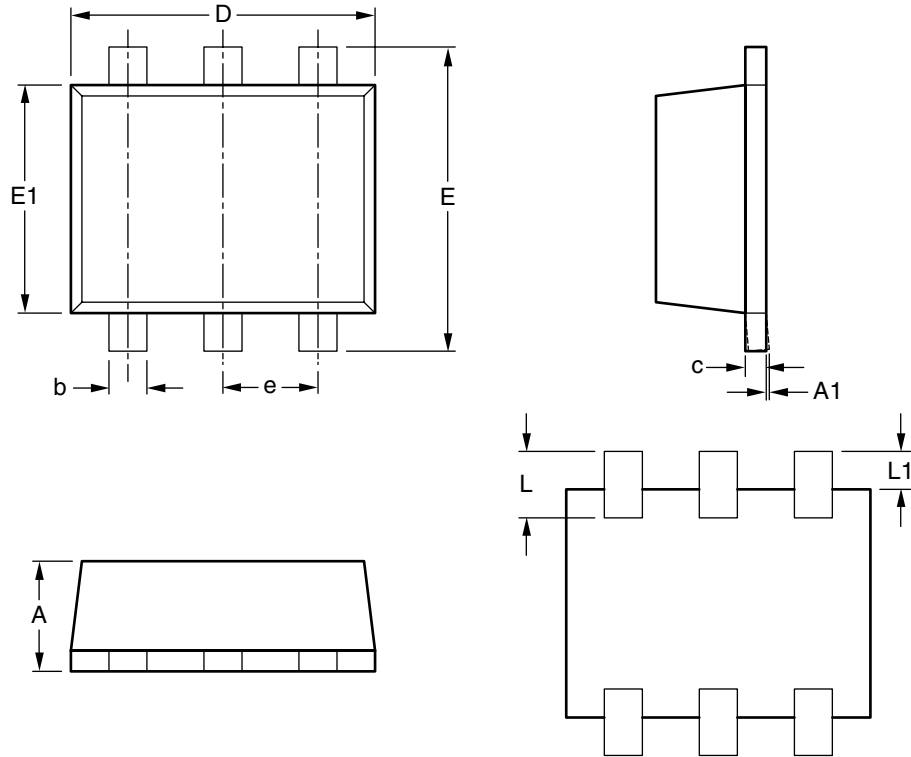
Dimensions in inches

Symbols	Min.	Nom.	Max.
A	0.035	—	0.044
A1	0.001	—	0.004
b	0.015	—	0.020
b2	0.030	—	0.037
c	0.003	—	0.007
D	0.110	—	0.120
E	0.083	—	0.104
E1	0.047	—	0.055
e	0.076 BSC		
e1	0.008 BSC		
L1	0.022 REF		
S	0.018	—	0.024
θ	0°	—	8°

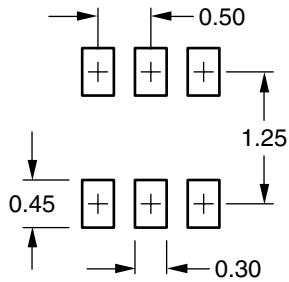
Notes:

1. All dimensions are in millimeters.
2. Tolerances are 0.10mm unless otherwise specified.
3. Package body sizes exclude mold flash and gate burrs.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

Package Dimensions, SC-89



RECOMMENDED LAND PATTERN



UNIT: mm

Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.53	0.58	0.62
A1	0.00	—	0.10
b	0.15	0.20	0.30
c	0.10	0.11	0.18
D	1.50	1.60	1.70
E	1.50	1.60	1.70
E1	1.10	1.20	1.30
e	0.50 BSC		
L	0.25	0.35	0.45
L1	0.13	0.20	0.27

Dimensions in inches

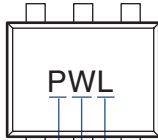
Symbols	Min.	Nom.	Max.
A	0.021	0.023	0.024
A1	0.000	—	0.004
b	0.006	0.008	0.012
c	0.004	0.004	0.007
D	0.059	0.063	0.067
E	0.059	0.063	0.067
E1	0.043	0.047	0.051
e	0.020 BSC		
L	0.010	0.014	0.018
L1	0.005	0.008	0.011

Notes:

1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per end. Dimension E1 does not include interlead flash or protrusion.
2. Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.
4. All dimensions are in millimeters.

Part Marking

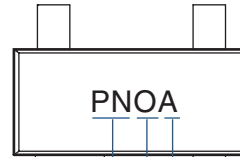
**AOZ8001KI
(SC-89)**



Part Number Code — Assembly Lot and Location Code
Week & Year Code

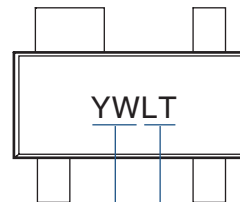
**AOZ8001JI
(SOT-143)**

Top Marking



Part Number Code — Assembly Location Code
Option Code

Bottom Marking



Year & Week Code — Assembly Lot Code

This datasheet contains preliminary data; supplementary data may be published at a later date. Alpha & Omega Semiconductor reserves the right to make changes at any time without notice.

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.