



Advanced Power
Electronics Corp.

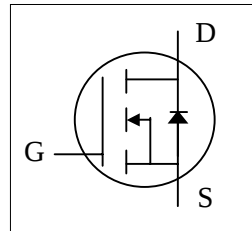
AP05N50S-HF

Halogen-Free Product

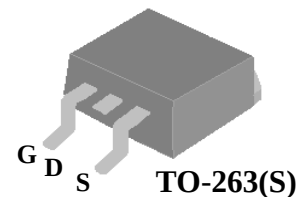
N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- ▼ 100% Avalanche Test
- ▼ Fast Switching Characteristic
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant & Halogen-Free



BV_{DSS}	500V
$R_{DS(ON)}$	1.4 Ω
I_D	5.0A



Description

The AP05N50 provide high blocking voltage to overcome voltage surge and sag in the toughest power system with the best combination of fast switching, ruggedized design and cost-effectiveness.

The TO-263 package is widely preferred for commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	500	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	5.0	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	2.8	A
I_{DM}	Pulsed Drain Current ¹	18	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation	73.5	W
E_{AS}	Single Pulse Avalanche Energy ²	45	mJ
I_{AR}	Avalanche Current	3	A
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	1.7	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient (PCB mount) ⁴	40	$^\circ\text{C}/\text{W}$



Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	500	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =2.7A	-	-	1.4	Ω
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2	-	4	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =2.7A	-	2.4	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =500V, V _{GS} =0V	-	-	25	uA
	Drain-Source Leakage Current (T _j =125°C)	V _{DS} =400V, V _{GS} =0V	-	-	250	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge ³	I _D =3.1A	-	19	30	nC
Q _{gs}	Gate-Source Charge	V _{DS} =400V	-	4.6	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	6.3	-	nC
t _{d(on)}	Turn-on Delay Time ³	V _{DD} =250V	-	11	-	ns
t _r	Rise Time	I _D =3.1A	-	8	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =12Ω, V _{GS} =10V	-	32	-	ns
t _f	Fall Time	R _D =80.6Ω	-	10	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	985	1580	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	85	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	3.3	-	pF
R _g	Gate Resistance	f=1.0MHz	-	2.5	3.8	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ³	I _S =4.5A, V _{GS} =0V	-	-	1.5	V
t _{rr}	Reverse Recovery Time ³	I _S =3.1A, V _{GS} =0V,	-	300	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	2.6	-	uC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Starting T_j=25°C , V_{DD}=50V , L=10mH , R_G=25Ω , I_{AS}=3A.
- 3.Pulse test
- 4.Surface mounted on 1 in² copper pad of FR4 board

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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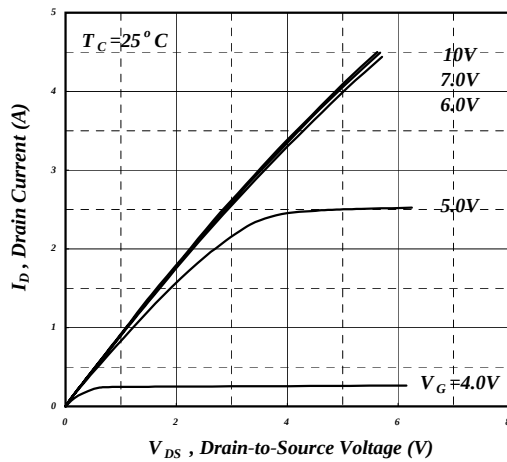


Fig 1. Typical Output Characteristics

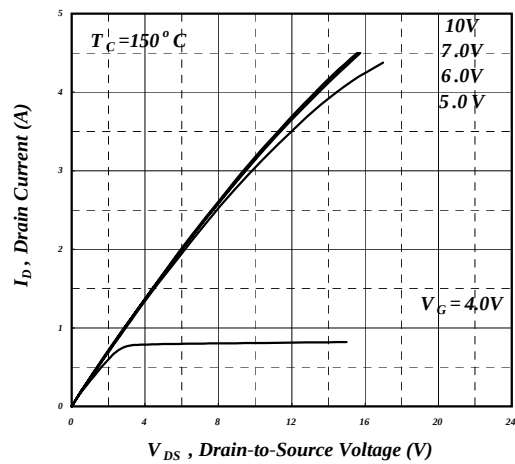


Fig 2. Typical Output Characteristics

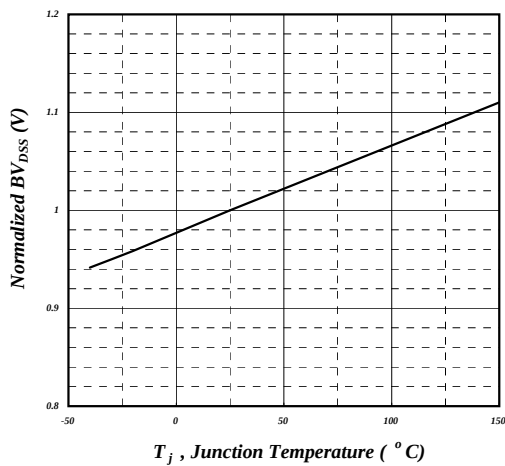


Fig 3. Normalized BV_{DSS} v.s. Junction Temperature

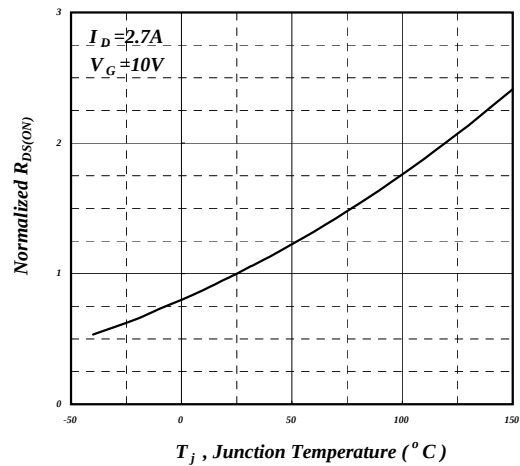


Fig 4. Normalized On-Resistance v.s. Junction Temperature

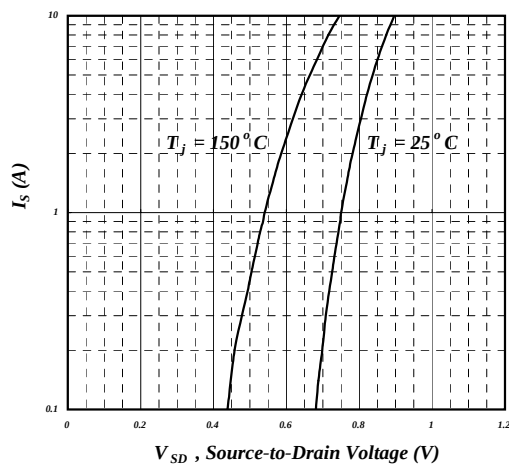


Fig 5. Forward Characteristic of Reverse Diode

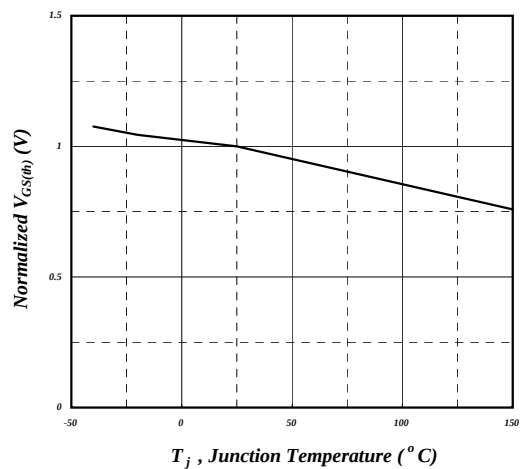


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

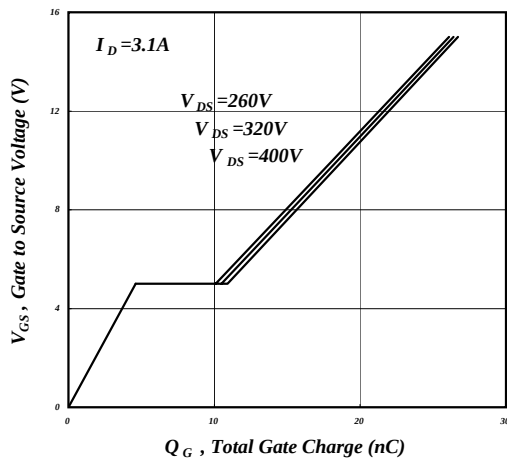


Fig 7. Gate Charge Characteristics

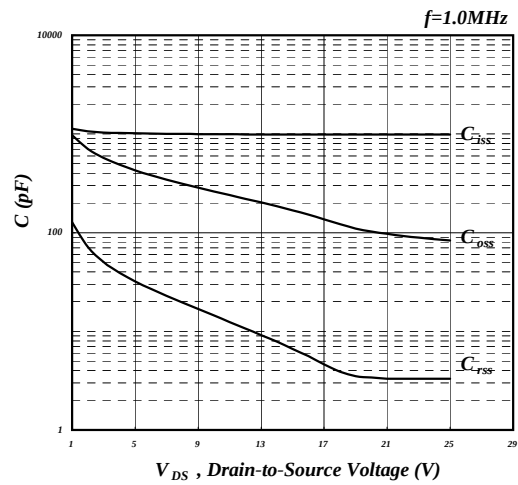


Fig 8. Typical Capacitance Characteristics

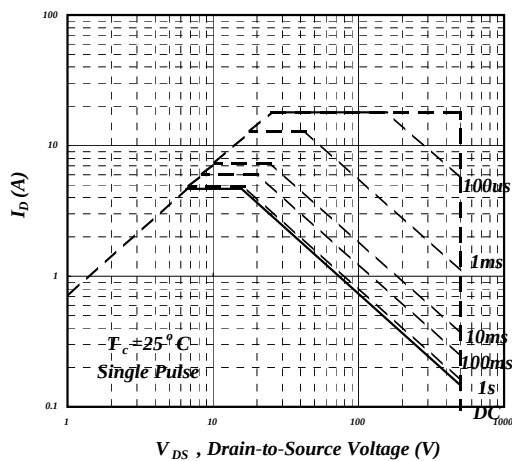


Fig 9. Maximum Safe Operating Area

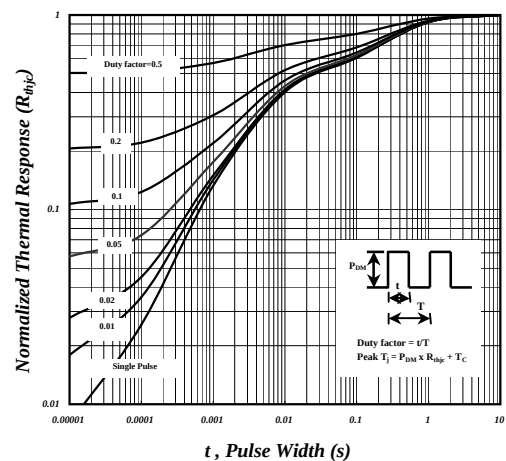


Fig 10. Effective Transient Thermal Impedance

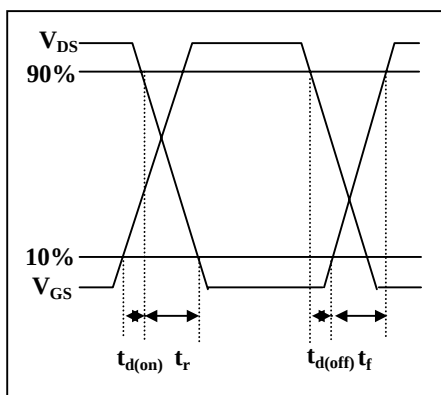


Fig 11. Switching Time Waveform

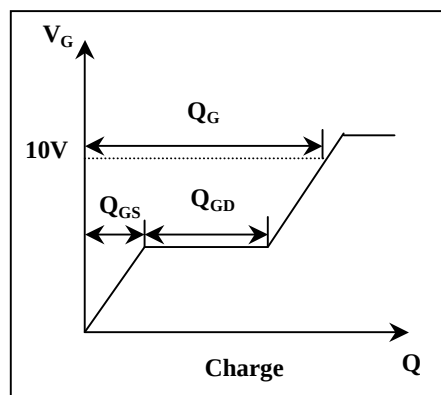


Fig 12. Gate Charge Waveform