AP1015BEN
10.5V 1ch H-Bridge Motor Driver IC

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1. Overview

The AP1015BEN has four drive mode of forward, reverse, brake and standby by 1 channel H-bridge Motor Driver corresponding to operating voltage 10.5V. The AP1015BEN layouts P-channel MOSFET for high side and N-channel LDMOSFET for low side in output circuit. This realizes a small package and less external parts. Under voltage detection and thermal shut down circuits are implemented. It is suitable for driving various small motors.

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2. Features

- Control Supply Voltage   2.7V to 5.5V
- Wide Motor Drive Operating Voltage   2.2V to 10.5V
- Maximum Output Current (DC)   1.1A @Ta=25°C, 0.8A @Ta=85°C
- Maximum Output Current (Peak) 1.4A (Ta=25°C, within 10ms in 100ms or within 20ms in 200ms)
- Maximum Output Current (Peak) 2.0A (Ta=25°C, 100ms within 5ms or within 10ms in 200ms)
- H-Bridge On Resistance   RON(TOP+BOT)=0.5 Ω (typ) @Ta=25°C
- Built-in Under Voltage Detection Circuit   Detect VC supply voltage under 2.2V(typ)
- Built-in Thermal Shut Down Circuit (Tj)   175°C (typ)
- Junction Temperature   150°C (max)
- Package   8-pin SON

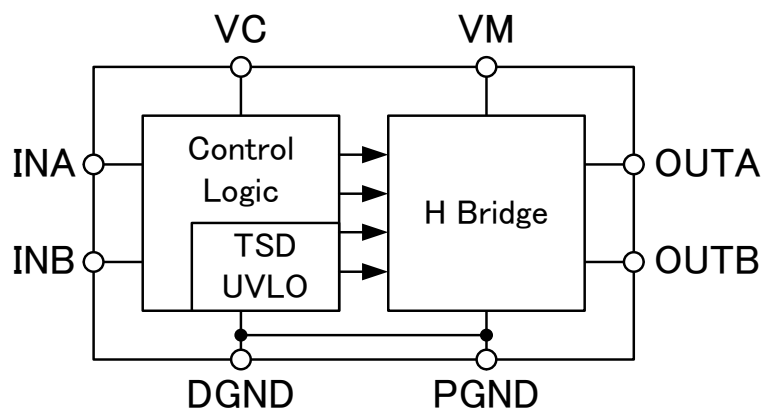| 3.	Table of Contents

4. Block Diagram

Figure 1. Block Diagram

5. Ordering Guide

AP1015BEN   -30°C ～+85°C   8-pin SON

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6. Pin Configuration and Functions

■ **Pin Configuration**

VM OUTA OUTB PGND

| 8 | 7 | 6 | 5 |

Exposed Pad(GND)

Steam Via

| 1 | 2 | 3 | 4 |

VC INA INB DGND

(Top view)
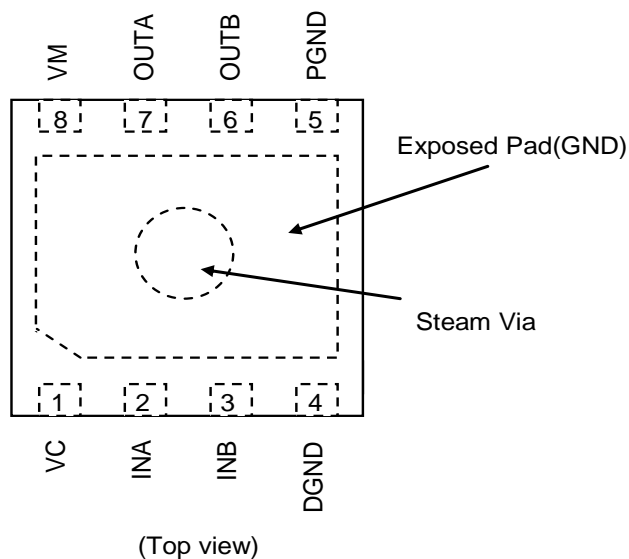
■ **Pin Functions**

Pin No.	Pin Name	I/O (Note 1)	Function	Description
1	VC	P	Control Power Supply	
2	INA	I	Control Signal Input Terminal	100kΩ pull-down
3	INB	I	Control Signal Input Terminal	100kΩ pull-down
4	DGND	P	Ground Terminal	
5	PGND	P	Power Ground Terminal	
6	OUTB	O	Motor Driver Output Terminal	
7	OUTA	O	Motor Driver Output Terminal	
8	VM	P	Motor Driver Output Supply	
Exposed Pad	EP	-	Exposed Pad	(Note 2)

Note 1. I (Input terminal)、O (Output terminal)、P(Power terminal)
Note 2. EP is Power Ground. EP is necessary soldered to GND.

■ Terminal Equivalent Circuit

Pin name	Name	Functions	Equivalent Circuit
1	VC	Control Power Supply	VC/VM
8	VM	Motor driver power supply	
2 3	INA INB	Logic Input	INA/INB 2k 2k 100k
7 6	OUTA OUTB	Motor Driver Output	VM OUTA OUTB PGND
4 5	DGND PGND	Ground Terminal Power Ground Terminal	DGND PGND
EP	EP	Exposed Pad	-

7. Absolute Maximum Ratings

(Ta = 25°C unless otherwise specified.)

Parameter	Symbol	min	max	Unit	Condition
Control Supply Voltage	VC	-0.5	6	V	
Motor Driver Supply Voltage	VM	-0.5	12	V	
Input Terminal Voltage(INA, INB)	Vterminal	-0.5	5.5	V	
Maximum DC Output Current	Iout1	-	1.1	A	Ta=25°C, OUTA and OUTB terminal
		-	0.8	A	Ta=85°C, OUTA and OUTB terminal
Maximum Peak Output Current	Iout2	-	1.4	A	OUTA and OUTB terminal within 20ms in 200ms
		-	2.0	A	OUTA,OUTB端子 within 10ms in 200ms
Power Dissipation	PD	-	1250	mW	(Note 4) Ta=25°C
		-	650	mW	(Note 4) Ta=85°C
Operating Temperature Range	Tj	-	150	°C	
Storage Temperature	Tstg	-65	150	°C	

Note 3. All above voltage is defined to VSS (DGND/PGND terminal voltage)
Note 4. This is calculated as RθJ=100 °C /W. EP terminal is connected ground.
Note 5. The each power supply of VC and VM is sequence-free.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.
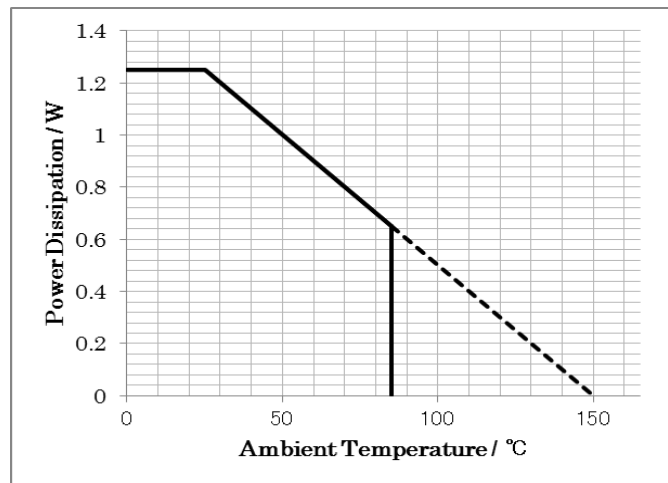
Figure 2. Power Dissipation

8. Recommended Operation Conditions

Parameter	Symbol	min	typ	max	Unit	Condition
Control Supply Voltage	VC	2.7	3.3	5.5	V	
Motor Driver Supply Voltage	VM	2.2	-	10.5	V	
Input Frequency Range	Fin	-	-	200	kHz	50%duty
Operating Temperature Range	Ta	-30	-	85	°C	

9. Electric Characteristics						
(Ta = 25°C, VM=7.2V, VC = 3.3V unless otherwise specified.)						
Parameter	Symbol	Condition	min	typ	max	Unit
UVLO						
VC under voltage detect voltage	VC_{UV}		1.9	2.2	2.5	V
TSD						
Thermal shut down temperature (Note 6)	T_{TSD}		150	175	200	°C
Temperature hysteresis(Note 6)	T_{TSDHYS}		20	30	40	°C
Quiescent Current						
VM quiescent current at standby	I_{VMPS}	INA="L", INB= "L"	-	-	1.0	μA
VC quiescent current at standby	I_{VCPS}	INA="L", INB= "L"	-	-	1.0	μA
VM quiescent current at brake	I_{VM}	INA="H", INB= "H"	-	100	200	μA
VC quiescent current at brake	I_{VC}	INA="H", INB= "H"	-	100	150	μA
VC quiescent current at PWM operation	I_{VCPWM}	INA=200kHz, INB="H"	-	200	300	μA
Motor Driver						
Driver on resistance (High side + Low side)	R_{ON1}	VC=3.3V, Iout=100mA Ta=25°C	-	0.5	0.8	Ω
Driver on resistance (High side + Low side) (Note 6)	R_{ON2}	VC=3.3V, Iout=1.1A Ta=25°C	-	0.65	0.9	Ω
Driver on resistance (High side + Low side) (Note 6)	R_{ON3}	VC=3.3V, Iout=0.8A Ta=85°C	-	0.75	1.0	Ω
Body diode forward voltage	V_F	I_F=100mA	-	0.8	1.2	V
H-Bridge propagation delay time (Standby→CW or CCW)	t_{PDZH}	tr=tf=10ns (OUTB. Note 8,Figure 3)	-	0.5	1.0	μs
H-Bridge propagation delay time (brake→CW or CCW)	t_{PDH}	tr=tf=10ns (Note 7,Figure 3)	-	0.2	1.0	μs
H-Bridge propagation delay time (CW or CCW→Standby)	t_{PDHZ}	tr=tf=10ns (OUTB. Note 8,Figure 3)	-	0.1	1.0	μs
H-Bridge propagation delay time (CW or CCW→Brake)	t_{PDL}	tr=tf=10ns (Note 7,Figure 3)	-	0.15	1.0	μs
Control Logic						
Input "H" level voltage (INA, INB)	V_{IH}	VC=2.7 to 5.5V	0.7 × VC	-	-	V
Input "L" level voltage (INA, INB)	V_{IL}	VC=2.7 to 5.5V	-	-	0.3× VC	V
Input "H" level current (INA, INB)	I_{IH}	Vterminal=3.3V	20	33	46	μA
Input "L" level current (INA, INB)	I_{IL}	VC=2.7 to 5.5V	-1.0	-	-	μA

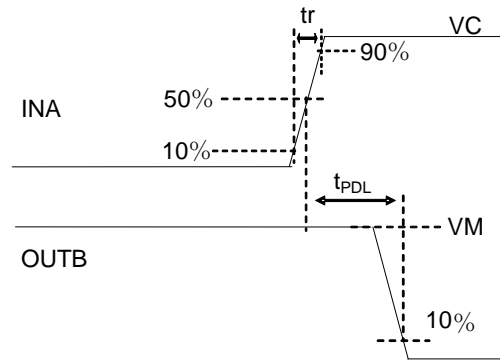Note 6. Not tested under mass-production.
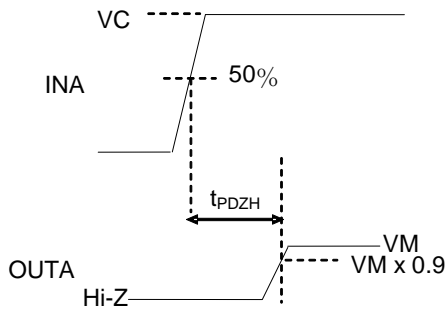Note 7. Connect 1kΩ between OUTA and OUTB.
Note 8. Connect 1kΩ between VM and OUTA/B, and OUTA/B and GND.

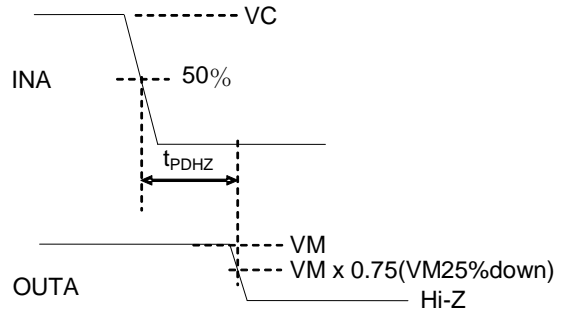Figure 3. Timing Chart（delay time）
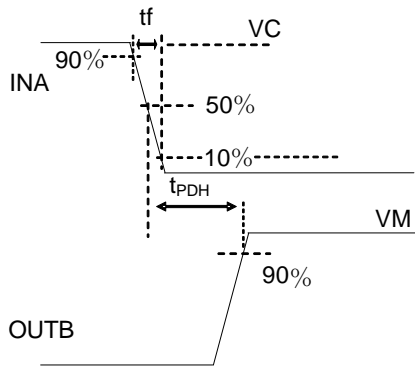
(a) delay time
(INB="H", brake→CCW)

(b) delay time
(INB="H", CCW→Brake)

(c) delay time
(INB = "L", Standby→CW)

(d) delay time
(INB = "L", CW→Standby)

10. Control Logic

The AP1015BEN is suitable to drive DC motor and voice coil motor. If the input signals are fed to INA and INB, the output signals, OUTA and OUTB are decided as Table 1.The AP1015BEN includes Under Voltage Lock Out (UVLO) and Thermal Shut Down (TSD) circuits. The UVLO circuit monitors the control voltage (VC). If the VC is less than the specified voltage, the output of the H-bridge goes to high impedance. The TSD circuit monitors the chip temperature. If the temperature of the chip exceeds specified temperature, the output of the H-bridge goes to high impedance. UVLO circuit and TSD circuit have hysteresis levels.

Table 1. Control Logic

Input		Output		Operation
INA	INB	OUTA	OUTB	
L	L	Z	Z	Standby(Coast)(Note 9)
L	H	L	H	Reverse (CCW)
H	L	H	L	Forward (CW)
H	H	L	L	Brake

Note 9. In standby mode, all the circuits include the TSD circuit are stopped.

The TSD circuit may not operate in the PWM operation which repeats CW(CCW) → standby.

It is recommended to use PWM operation with CW(CCW) → brake.
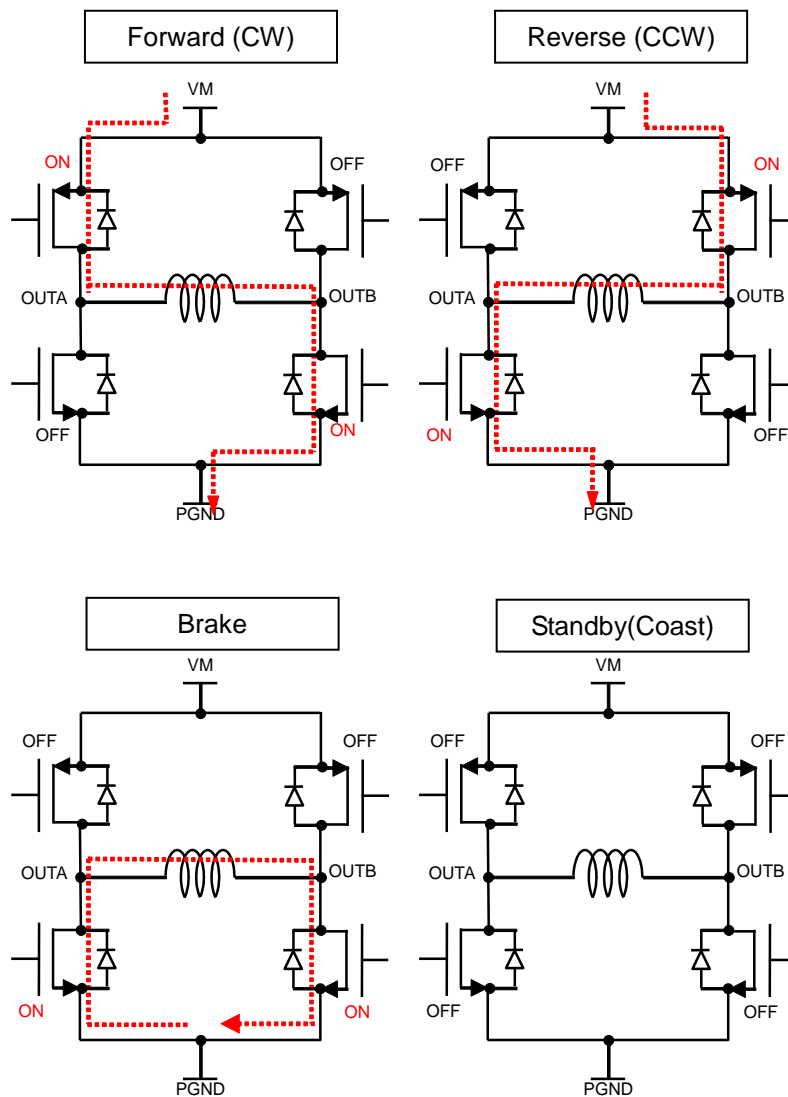
Figure 4. Direction of current
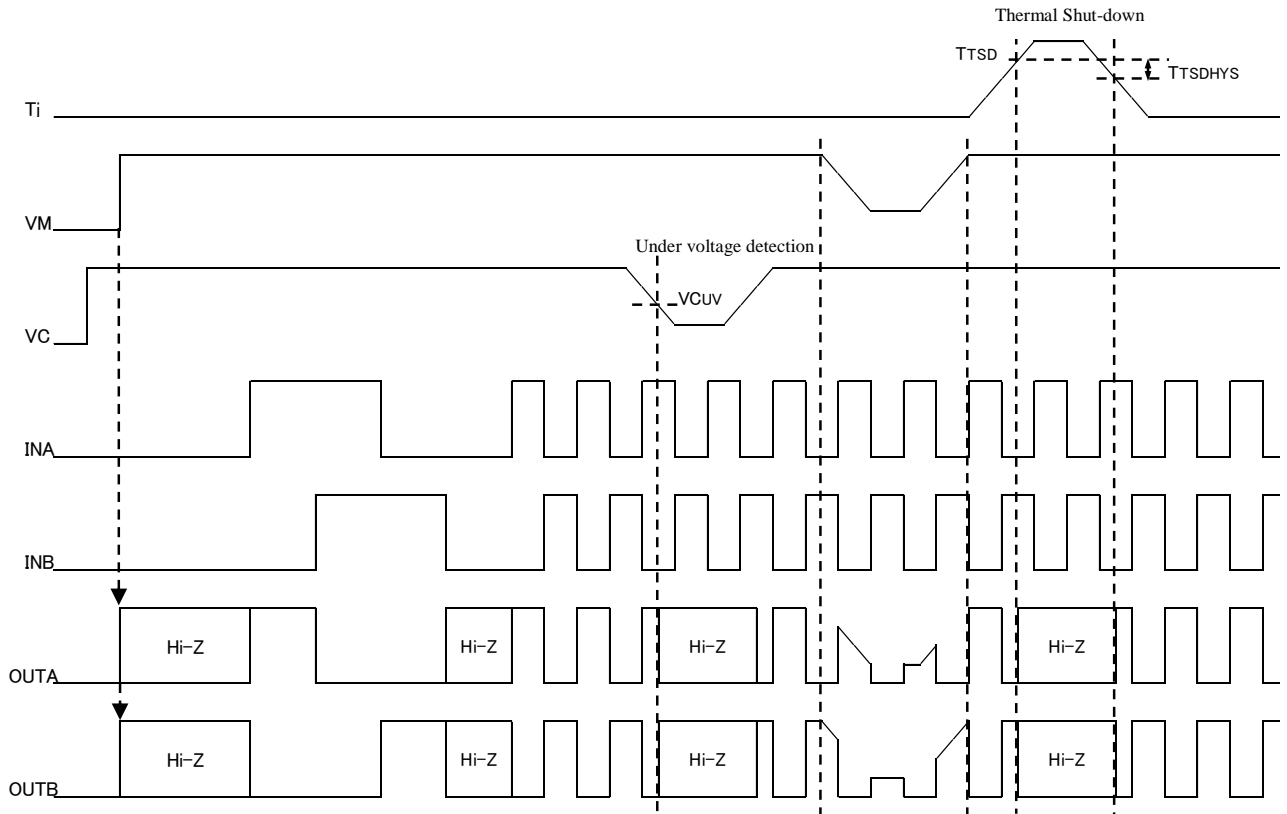
Figure 5. Timing Chart

11. Recommended External Circuit
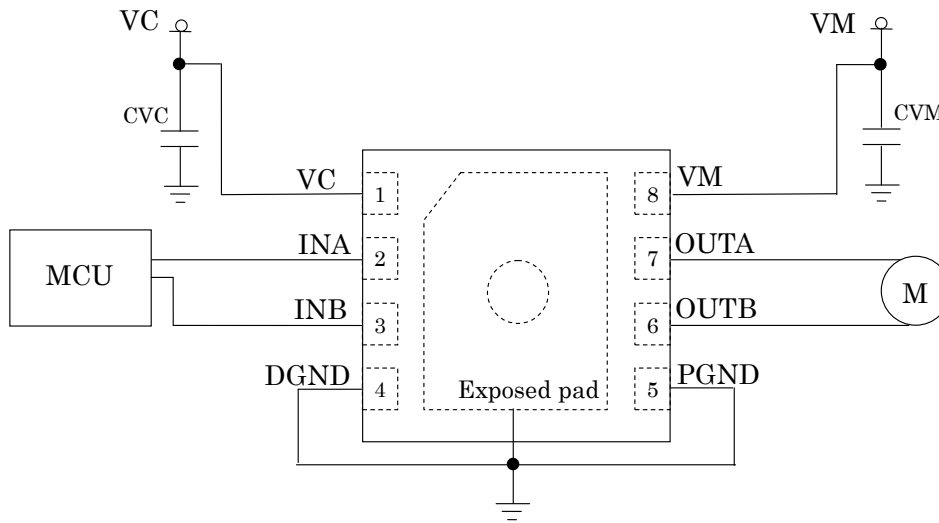
Figure 6. Recommended External Circuit(Top view)

Table 2. Parts List

Parameter	Symbol	min	typ	max	Unit	Notes
Motor driver power supply (decoupling capacitor)	CVM	1.0	10.0	-	μF	(Note 10)
Control power supply (decoupling capacitor)	CVC	0.1	1.0	-	μF	(Note 10)

Note 10. CVM and CVC should be near terminals. Please adjusts the connecting capacitor of CVM and CVC depending on the load current profile, the load capacitance, the line resistance and etc. with each application boards.

12. Package

■ Outline Dimentions

・8-pin SON (Unit : mm)

Top View
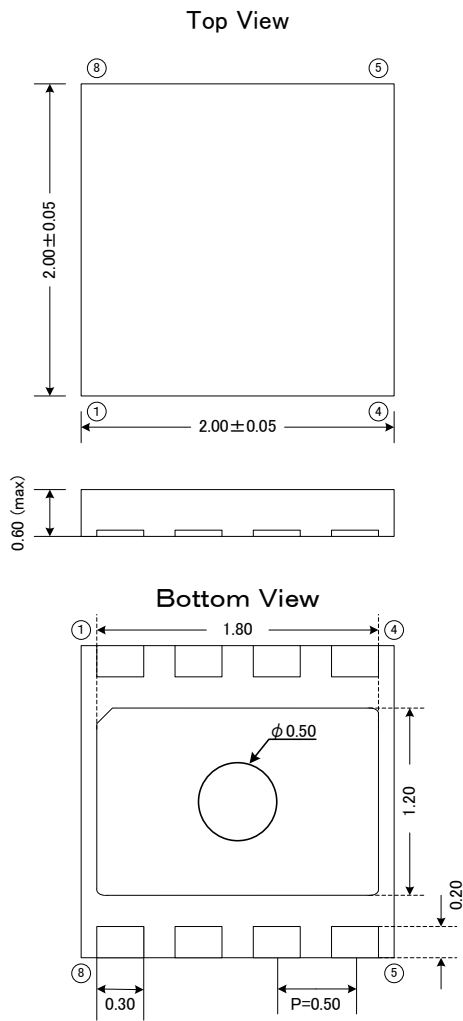
Recommended foot pattern

Bottom View
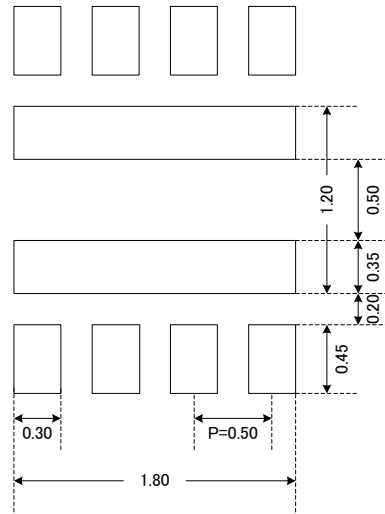
Note) The Exposed Pad is Power Ground.
The Exposed Pad is necessary soldered to PCB.
Please layout the foot pattern of Exposed Pad not
to surround the steam via of the IC.

Unit : mm

■ Marking

1015B
ABCD
●

Market No.

Date Code

Pin #1 Indication
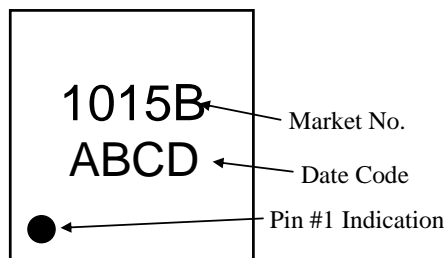
ABCD: Date code (4 digit)
　　A: Year code (last 1 digit)
　BC: Week code
　　D: Management code

13. Revise History

Date (YY/MM/DD)	Revision	Page	Contents
15/08/12	00	-	First Edition

—————— IMPORTANT NOTICE ——————