

AP1016AEN

9.0V Dual H-Bridge Motor Driver IC

1. Genaral Description

The AP1016 includes 2 channel H-bridge drivers in one package. It also includes Under Voltage Detection and Thermal Shut Down circuits. It is suitable for driving stepper motor and voice coil motors.

2. Features

- 2 channel H-bridge drivers in one package
- Power Supply Voltage Range Control (VC) 2.7V ~ 5.5V Motor (VM) 2.0V ~ 9.0V
- Output Current 0.7A(DC)
- H-Bridge ON Resistance : RDSON (TOP+BOT)=0.54Ω @25°C or 0.72Ω @85°C
- PWM Pulse Input max 200kHz
- Built in Flow-through Current Protection Circuit
- Built in Charge Pump Circuit
- Built in UVLO & TSD Circuits
- Package 16-pin QFN 3mm×3mm

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4. Block Diagram

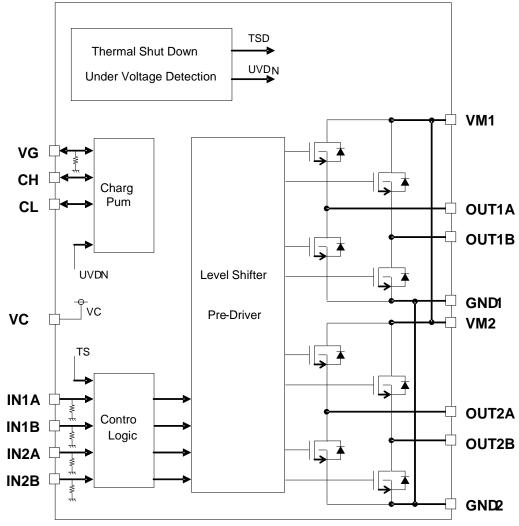


Figure 1. Block Diagram

• H-bridge driver block

NMOS type FETs are applied both high side and low side FETs of a H-bridge.

- Charge pump block It generates the drive voltage (VG) of gate for a high side FET.
- Control logic block

Each H-bridge driver is controlled by two input signal IN1/2A or IN1/2B.

- Level shifter & pre-driver block Control signals for the high side FET is shifted VG voltage and then drive the gate of the high side FET.
- Under Voltage Detection

It is monitoring the control voltage (VC), if the VC is less than the specified voltage, the output of the H-bridge goes to high impedance.

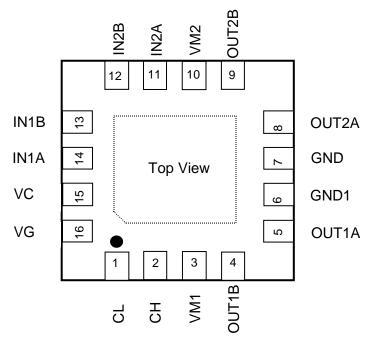
• Thermal Shut Down If the temperature of the chip is more than the specified temperature, the output of the H-bridge goes to high impedance.

5. Ordering Guide

AP1016AEN -40~85°C 16-pin QFN 3mm×3mm



Pin Configurations



Function

Pin No.	Name	I/O (Note 1)	Functions	Comments
1	CL	I/O	Charge pump capacitor	
2	CH	I/O	Charge pump capacitor	
3	VM1	Р	Motor driver power supply	
4	OUT1B	0	Motor driver output	CH1
5	OUT1A	0	Motor driver output	CH1
6	GND1	Р	Power Ground	
7	GND2	Р	Power Ground	
8	OUT2A	0	Motor driver output	CH2
9	OUT2B	0	Motor driver output	CH2
10	VM2	Р	Motor driver power supply	
11	IN2A	Ι	Control signal input	CH2, 200kΩ (Typ) pull down
12	IN2B	Ι	Control signal input	CH2, 200k Ω (Typ) pull down
13	IN1B	Ι	Control signal input	CH1, 200kΩ (Typ) pull down
14	IN1A	Ι	Control signal input	CH1, 200kΩ (Typ) pull down
15	VC	Р	Control circuit power supply	
16	VG	Р	Charge pump output capacitor	
Exposed Pad	EP	-	Thermal pad	The pad must be connected to the ground.

Note 1. I (Input terminal), O (Output terminal) and P (Power terminal)

Parameter	Symbol	min	max	Unit	Comments
Control supply voltage	VC	-0.5	6.0	V	
Motor supply voltage1	VM	-0.5	9.5	V	
VC level terminal voltage (IN1A, IN1B, IN2A and IN2B)	Vterm1	-0.5	VC	V	
VM level terminal voltage (OUT1A, OUT1B, OUT2A, OUT2B and CL)	Vterm2	-0.5	VM	V	
VC+VM level terminal voltage (CH, VG)	Vterm3	-0.5	15.5	V	
Maximum output current	Iload1	-	1.0	Α	Ta=25°C
Maximum output current	Iload2	-	0.7	Α	Ta=85°C
Maximum output peak current	Iload3	-	1.4	Α	(Note 3)
Power dissipation	PD1	-	2.0	W	(Note 4),Ta=25°C
Power dissipation	PD2	-	1.0	W	(Note 4),Ta=85°C
Storage temperature	Tstg	-40	150	°C	

7. Absolute Maximum Ratings

Note 2. All above voltage is defined to GND1/2=0V.

Note 3. Under 10ms in 200ms

Note 4. When the 2-layer (pattern rate: 150%) board is used. This is calculated by $R\theta J = (60)^{\circ}C/W$.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is guaranteed at these extremes.

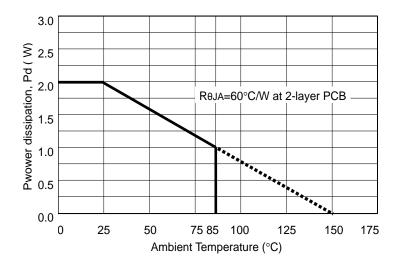


Figure 2. Maximum Power Dissipation

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8. Recommended Operating Conditions									
	$(Ta = 25^{\circ}C \text{ unless otherwise specified. (Note 2)})$								
Parameter	Symbol	min	typ	max	Unit	Comments			
Motor driver supply voltage	VM	2.0	5.0	9.0	V				
Control supply voltage	VC	2.7	3.0	5.5	V				
Input pulse frequency	FIN	-	-	200	kHz	Duty=50%(input pulse)			
Ambient temperature	Та	-40	-	85	°C				
Maximun junction temperature	Tj	-	-	150	°C				

9. Electrical Characteristics							
(Operating condi-	tions; Ta = 25°C	C, VM= $5.0V$ and VC = $3.0V$, ur	less oth	erwise sp	pecified.,(Note 2	
Parameter	Symbol	Condition	min	typ	max	Uni	
Current consumption							
VM stand by current	IVM STBY	IN1A=IN1B=IN2A=		35	100	μΑ	
VC stand by current	IVC STBY	IN2B="L"		135	400	μΑ	
VC current	IVC	IN1A=IN2A="L" IN1B=IN2B=200kHz		500	800	μΑ	
VM stand by current (In under voltage detection mode)	IVM UVD	VM = 5.0V $VC = 0V$		0.1	1.0	μΑ	
Charge pump							
Charge pump voltage	VG	VG = VM + VC, Iload=0A			8.0	V	
Charge pump wake up time (Figure 4, Figure 5)	tVGON	VC > VCUV		0.3	3.0	ms	
H-bridge driver	·	•		•			
H-bridge driver High or Low side ON resistance	RON1	VC = 3V, Iload = 100mA Ta = 25°C		0.27	0.31	Ω	
H-bridge driver High or Low side ON resistance	RON2	VC = 3V, Iload = 700mA Ta = 25°C Guaranteed by design (Note 6)		0.32	0.37	Ω	
H-bridge driver High or Low side ON resistance	RON3	VC = 3V, Iload = 700mA Ta = 85°C Guaranteed by design (Note 6)		0.36	0.43	Ω	
H-bridge driver Body diode forward voltage	Vf	If = 100mA		0.8	1.2	v	

Symbol	Condition	min	typ	max	Unit
tPDLH	Load=1 kΩ between OUTA and OUTB Refer to Figure 3(a) IN1A=IN2A=L IN1B=IN2B=200kHz		0.07	0.3	μs
tPDHL			0.17	0.3	μs
tPDZH	(Note 5)the time from 50% input to 90% output Refer to Figure 3(c) Guaranteed by design(Note 6)		0.1	0.3	μs
tPDHZ	(Note 5)the time from 50% input to 25% down output Refer to Figure 3(d) Guaranteed by design(Note 6)		0.1	0.3	μs
tPW	Load=20kΩ between OUTA and OUTB, Input puls width=1us,Refer to Figure 3(b) Guaranteed by design (Note 6)	0.7	1.09	1.5	μs
VIH		0.7×VC			V
VIL	VC = 2.7V - 5.5V			0.3×VC	V
IIH	Vterm1 = 3.0V	9	15	21	μΑ
IIL		-1.0			μΑ
tr	VC = 2.7V-5.5V			1.0	μs
tf				1.0	μs
Figure 5)					
VCUV		1.9	2.2	2.5	v
VCUVHY S	Guaranteed by design (Note 6)	0.02	0.05	0.1	V
TTOD	Guaranteed by design	150	175	200	°C
TTSD	(Note 6)	150	175	200	C
	tPDLH tPDHL tPDHZ tPDHZ tPDHZ tPW VIH VIH VII IIH III III tr tf tf tf tf tf tr tf tr tf tr tr	Load=1 k Ω between OUTA and OUTB Refer to Figure 3(a) IN1A=IN2A=L IN1B=IN2B=200kHztPDHL(Note 5)the time from 50% input to 90% output Refer to Figure 3(c) Guaranteed by design(Note 6)tPDZH(Note 5)the time from 50% input to 25% down output Refer to Figure 3(d) Guaranteed by design(Note 6)tPDHZEffer to Figure 3(d) Guaranteed by design(Note 6)tPDHZLoad=20k Ω between OUTA and OUTB, Input puls width=1us,Refer to Figure 3(b) Guaranteed by design (Note 6)VIHVC = 2.7V-5.5VVILIIHVC = 2.7V-5.5VIILVC = 2.7V-5.5VtrVC = 2.7V-5.5VtfFigure 5)VCUVVCUVHYGuaranteed by design (Note 6)	I Load=1 k\Omega between OUTA and OUTB Refer to Figure 3(a) IN1A=IN2A=L IN1B=IN2B=200kHztPDHL(Note 5)the time from 50% input to 90% output Refer to Figure 3(c) Guaranteed by design(Note 6)tPDHZ(Note 5)the time from 50% input to 25% down output Refer to Figure 3(d) Guaranteed by design(Note 6)tPDHZ(Note 5)the time from 50% input to 25% down output Refer to Figure 3(d) Guaranteed by design(Note 6)tPDHZ(Note 5)the time from 50% input to 25% down output Refer to Figure 3(d) Guaranteed by design(Note 6)tPWUOTA and OUTB, Input puls width=1us,Refer to Figure 3(b) Guaranteed by design (Note 6)VIHVC = 2.7V-5.5VVIHVC = 2.7V-5.5VIIHVterm1 = 3.0VIIL-1.0trVC = 2.7V-5.5Vtf.1.9VCUV1.9VCUVHYGuaranteed by design (Note 6)	Load=1 k\Omega between OUTA and OUTB Refer to Figure 3(a) IN1A=IN2A=L IN1B=IN2B=200kHz0.07tPDLH(Note 5)the time from 50% input to 90% output Refer to Figure 3(c) Guaranteed by design(Note 6)0.17tPDHZ(Note 5)the time from 50% input to 25% down output Refer to Figure 3(d) Guaranteed by design(Note 6)0.1tPDHZLoad=20kQ between OUTA and OUTB, Input puls width=lus,Refer to Figure 3(b) Guaranteed by design (Note 6)0.7VIHVC = 2.7V-5.5V0.7×VCVILVC = 2.7V-5.5VIIL-1.0trVC = 2.7V-5.5Vtf.10trVC = 2.7V-5.5VVIL1.92.2VCUVVCUV1.9VCUV1.9VCUV0.020.05	Load=1 kΩ between OUTA and OUTB Refer to Figure 3(a) IN1A=IN2A=L IN1B=IN2B=200kHz 0.07 0.3 tPDHL 0.17 0.3 tPDHZ Refer to Figure 3(c) Guaranteed by design(Note 6) 0.1 0.3 tPDHZ Load=20kΩ between OUTA and OUTB, Input puls width=1us,Refer to Figure 3(b) Guaranteed by design (Note 6) 0.7 1.09 1.5 VIH VC = 2.7V-5.5V 0.7×VC 0.3×VC IIH Vterm1 = 3.0V 9 15 21 IIL VC = 2.7V-5.5V 1.0 1.0 1.0 tr VC = 2.7V-5.5V 1.0 1.0 1.0 tr VC = 2.7V-5.5V 0.02 0.05 0.1

Note 5. $100k\Omega$ load resister is connected between VM and OUTA/B, and also between OUTA/B and GND. Note 6. Not tested in production.

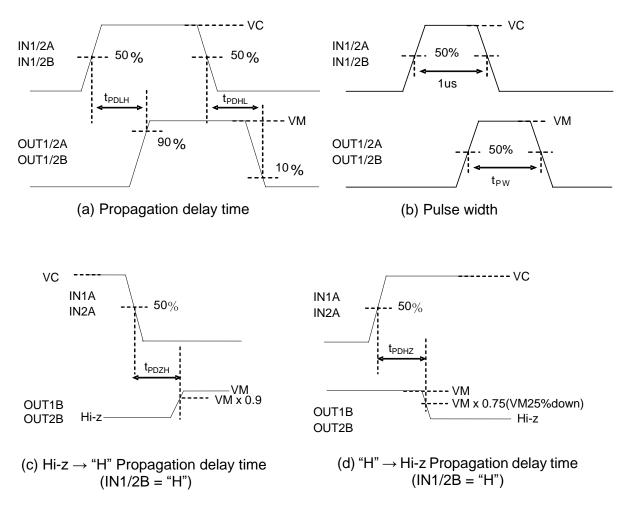


Figure 3. Time chart of propagation delay time and pulse width

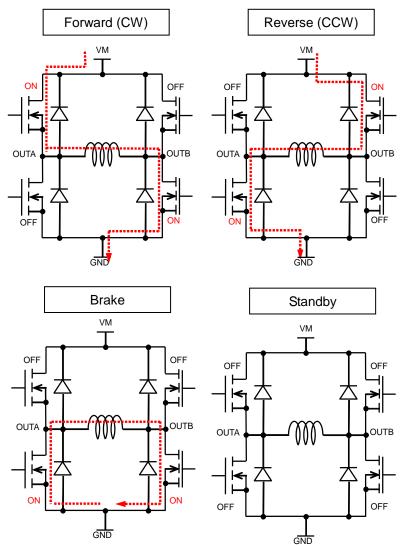
10. Description

The AP1016 is suitable to drive stepper motor and voice coil motor. If the input signals are fed to IN1A, IN1B, IN2A and IN2B, the output signals, OUT1A, OUT1B, OUT2A and OUT2B are defined by table 1. The AP1016 includes Under Voltage Detection and Thermal Shut Down (TSD) circuits. The under voltage detection circuit is monitoring the control voltage (VC), if the VC is less than the specified voltage(UVD), the output of the H-bridge goes to high impedance. The thermal shut down circuit is monitoring the chip temperature. If the temperature of the chip is more than the specified temperature, the output of the H-bridge goes to high impedance. Under voltage detection and thermal shut down circuit has each hysteresis level.

able 1. Control logic truth table (X. doi: t care)								
Protection	n detection	Inj	out	Out	tput	Motion		
UVDN	TSD	IN1A IN2A	IN1B IN2B	OUT1A OUT2A	OUT1B OUT2B	(Note 7)		
Н	L	L	L	L	L	Brake		
Н	L	Н	L	Н	L	Forward (CW)		
Н	L	L	Н	L	Н	Reverse (CCW)		
Н	L	Н	Н					
Н	Н	Х	Х	Hi-Z	Hi-Z	Standby		
L	Х	Х	Х					

Table 1. Control logic truth table (X: don't care)

Note 7. Direction of Current



[AP1016AEN]

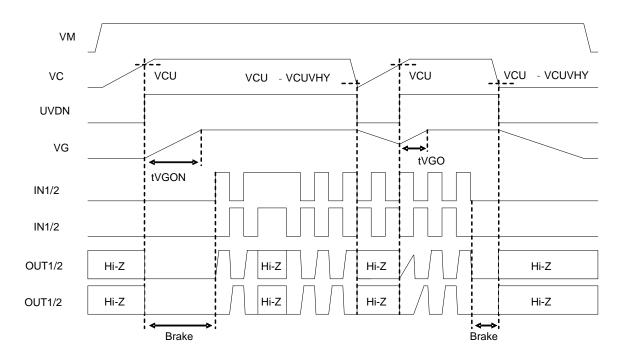


Figure 4. Time chart of input and output (in cace of VDUV detection)

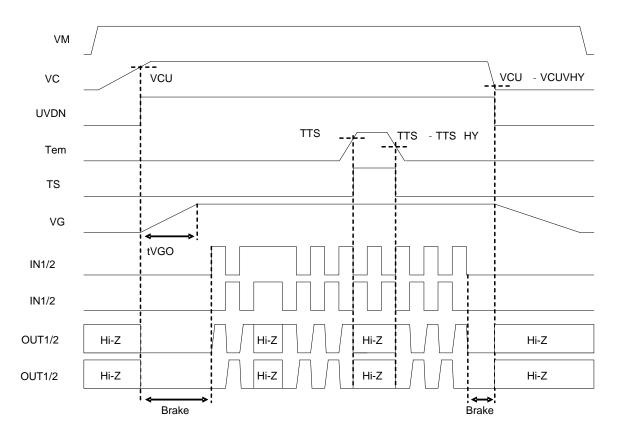


Figure 5. Time chart of input and output (in cace of TSD detection)

11. Recommended External Circuits

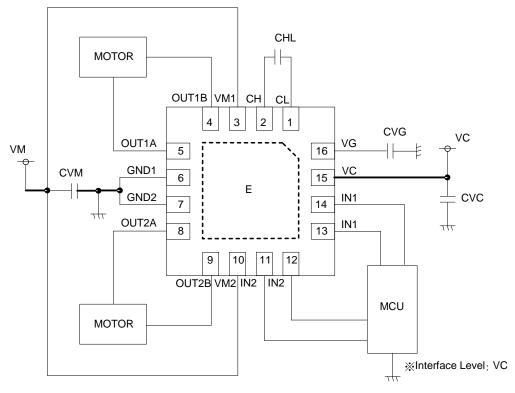


Figure 6. Recommended External Circuits (Top view)

Table 2. Recommended external	components example

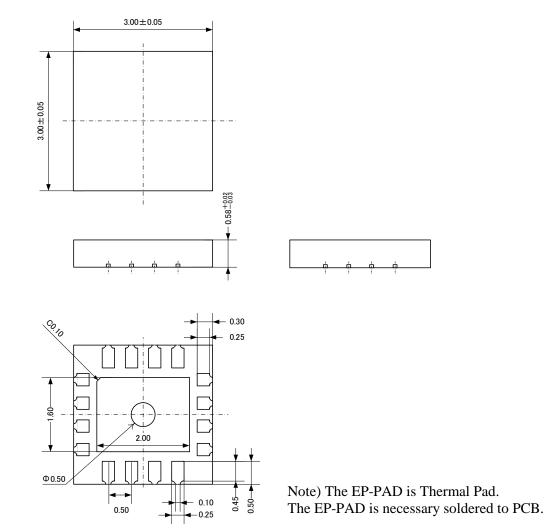
Parameter	Symbol	min	typ	max	Unit	Condition
Motor driver power supply connection decupling capacitor	CVM	-	1	-	μF	(Note 8)
Control power supply connection bypass capacitor	CVC	-	0.1	-	μF	(Note 8)
Charge pump capacitance1	CVG	0.047	0.1	0.22	μF	
Charge pump capacitance2	CHL	0.047	0.1	0.22	μF	

Note 8. Please adjust the connecting capacitor of CVM and CVC depending on the load current profile, the load capacitance, the line resistance and etc. with each application boards.

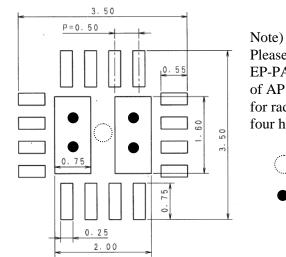
12. Package

Outline Dimensions

(Unit: mm)



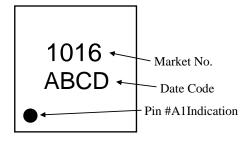
Recommended foot pattern



Please layout the foot pattern of EP-PAD not to surround the steam via of AP1016. Please locate thermal via for radiation improvement more than four halls.

- : example of steam via
- : example of thermal via

Marking



YWWA: Date code (4 digit) A: Manage number WW: Producing week Y: Producing year (Ex: 2013 → "3")

13. Revise History

Date (YY/MM/DD)	Revision	Page	Contents
14/01/31	00		First edition
14/08/07	01	7	Propagation delay time (Hi-z \rightarrow "H", "H" \rightarrow Hi-z)Condition "the time from 50% to 75% output" \rightarrow "the time from 50% input to 90% output" "the time from 75% to 50% output" \rightarrow "the time from 50% input to 90% output"
		8	 "the time from 50% input to 90% output" Propagation delay time ("H"→Hi-Z) typ 0.15µs → typ 0.1µs Figure 3 Time chart of propagation Hi-z → "H" and "H"→Hi-z were added.
14/10/09	02	9	Figure of direction of current was corrected.
14/12/24	03	3	Correct temperature range in ordering guide

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