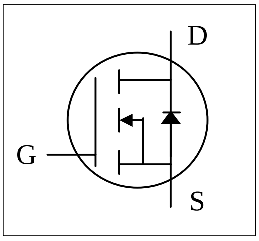
AP10NA034YT

Halogen-Free Product

Advanced Power Electronics Corp.

N-CHANNEL ENHANCEMENT MODE POWER MOSFET

- ▼ **Simple Drive Requirement**
- ▼ **Small Size & Lower Profile**
- ▼ **RoHS Compliant & Halogen-Free**

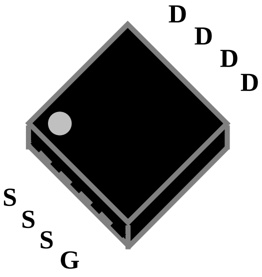


BV_{DSS}	100V
$R_{DS(ON)}$	34mΩ

Description

AP10NA034 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK® 3x3 package is special for voltage conversion application using standard infrared reflow technique with the backside heat sink to achieve the good thermal performance.



PMPAK® 3 x 3

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V	18	A
I_D@T_A=25℃	Drain Current, V_{GS} @ 10V[3]	7	A
I_D@T_A=70℃	Drain Current, V_{GS} @ 10V[3]	5.6	A
I_{DM}	Pulsed Drain Current[1]	30	A
P_D@T_A=25℃	Total Power Dissipation	3.12	W
E_{AS}	Single Pulse Avalanche Energy[5]	24.5	mJ
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	6	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	40	℃/W

Electrical Characteristics@T_j=25^{o}C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	100	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=6A	-	-	34	mΩ
		V_{GS}=6V, I_D=3A	-	-	56	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	2	-	4	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=6A	-	12	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=80V, V_{GS}=0V	-	-	25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}= ±20V, V_{DS}=0V	-	-	±0.1	uA
Q_g	Total Gate Charge[4]	I_D=6A	-	12	19.2	nC
Q_{gs}	Gate-Source Charge[4]	V_{DS}=50V	-	3	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge[4]	V_{GS}=10V	-	4.5	-	nC
$t_{d(on)}$	Turn-on Delay Time[4]	V_{DS}=50V	-	8	-	ns
t_r	Rise Time[4]	I_D=1A	-	7	-	ns
$t_{d(off)}$	Turn-off Delay Time[4]	R_G=3.3Ω	-	17	-	ns
t_f	Fall Time[4]	V_{GS}=10V	-	30	-	ns
C_{iss}	Input Capacitance[4]	V_{GS}=0V	-	480	768	pF
C_{oss}	Output Capacitance[4]	V_{DS}=80V	-	77	-	pF
C_{rss}	Reverse Transfer Capacitance[4]	f=1.0MHz	-	10	-	pF
R_g	Gate Resistance	f=1.0MHz	-	0.8	1.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=2.4A, V_{GS}=0V	-	-	1.3	V
t_{rr}	Reverse Recovery Time[4]	I_S=6A, V_{GS}=0V,	-	35	-	ns
Q_{rr}	Reverse Recovery Charge[4]	dI/dt=100A/µs	-	33	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 2oz copper pad of FR4 board, t ≤10sec, 210^{o}C/W when mounted on min. copper pad.

4.Guaranteed by design.

5.Starting T_j=25^{o}C , V_{DD}=50V , L=1mH , R_G=25Ω

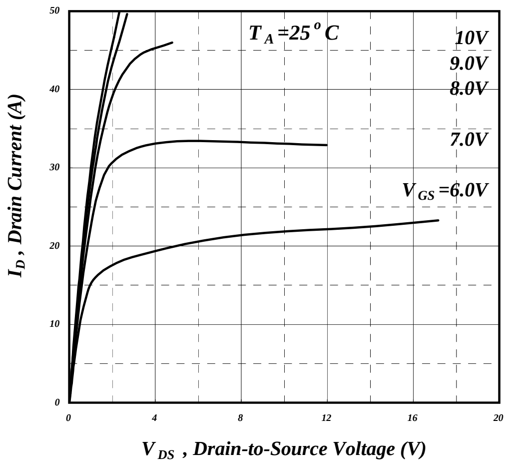


Fig 1. Typical Output Characteristics

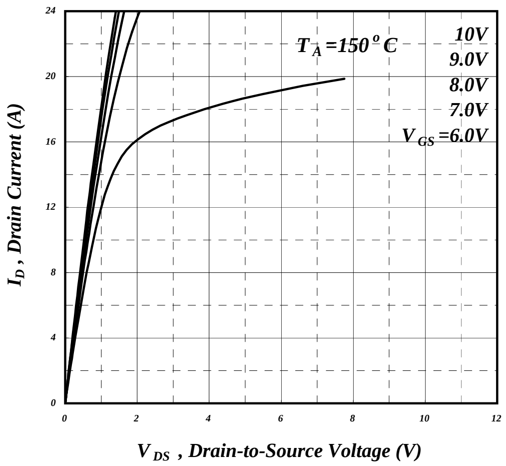


Fig 2. Typical Output Characteristics

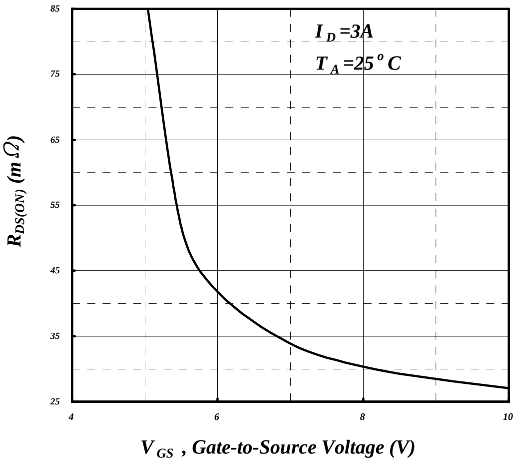


Fig 3. On-Resistance v.s. Gate Voltage

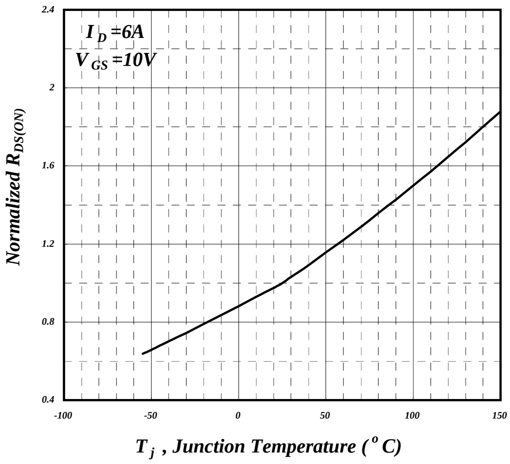


Fig 4. Normalized On-Resistance v.s. Junction Temperature

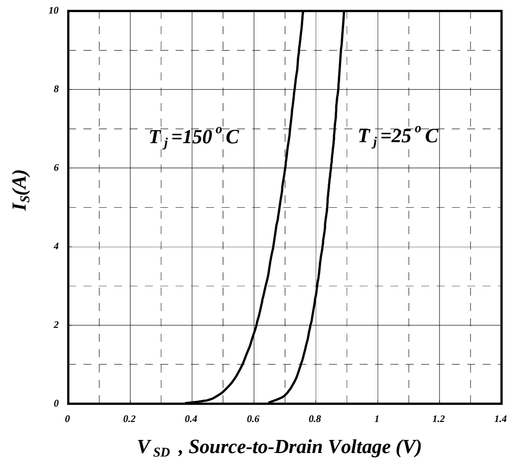


Fig 5. Forward Characteristic of Reverse Diode

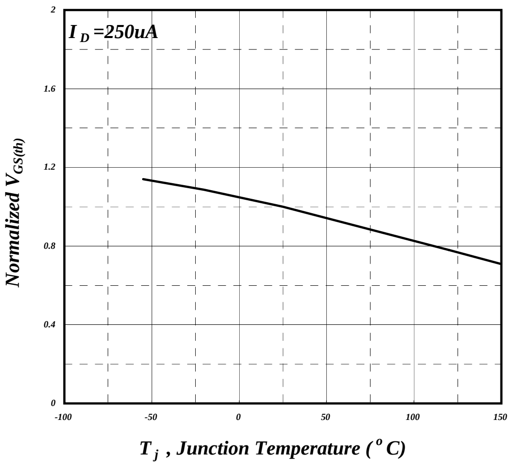


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

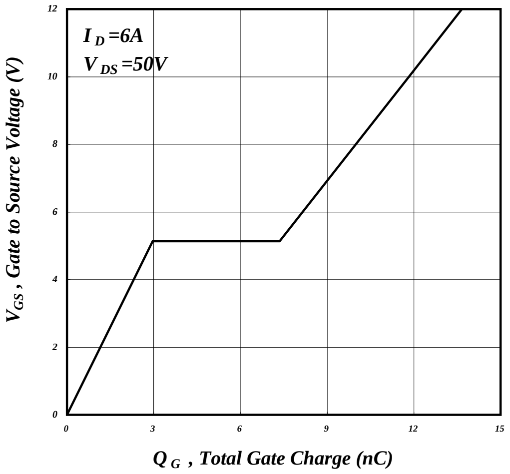


Fig 7. Gate Charge Characteristics

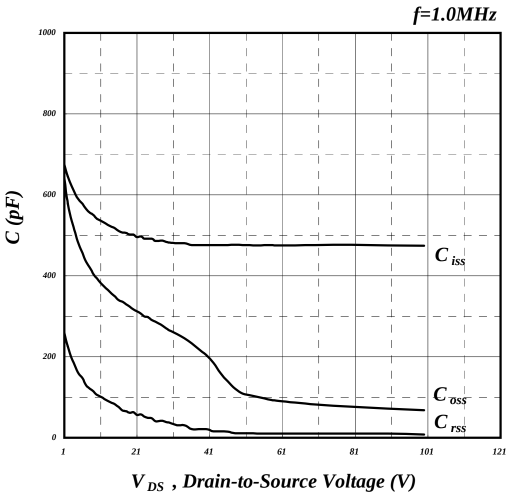


Fig 8. Typical Capacitance Characteristics

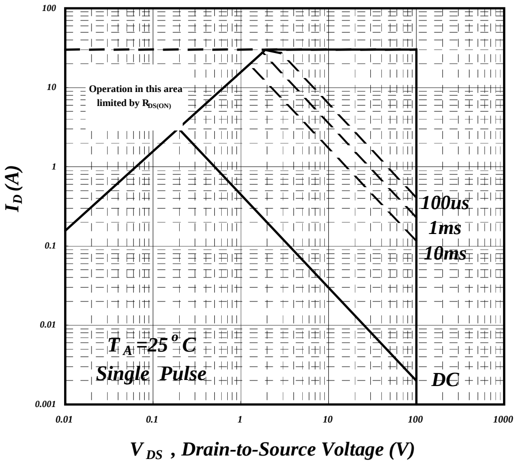


Fig 9. Maximum Safe Operating Area

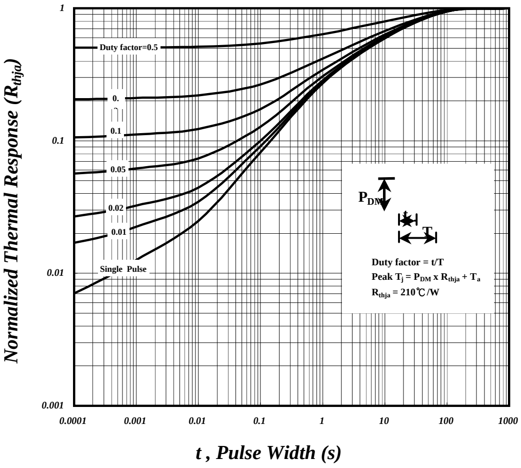


Fig 10. Effective Transient Thermal Impedance

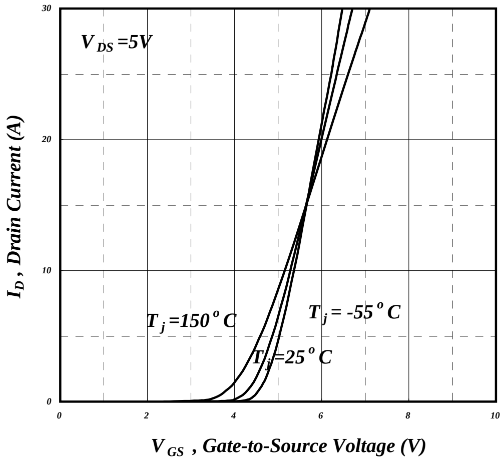


Fig 11. Transfer Characteristics

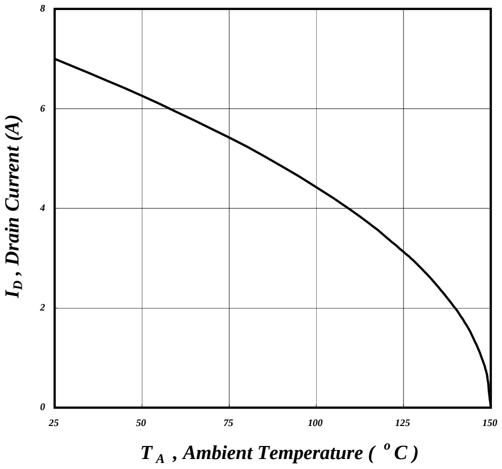


Fig 12. Drain Current v.s. Ambient Temperature

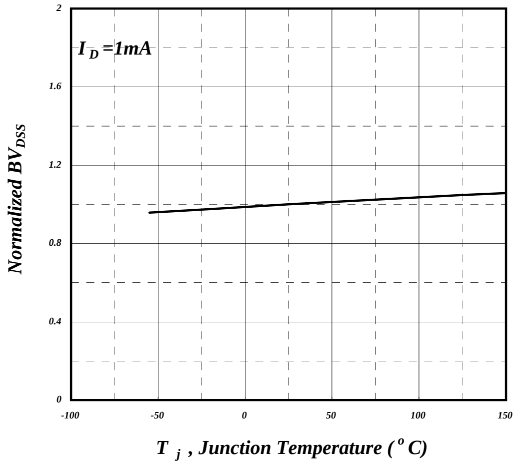


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

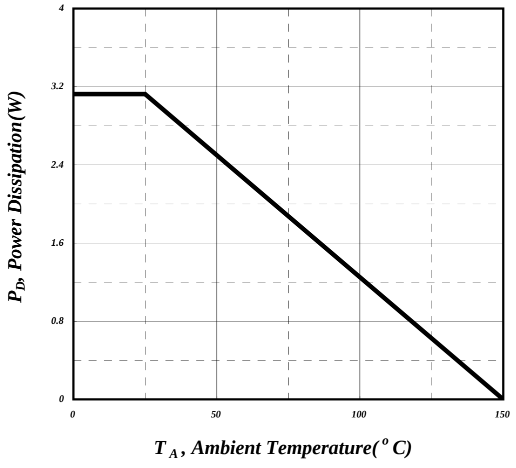


Fig 14. Total Power Dissipation

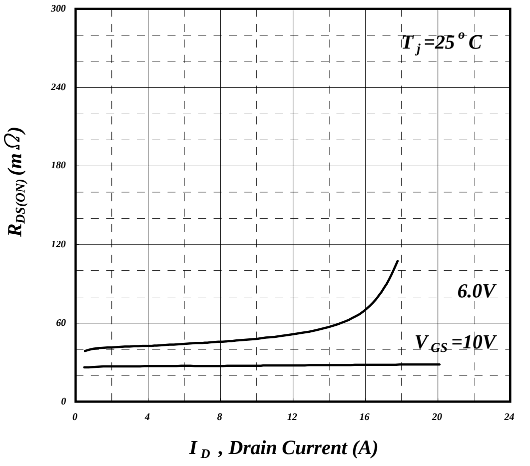
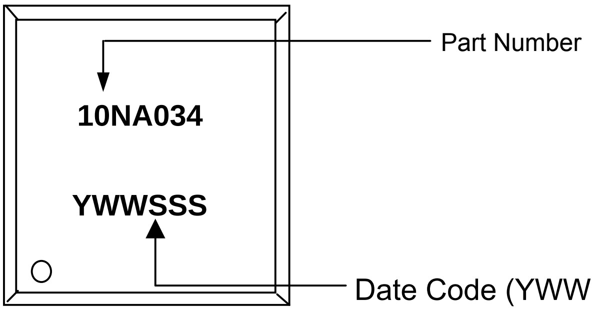


Fig 15. Typ. Drain-Source on State Resistance

MARKING INFORMATION



Date Code (YWWSSS)

Y：Last Digit Of The Year
WW：Week
SSS：Sequence