AP1151

200mA Output,High PSRR,Low Noise LDO Regulator Adjustable Output Voltage Type

1. General Description

The AP1151 is a low dropout linear regulator with On/Off control, which can supply 200mA load current. The output voltage can be set between 1.3 to 13.5V by an external resistor, and the output capacitor is available to use a small 0.22uF ceramic capacitor.
The AP1151 has a built-in over-current protection and thermal shutdown protection circuit, and is possible to provide two types of package, the AP1151ADS is the SOT23-5 package and the AP1151AEU is the PLP1822-6 package with Heat Sink pad.

2. Features

- Operating Temperature Range -40 to 85℃
- Operating Voltage Range 2.1 to 14.0V
- Output Current 200mA
- Settable range of output voltage 1.3 to 13.5V
- Reference voltage accuracy 1.27V ± 20mV
- Dropout Voltage 120mV at I_{OUT}=100mA
- Ripple Rejection 80dB at 1kHz
- Available very low noise application
- Available to use a small ceramic capacitor
- On/Off control (High active)
- Built-in Short circuit protection, thermal shutdown
- Package AP1151ADS : SOT23-6
  AP1151AEU : PLP1822-6 (with Ex-posed Pad)

3. Applications

- RF Power Supplies — PLL, VCO, Mixer, LNA
- Low Noise Image Sensor Unit — Digital Still Camera
- High Speed/High Precision A-D, D-A, Amplifier — Audio Equipment, Medical Equipment, Instrumentation
- Precision Power Supplies
- Post Regulator for Switching Supplies — Car Infotainment

4. Table of Contents

5. Block Diagram

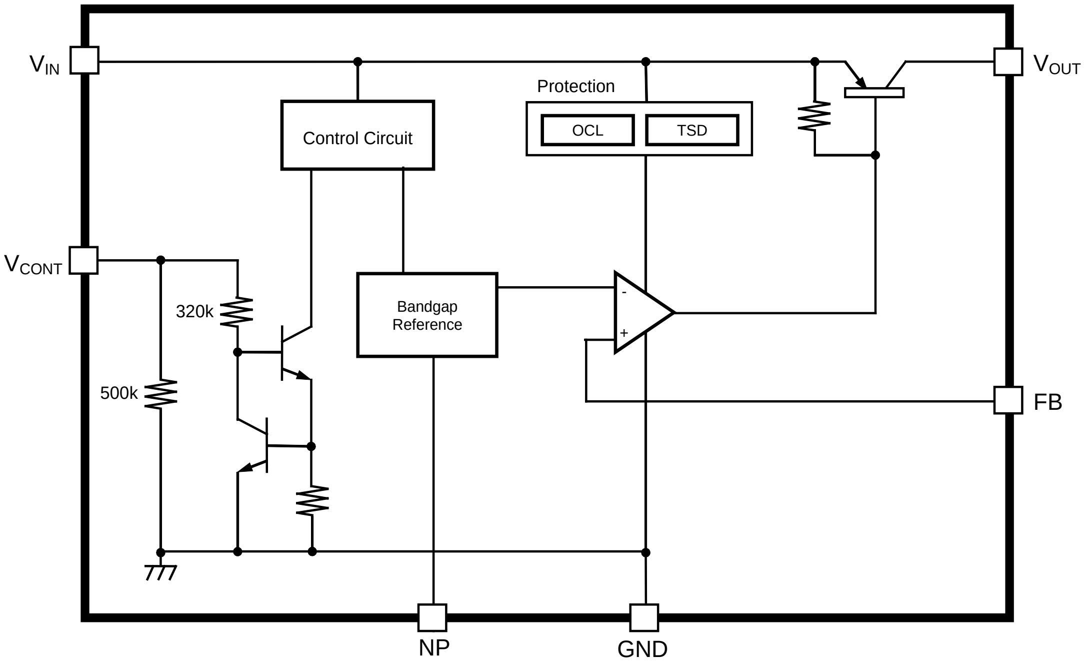


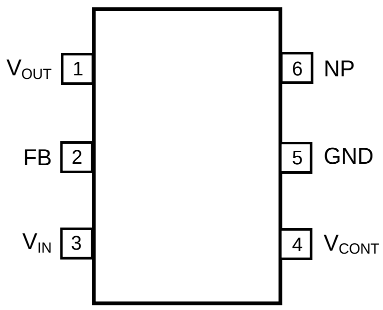
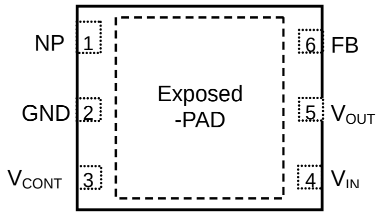
Figure 1. Block Diagram

6. Ordering Guide

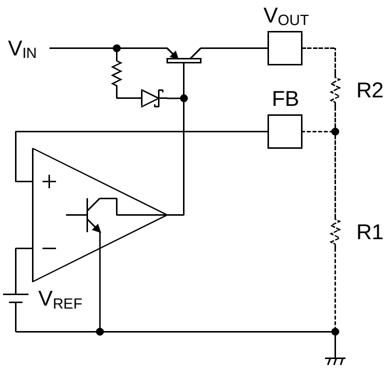
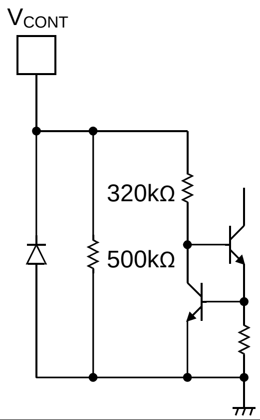
AP1151ADS	Ta = -40 to 85°C	SOT23-6
AP1151AEU	Ta = -40 to 85°C	PLP1822-6

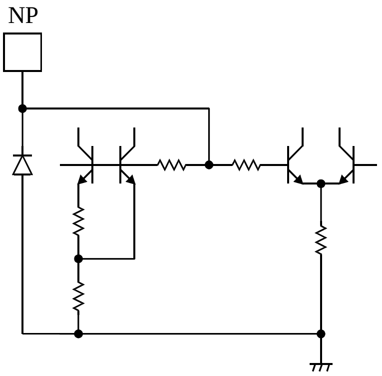
7. Pin Configuration and Functions

■ Pin Configurations

SOT23-6	PLP1822-6
 (Top View)	 (Top View)

■ Functions

Pin No.		Pin Description	Internal Equivalent Circuit	Description
SOT23 -6	PLP1822 -6			
1	5	V_{OUT}		Output Terminal The output voltage is decided by the following formulas. $V_{OUT} = V_{FB} \times \frac{R1+R2}{R1}$
2	6	FB		Feedback Terminal Connect a resistance R1 between GND, and a resistance R2 between V_{OUT}.
3	4	V_{IN}		Input Terminal
4	3	V_{CONT}		On/Off Control Terminal V_{CONT} > 1.8V : ON V_{CONT} < 0.35V : OFF The pull-down resister (500kΩ) is built-in.
5	2	GND		Ground Terminal

Pin No.		Pin Description	Internal Equivalent Circuit	Description
SOT23-6	PLP1822-6			
6	1	NP		Noise Bypass Terminal Connect a bypass capacitor between GND.
-	Exposed Pad	-		Ground Terminal Heat dissipation pad Exposed Pad must be connected to GND.

8. Absolute Maximum Ratings

Parameter		Symbol	min	max	Unit	Condition
Supply Voltage		$V_{CC(MAX)}$	-0.4	16	V	
Reverse Bias Voltage		$V_{REV(MAX)}$	-0.4	6	V	$V_{OUT(TYP)} \leqq 2.0V$
			-0.4	14.5	V	$2.0V \leqq V_{OUT(TYP)}$
FB Terminal Voltage		$V_{FB(MAX)}$	-0.4	5	V	
NP Terminal Voltage		$V_{NP(MAX)}$	-0.4	5	V	
V_{CONT} Terminal Voltage		$V_{CONT(MAX)}$	-0.4	16	V	
Junction Temperature		Tj	-	150	°C	
Storage Temperature Range		T_{STG}	-55	150	°C	
Power Dissipation	SOT23-6	P_D	-	500	mW	(Note 1)
	PLP1822-6			1500	mW	(Note 1)

Note 1. A 4-layer JEDEC51-3 compliant board is used.
If the temperature exceeds 25°C, be sure to derate at Figure 2.
SOT23-6 : θ_{JA} =250°C /W (A 2-layer board is used.)
PLP1822-6 : θ_{JA} =83°C /W (A 4-layer JEDEC51-3 compliant board is used.)

WARNING: The maximum ratings are the absolute limitation values with the possibility of the IC breakage. When the operation exceeds this standard quality cannot be guaranteed.

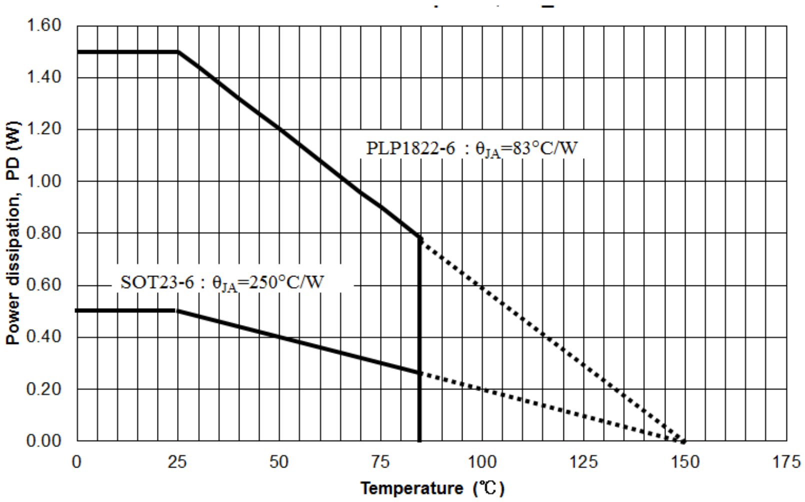


Figure 2. Maximum Power Dissipation

9. Recommended Operating Conditions

Parameter	Symbol	min	typ	max	Unit	Condition
Operating Temperature Range	Ta	-40	-	85	°C	
Operating Voltage Range	V_{OP}	2.1	-	14	V	
Output Voltage Range	V_{OUT}	1.3	-	13.5	V	

10. Electrical Characterisics

■ Electrical Characteristics of Ta=Tj=25°C

The parameters with min or max values will be guaranteed at Ta=Tj=25°C.

(V_{IN}=4.0V, R1=51kΩ, R2=68kΩ, V_{CONT}=1.8V, Ta=Tj=25°C, unless otherwise specified.)

Parameter	Symbol	Condition	min	typ	max	Unit
FB Terminal Voltage	V_{FB}	I_{OUT}=5mA	1.250	1.270	1.290	V
Line Regulation	LinReg	ΔV_{IN}=5V	-	0.0	5.0	mV
Load Regulation (Note 2)	LoaReg	I_{OUT}=5mA~100mA	-	11	27	mV
		I_{OUT}=5mA~200mA	-	26	61	mV
Dropout Voltage	V_{DROP}	I_{OUT}=50mA	-	80	140	mV
		I_{OUT}=100mA	-	120	210	mV
		I_{OUT}=200mA	-	200	350	mV
Maximum Output Current (Note 3)	$I_{OUT(MAX)}$	When V_{OUT} drops 0.3V	240	320	-	mA
Quiescent Current	I_Q	I_{OUT}=0mA	-	78	125	μA
Standby Current	$I_{STANDBY}$	V_{CONT}=0V	-	0.0	0.1	μA
Ground Terminal Current	I_{GND}	I_{OUT}=50mA	-	1.0	1.8	mA
Control Terminal (VCONT)						
VCONT Terminal Current	I_{CONT}	V_{CONT}=1.8V	-	5.0	15.0	μA
VCONT Terminal Voltage	V_{CONT}	V_{OUT} ON state	1.8	-	-	V
		V_{OUT} OFF state	-	-	0.35	V
Reference Value						
NP Terminal Voltage	V_{NP}		-	1.27	-	V
Output Voltage / Temp.	Vo/Ta		-	35	-	ppm /°C
Short Circuit Current	I_{SHORT}		-	360	-	mA
Output Noise Voltage	V_{NOISE}	C_L=1.0μF, C_{NP}=0.01μF C_{FB}=100pF, I_{OUT}=30mA	-	34	-	μVrms
Ripple Rejection	R.R	C_L=1.0μF, C_{NP}=0.01μF C_{FB}=100pF, I_{OUT}=10mA f=1kHz	-	80	-	dB
Rise Time	tr	C_L=1.0μF, C_{NP}=0.001μF C_{FB}=100pF V_{CONT} : Pulse Wave (100Hz) V_{CONT} ON → V_{OUT}×95% point	-	40	-	μs

Note 2. Load Regulation changes with output voltage. The value mentioned above is guaranteed with the condition at R1=51kΩ, R2=68kΩ (set at $V_{OUT(TYP)}$=3.0V).

Note 3. The maximum output current is limited by power dissipation.

■ Electrical Characteristics of Ta=-40°C to 85°C

The parameters with min or max values will be guaranteed at Ta=-40°C to 85°C.

(V_{IN}=4.0V, R1=51kΩ, R2=68kΩ,V_{CONT}=1.8V,Ta= -40 ~ 85°C, unless otherwise specified.)

Parameter	Symbol	Condition	min	typ	max	Unit
FB pin Voltage	V_{FB}	I_{OUT}=5mA	1.240	1.270	1.300	V
Line Regulation	LinReg	ΔV_{IN}=5V	-	0.0	8.0	mV
Load Regulation (Note 4)	LoaReg	I_{OUT}=5mA~100mA	-	11	50	mV
		I_{OUT}=5mA~200mA	-	26	80	mV
Dropout Voltage	V_{DROP}	I_{OUT}=50mA	-	80	180	mV
		I_{OUT}=100mA	-	120	270	mV
		I_{OUT}=200mA	-	200	390	mV
Maximum Output Current (Note 5)	$I_{OUT(MAX)}$	When V_{OUT} drops 0.3V	220	320	-	mA
Quiescent Current	I_Q	I_{OUT}=0mA	-	78	150	μA
Standby Current	$I_{STANDBY}$	V_{CONT}=0V	-	0.0	0.5	μA
GND Pin Current	I_{GND}	I_{OUT}=50mA	-	1.0	2.2	mA
Control Terminal (VCONT)						
VCONT Terminal Current	I_{CONT}	VCONT=1.8V	-	5.0	15.0	μA
VCONT Terminal Voltage	V_{CONT}	VOUT ON state	1.8	-	-	V
		VOUT OFF state	-	-	0.35	V
Reference Value						
NP Terminal Voltage	V_{NP}		-	1.27	-	V
Output Voltage / Temp.	V_O/Ta		-	35	-	ppm /°C
Short Circuit Current	I_{SHORT}		-	360	-	mA
Output Noise Voltage	V_{NOISE}	C_L=1.0μF, C_{NP}=0.01μF C_{FB}=100pF, I_{OUT}=30mA	-	34	-	μVrms
Ripple Rejection	R.R	C_L=1.0μF, C_{NP}=0.01μF C_{FB}=100pF, I_{OUT}=10mA f=1kHz	-	80	-	dB
Rise Time	tr	C_L=1.0μF, C_{NP}=0.001μF C_{FB}=100pF V_{CONT} : Pulse Wave (100Hz) V_{CONT} ON → V_{OUT}×95% point	-	40	-	μs

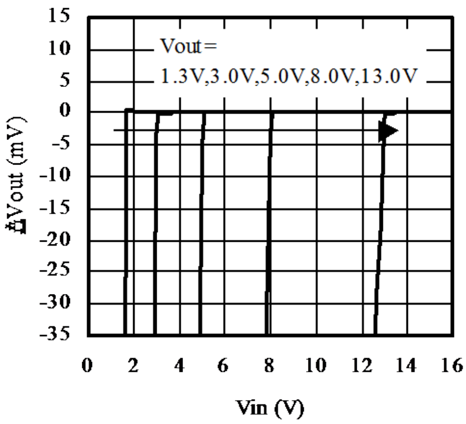
Note 4. Load Regulation changes with output voltage. The value mentioned above is guaranteed with the condition at R1=51kΩ, R2=68kΩ (set at $V_{OUT(TYP)}$=3.0V).

Note 5. The maximum output current is limited by power dissipation.

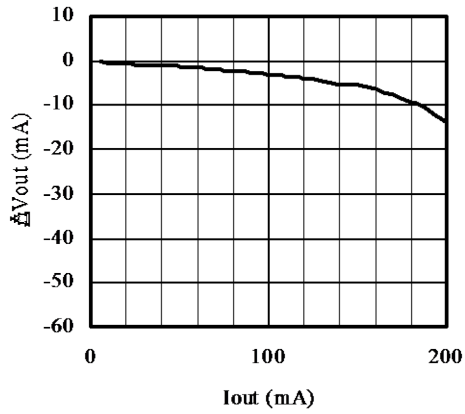
11. Description

11.1 DC Characteristics

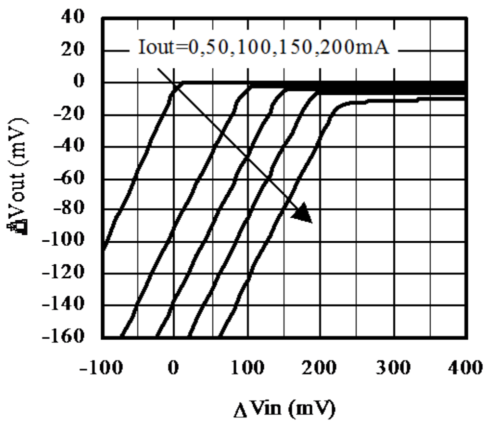
■ Line Regulation



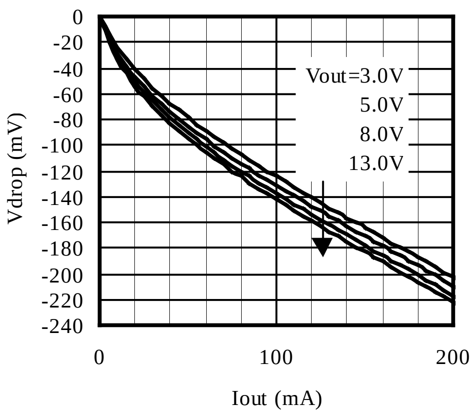
■ Load Regulation ($V_{OUT(TYP)}$ =3.0V)



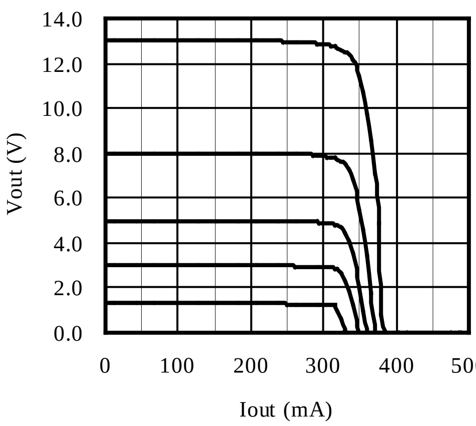
■ Regulation Point (2.1V ≤ $V_{OUT(typ)}$)



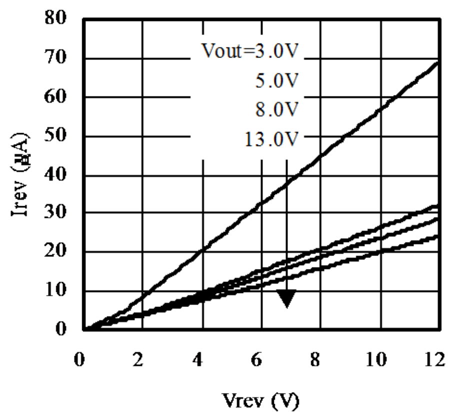
■ Dropout Voltage vs Output Current



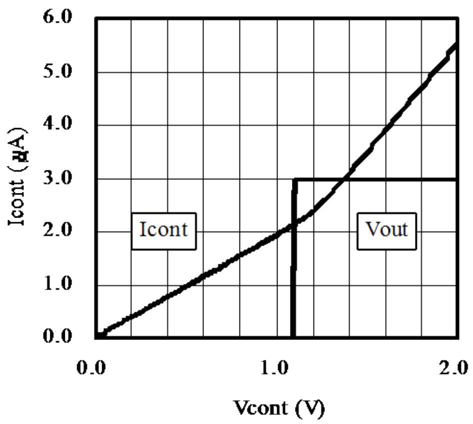
■ Output Short-Circuit Current



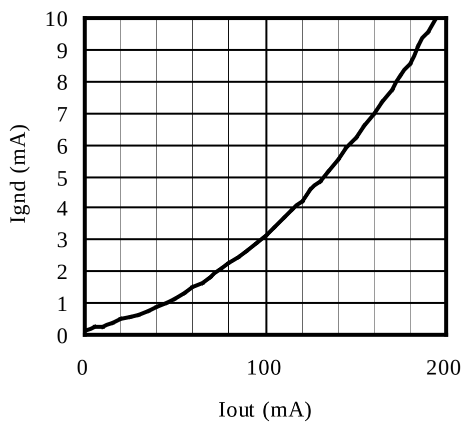
■ Reverse Bias Current



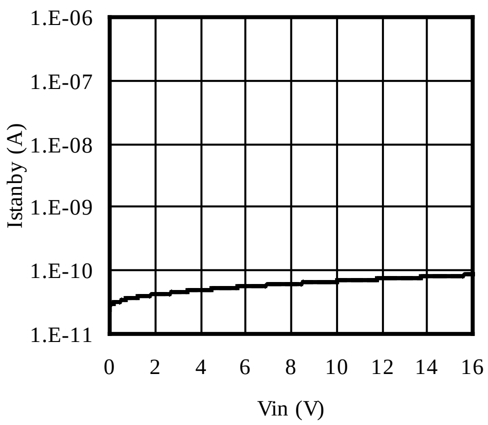
■ CONT Terminal Current and On/Off Point



■ Quiescent Current vs Output Current

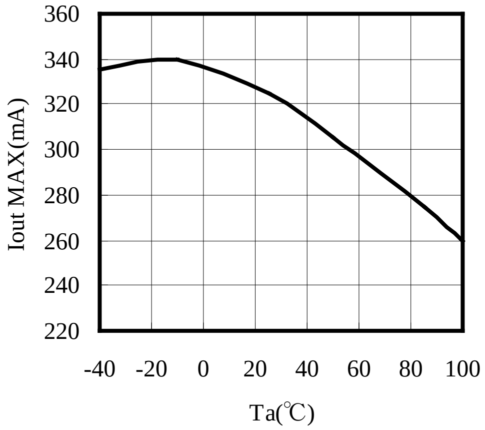


■ Standby Current ($V_{CONT=}$0V)

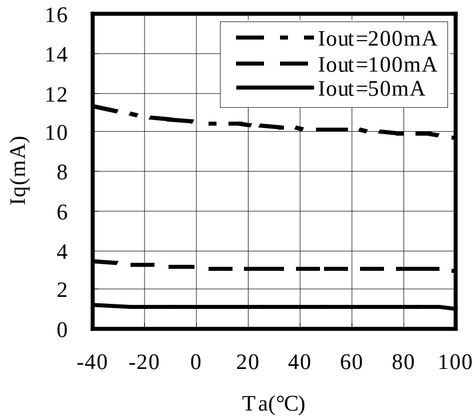


11.2 DC Temperature Characteristics

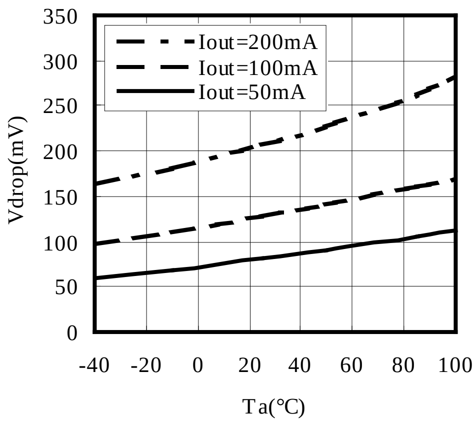
■ Maximum Output Current



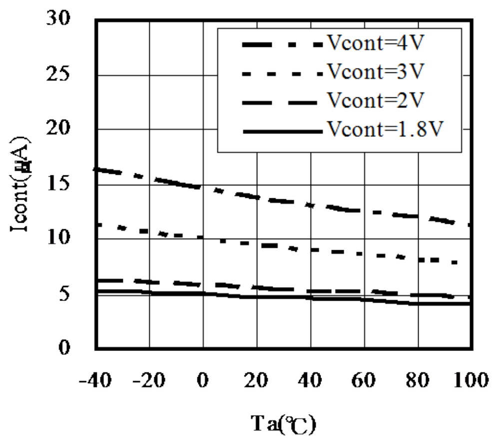
■ Quiescent Current



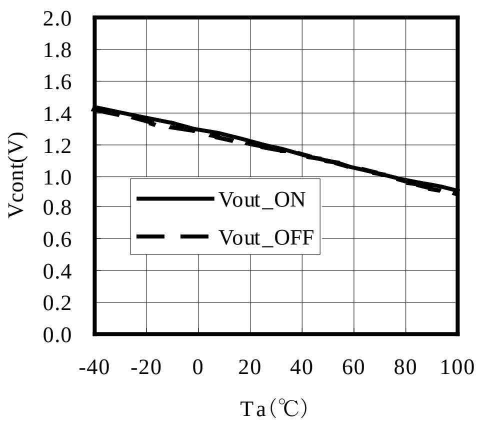
■ Dropout Voltage



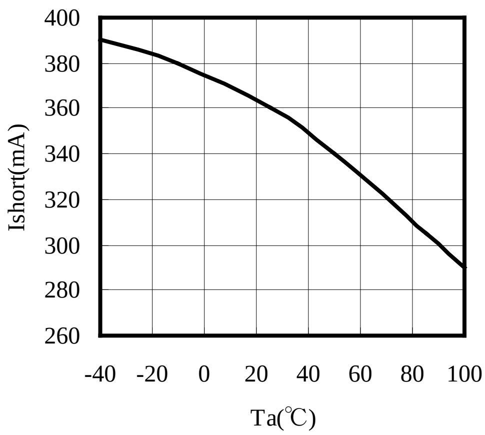
■ CONT Terminal Current



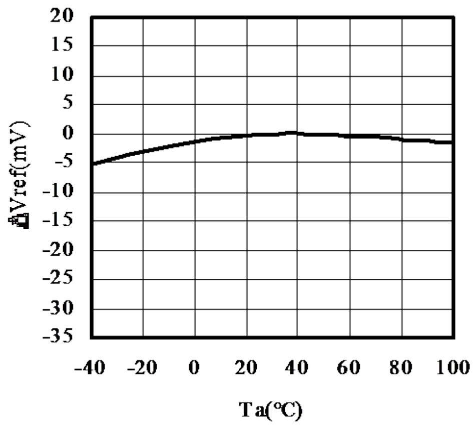
■ CONT Terminal On/Off point



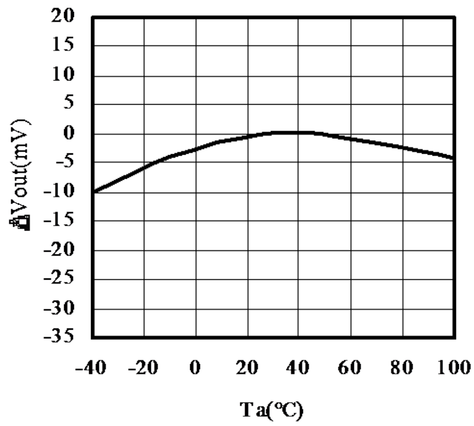
■ Short Circuit Current



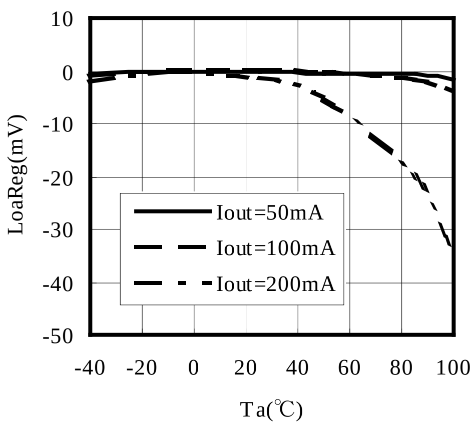
■ V_{REF} ($V_{REF(TYP)}$=1.27V)



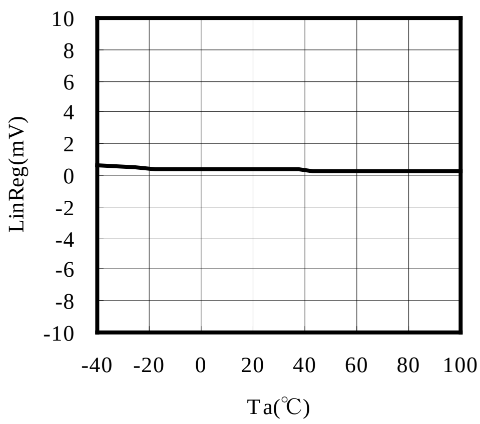
■ V_{OUT} ($V_{OUT(TYP)}$=3.0V)



■ Line Regulation ($V_{OUT(TYP)}$=3.0V, Ta=Tj)



■ Load Regulation

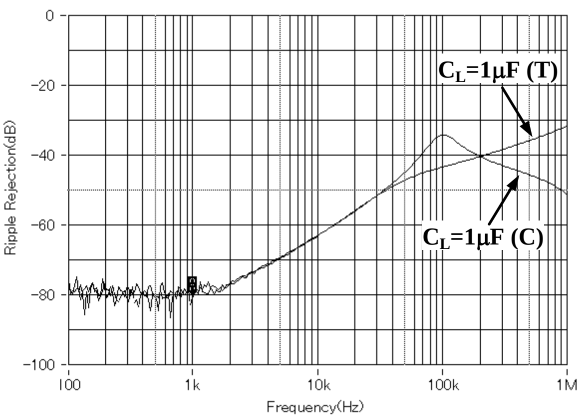


11.3 AC Characteristics

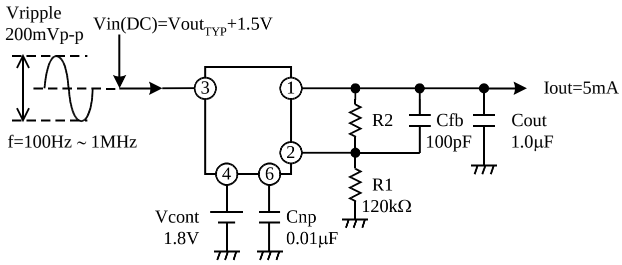
・Ripple Rejection

The ripple rejection characteristic depends on the characteristic and the capacity value of the capacitor connected with the output side. The ripple rejection characteristic of 50kHz or more changes greatly in the capacitor on the output side and PCB pattern. Please confirm stability if necessary while operated.

■ C_L=1.0μF : Ceramic (C), Tantalum (T)

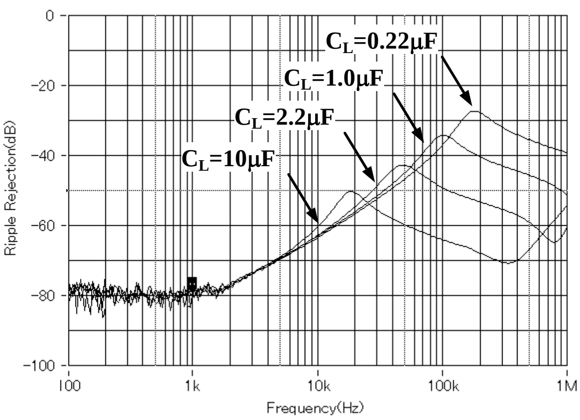


■ Test conditions

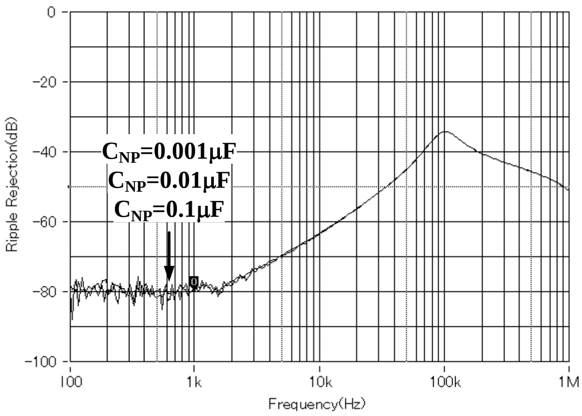


$V_{OUT(TYP)}$=3.0V : R2=163.5kΩ

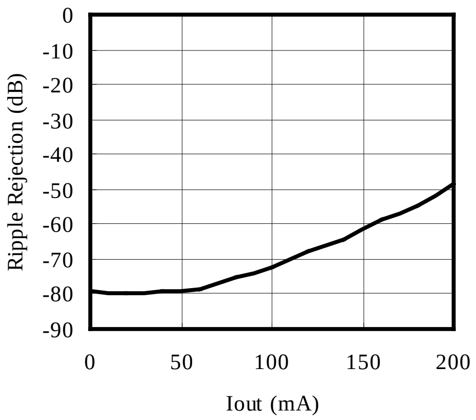
■ C_L==0.22μF, 1.0μF, 2.2μF, 10μF : Ceramic



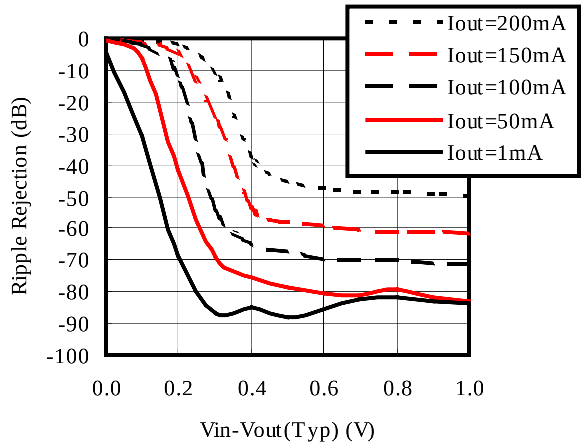
■ C_{NP}=0.001μF, 0.01μF, 0.1μF



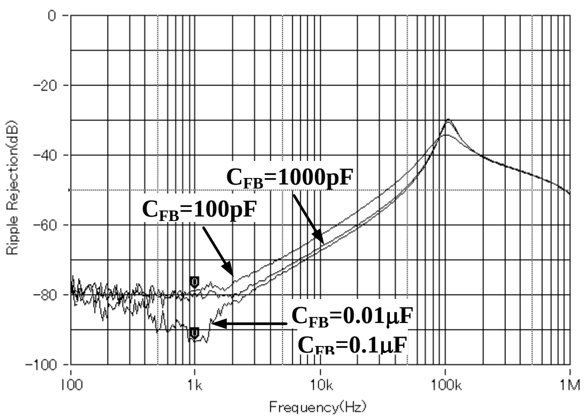
■ R.R vs I_{OUT} : Frequency=1kHz



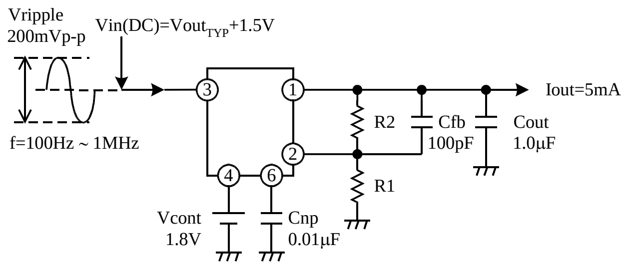
■ R.R vs Low V_{IN}: Frequency=1kHz



■ C_{FB} = 100pF, 1000pF, 0.01μF, 0.1μF
$V_{OUT(TYP)}$ =1.3V

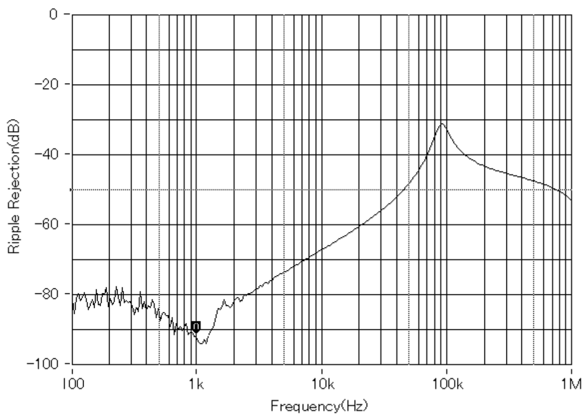


■ Test conditions

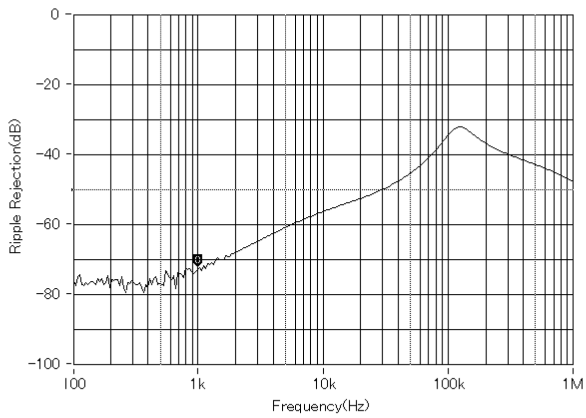


$V_{OUT(TYP)}$ =1.3V: R1=120kΩ, R2=2.8kΩ
3.0V: R1=120kΩ, R2=163.5kΩ
5.0V: R1=120kΩ, R2=352kΩ
8.0V: R1=75kΩ, R2=397kΩ
13.0V: R1=51kΩ, R2=470kΩ

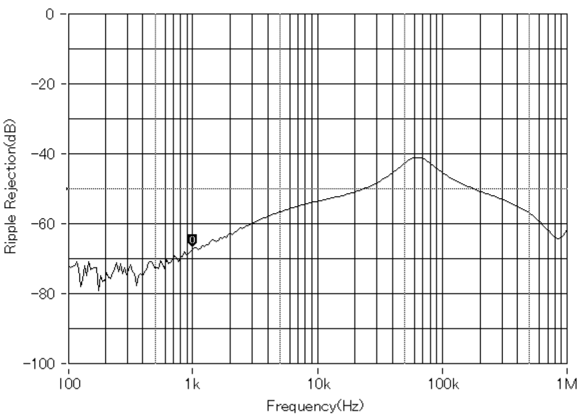
■ $V_{OUT(TYP)}$ =1.3V



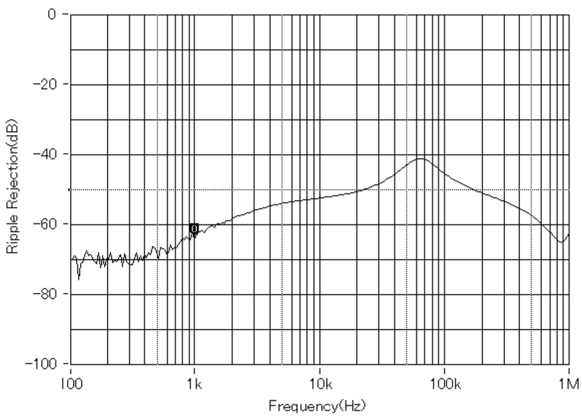
■ $V_{OUT(TYP)}$ =5.0V



■ $V_{OUT(TYP)}$ =8.0V



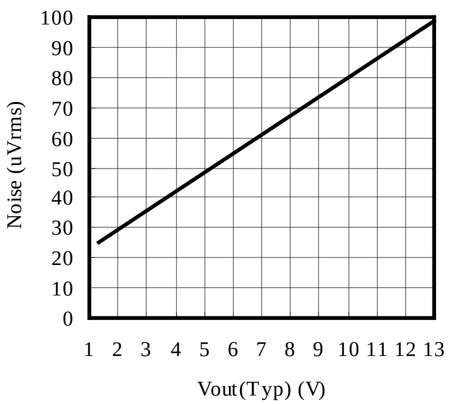
■ $V_{OUT(TYP)}$ =13V



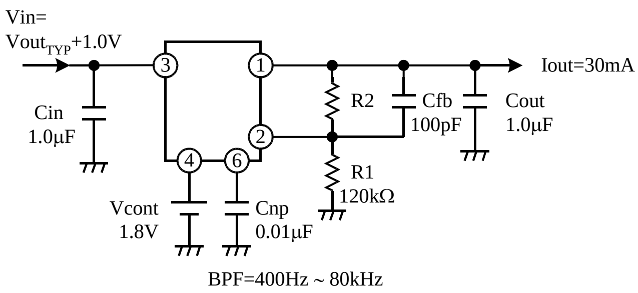
・**Output Noise**

It is more effective if it increases the CNP than to increase the CL is the case that require low noise. CNP capacity is recommended 0.01μF to 0.1μF. Amount of noise will be a lot higher output voltage products.

■ V_{OUT} vs Noise
R1=51kΩ, R2=1.2kΩ ~ 470kΩ

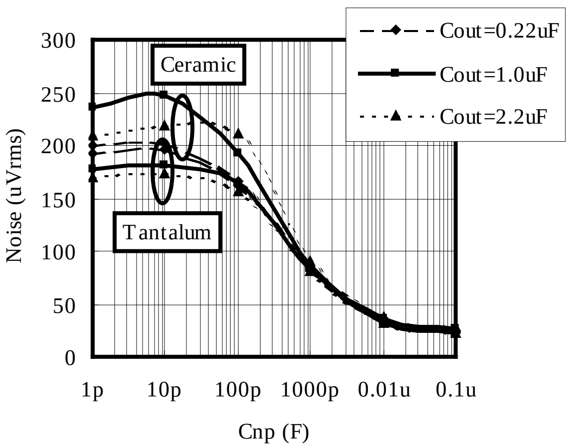


■Test conditions

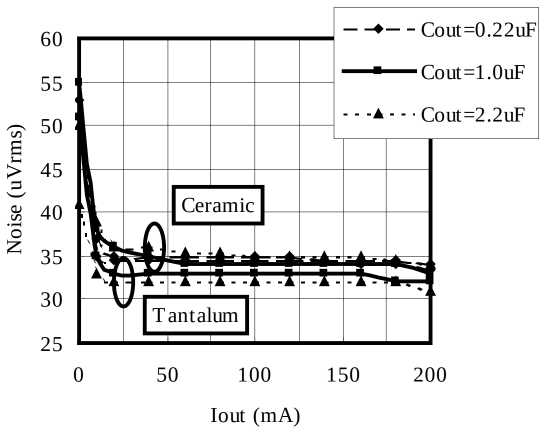


$V_{OUT(TYP)}$ =3.0V : R2=163.5kΩ

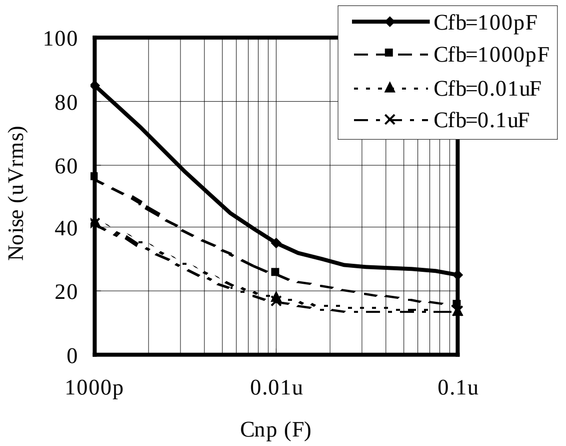
■ C_{NP} vs Noise



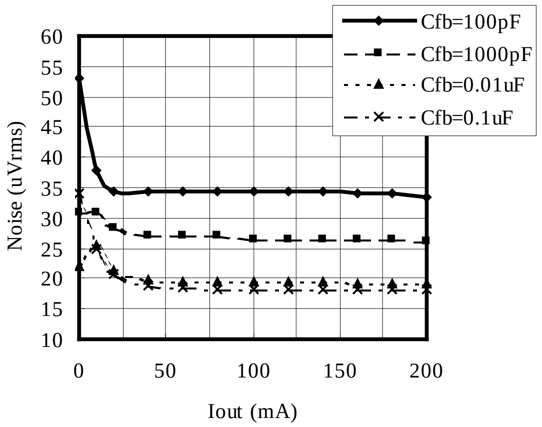
■ I_{OUT} vs Noise



■ C_{NP} vs Noise (C_L: Ceramic)
C_{FB}=100pF, 1000pF, 0.01μF, 0.1μF

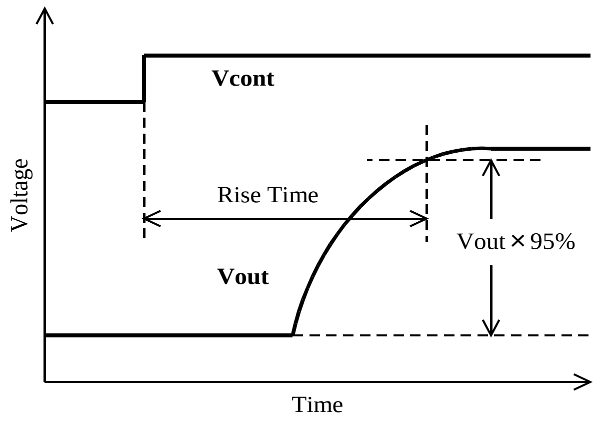


■ I_{OUT} vs Noise (C_L: Ceramic)
C_{FB}=100pF, 1000pF, 0.01μF, 0.1μF

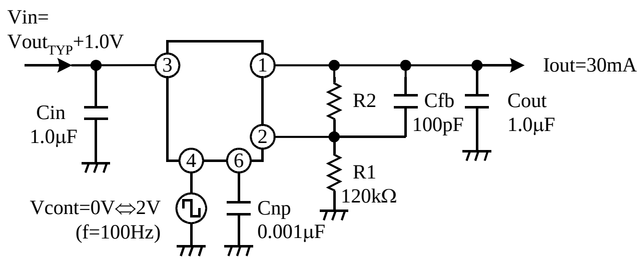


・On/Off Transient

The rise time of the IC will be slow and C_L, C_{NP} is large. Rise time is dependent C_L, on the C_{NP}, fall time is dependent on the C_L.

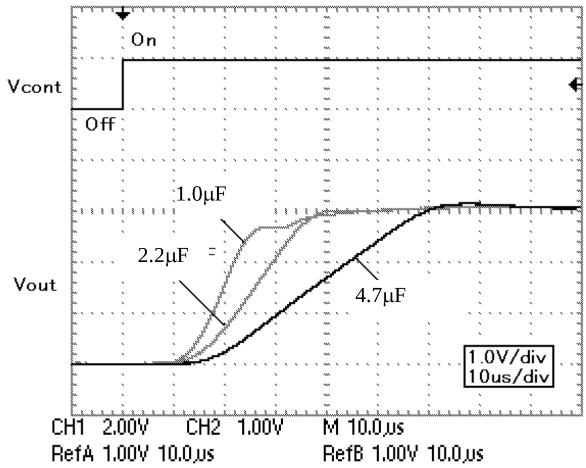


■ Test conditions

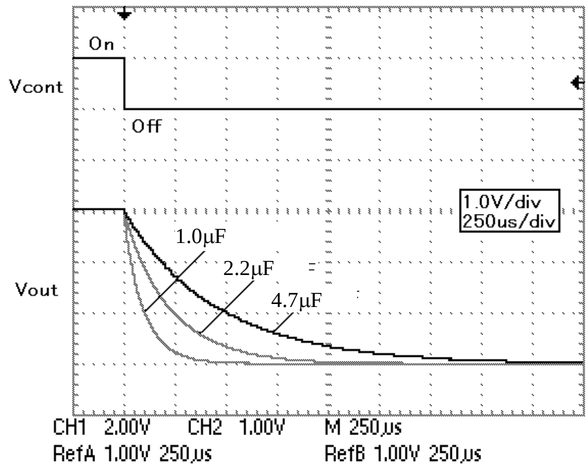


$V_{OUT(TYP)}$=3.0V : R2=163.5kΩ

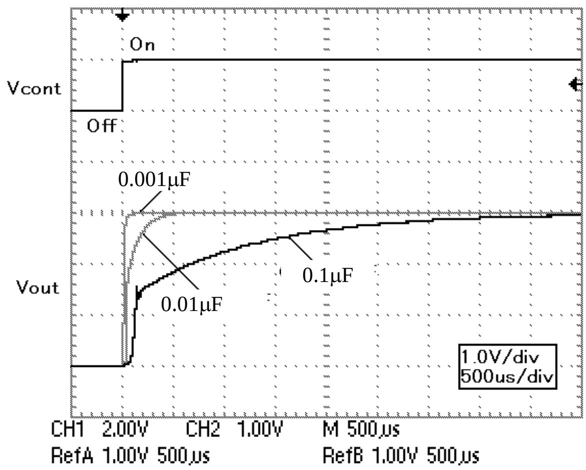
■ C_L=1.0μF, 2.2μF, 4.7μF



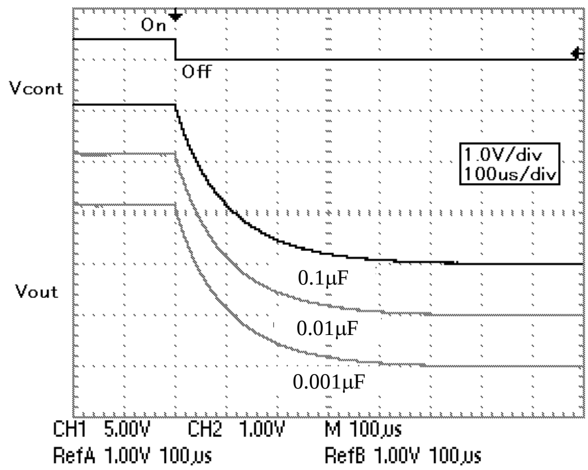
■ C_L==1.0μF, 2.2μF, 4.7μF



■ C_{NP}=0.001μF, 0.01μF, 0.1μF



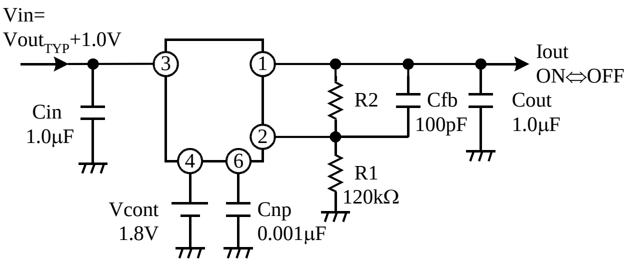
■ C_{NP}=0.001μF, 0.01μF, 0.1μF



・Load Transient

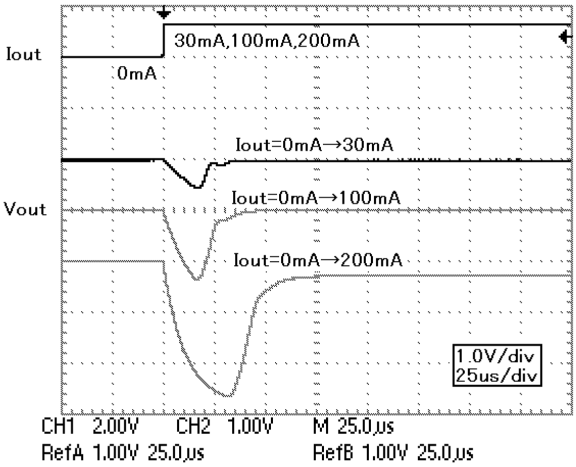
IC can improve the load change to keep some flow of load current. When there is a fast large current change, please increase the load side capacitor. It can reduce the voltage fluctuation.

■ Test conditions

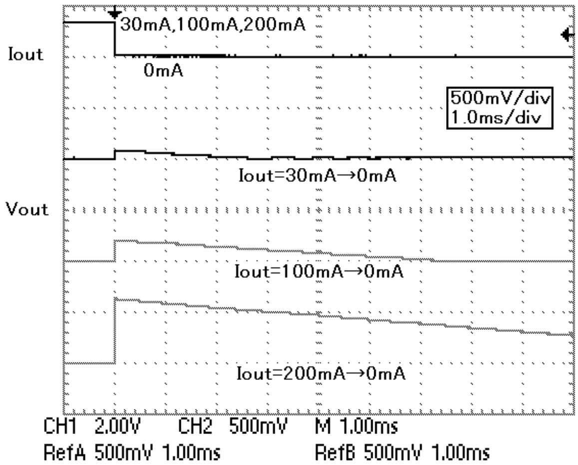


$V_{OUT(TYP)}$ =3.0V : R2=163.5kΩ

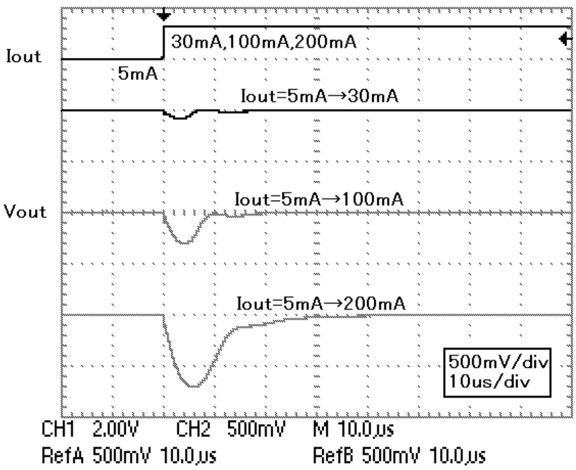
■ I_{OUT}=0⇒30mA, 0⇒100mA, 0⇒200mA



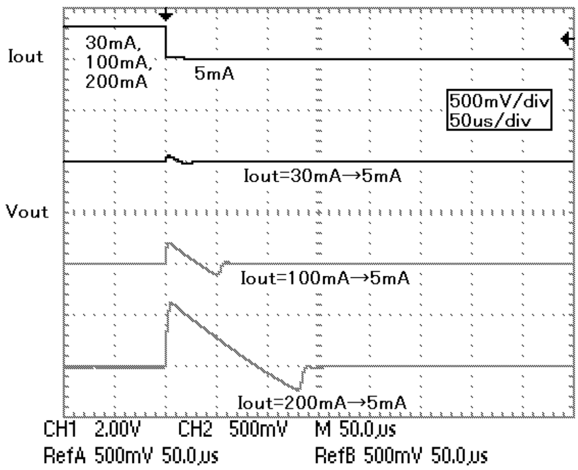
■ I_{OUT}=30⇒0mA, 100⇒0mA, 200⇒0mA



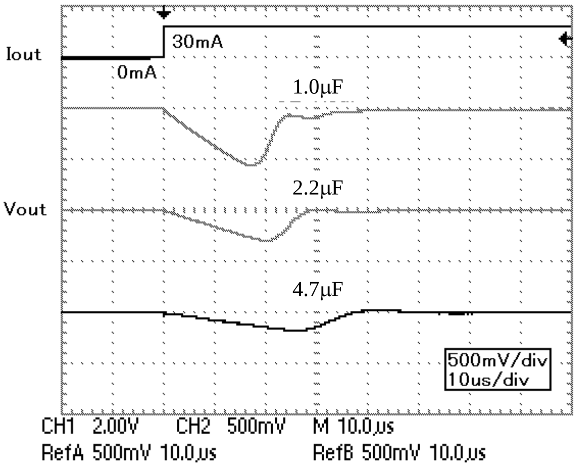
■ I_{OUT}=5⇒30mA, 5⇒100mA, 5⇒200mA



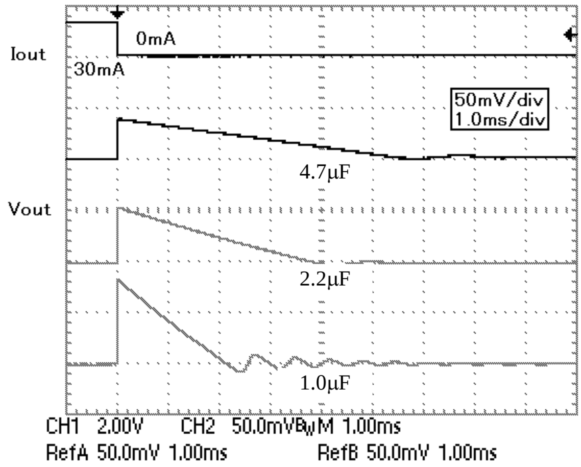
■ I_{OUT}=30⇒5mA, 100⇒5mA, 200⇒5mA



■ C_L=1.0μF, 2.2μF, 4.7μF: I_{OUT}=0⇒30mA

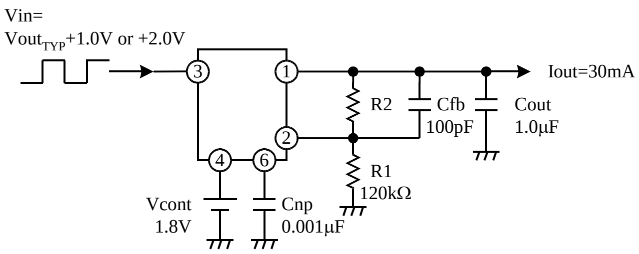


■ C_L=1.0μF, 2.2μF, 4.7μF: I_{OUT}=30⇒0mA



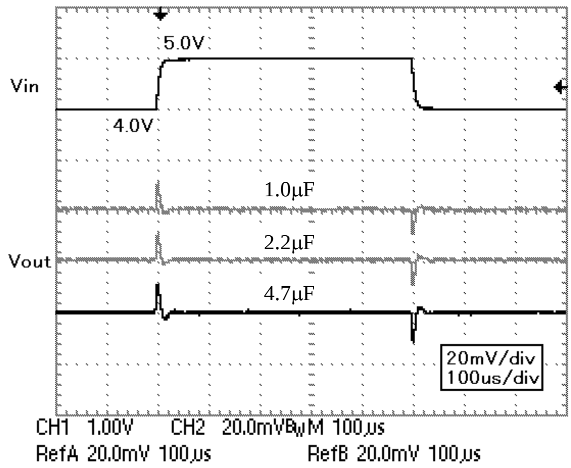
・Line Transient

■ Test conditions

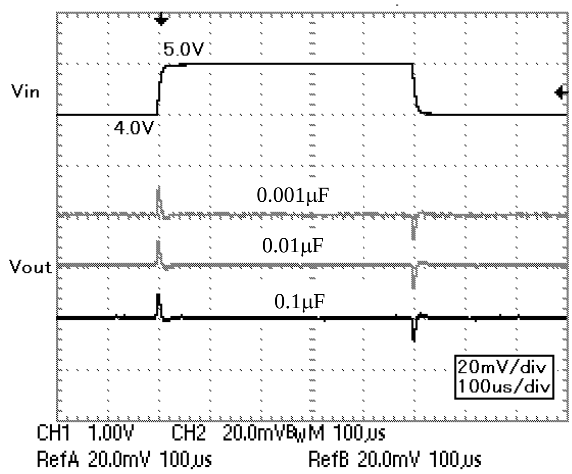


$V_{OUT(TYP)}$=3.0V : R2=163.5kΩ

■ C_L=1.0μF, 2.2μF, 4.7μF



■ C_{NP}=0.001μF, 0.01μF, 0.1μF



11.4 About stable operation

AP1151 is required for input and output capacitors in order to maintain the regulator's loop stability.

・Input Capacitor (C_{IN})

The input capacitor is necessary when the battery is discharged, the power supply impedance increases, or the line distance to the power supply is long. This capacitor might be necessary on each individual IC even if two or more regulator ICs are used. It is not possible to determine this indiscriminately. Please confirm the stability while mounted.
The recommended value is C_{IN} = 1.0μF.

・Output Capacitor (C_L)

Operation is stabilized by 0.22μF ($V_{OUT} \geq$ 1.3V) the output side capacitor (C_L). Without taking into account the ESR if C_L is equal to or greater than 0.22μF in the entire operating temperature range, it can also be used tantalum capacitor not only the ceramic capacitor.
However, since there are variations in the capacity component, can only capacity, please use larger. And large capacitance value as the output noise and ripple noise is reduced small, furthermore, also improves the response to further output side load fluctuation. The IC does not damage by increasing the capacity
In addition, since the low output voltage product is easier to be oscillation, please use or tantalum capacitor to increase the C_L capacity. More of the tantalum capacitor can be obtained the same stability with a smaller value. This serves as the ESR of the tantalum capacitor damping resistance, are considered IC to a more stable operation.
The recommended value is C_{IN} = 1.0μF.

Figure 3 means that IC stable operation with a ceramic capacitor of 0.1uF except for the small current region. In the low voltage and low current region does not stable operation is necessary to increase the capacity. Please select the optimum output capacitor by using voltage and current used. The output side capacitor (C_L) is stable operating larger. (Stable operation area will spread). Please use only the large capacity can be.

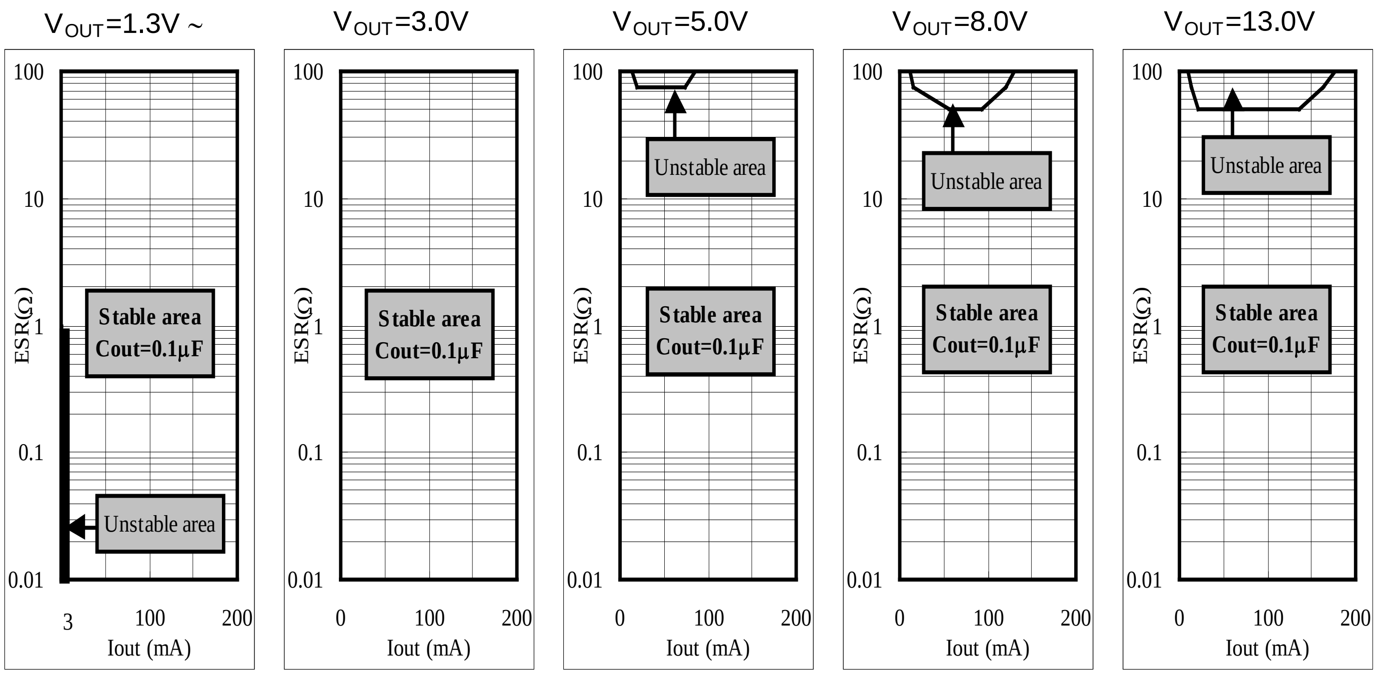
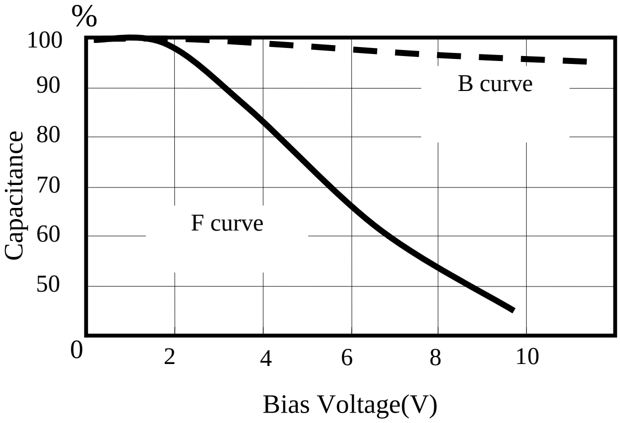


Figure 3. Stable operation area vs. voltage, current, and ESR

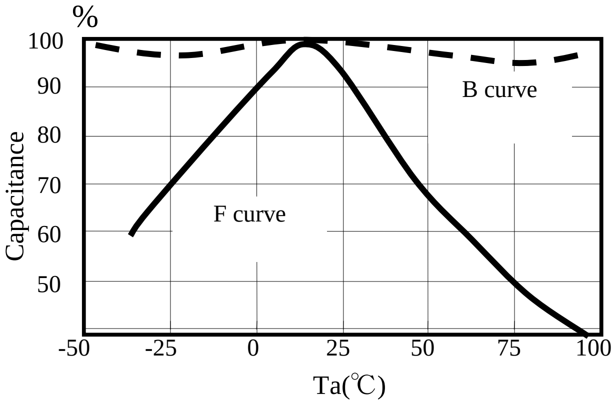
Note 6. Capacitor product was used in the evaluation
Kyocera:CM05B104K10AB,CM05B224K10AB,CM105B104K16A,CM105B224K16A,CM21B225K10A
Murata:GRM36B104K10,GRM42B104K10,GRM39B104K25,GRM39B224K10,GRM39B105K6.3

・Bias voltage and temperature characteristics of the ceramic capacitor
Generally, a ceramic capacitor has both a temperature characteristic and a voltage characteristic. Please consider both characteristics when selecting the part. The B curves are the recommend characteristics.

■ Capacitance versus Voltage



■ Capacitance versus Ambient Temperature



11.5 On/Off Control

It is recommended to turn the regulator off when the circuit following the regulator is non-operating. A design with little electric power loss can be implemented. We recommend the use of the on/off control of the regulator without using a high side switch to provide an output from the regulator. A highly accurate output voltage with low voltage drop is obtained. Because the control current is small, it is possible to control it directly by CMOS logic. The pull-down resister (500kΩ) is built-in.

Table 1. Control terminal voltage and operating state

Control terminal voltage (V_{CONT})	Status
V_{CONT} > 1.8V	ON
V_{CONT} < 0.35V	OFF

11.6 Noise Pass Terminal

The noise and the ripple rejection characteristics depend on the capacitance on the Np terminal. The ripple rejection characteristic of the low frequency region improves by increasing the capacitance of C_{NP}. A standard value is C_{NP}=0.001μF. Increase C_{NP} in a design with important output noise and ripple rejection requirements. The IC will not be damaged if the capacitor value is increased. The On/Off switching speed changes depending on the NP terminal capacitance. The switching speed slows when the capacitance is large.

11.7 Notes on output terminal (V_{OUT}) to GND short-circuit evaluation

The resonance phenomenon due to stick to the output terminal CL (C component) and the short-circuit line (L component), the output terminal will become a negative potential. Output terminal parasitic transistor operates in the IC enters the minus side, leads to the worst case burning for packages that latch-up phenomenon occurs in the IC (white smoke) or damage.
The resonance phenomenon appears remarkably In the ESR value is small ceramic capacitors and the like of the capacitor. As a measure of this phenomenon, we can to reduce the resonance phenomenon to be short-circuited by connecting the short-circuit line and the series in more than 2Ω resistance. This allows you to prevent latch-up phenomenon in the IC.

In large tantalum and electrolytic capacitor of ESR, it generally influence of there resonance phenomenon ESR value is greater than or equal to 2Ω is reduced. Also, if a constraint or the like on your set can not be performed the measures as described above, please insert a schottky diode between GND terminal and the output terminal. This parasitic transistor in the internal IC will not work. A result, you can avoid the latch-up because the parasitic transistor does not work.

11.8 Thermal Resistance and Power Dissipation

・How to determine the thermal resistance when mounted on PCB

The thermal resistance when mounted is expressed as follows:

$$T_j = \theta_{JA} \times P_D + 25$$

T_j of IC is set around 150°C. P_D is the value when the thermal sensor is activated. If the ambient temperature is 25°C, then:

$$150 = \theta_{JA} \times P_D + 25$$
$$\theta_{JA} \times P_D + 25 = 150$$
$$\theta_{JA} \times P_D = 125$$
$$\theta_{JA} = \frac{125}{P_D} \text{ (°C/W)}$$

・Simple method to calculate Power Dissipation(P_D)

Mount the IC on the print circuit board. P_D will be $V_{IN} \times I_{IN}$ when the short circuit on the output side of the IC. The output terminal short-circuited with GND to measure gradually the input current gradually increase the input voltage. Increase gradually to 10V position the input voltage. Initial input current value is the maximum instantaneous output current value, but gradually decreased due to the temperature rise of the chip, it will eventually become a thermal equilibrium state (natural air cooling). This is calculated by using the input current value and the input voltage value when became constant.

$$P_D(\text{mW}) \cong \text{Vin(V)} \times \text{Iin(mA)}$$

・Maximum available current at the maximum temperature

Available at the time the highest operating temperature current, you can ask in the graph of Figure 4. Than DPD value obtained from the graph of Figure 4, the maximum available current at the time of the maximum temperature can be calculated by the following equation.

$$\text{Iout} \cong \{ DP_D \div (V_{in,MAX} - \text{Vout}) \}$$

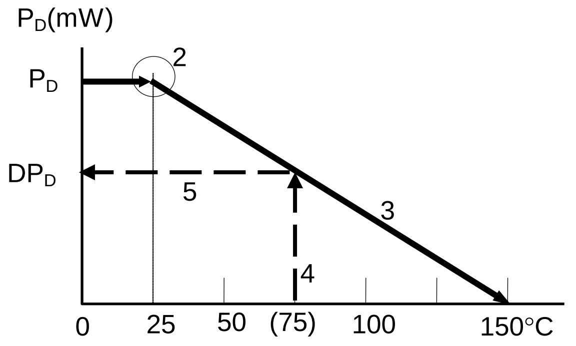
	Procedure (When mounted on PCB.) 1. Find P_D ($V_{IN} \times I_{IN}$ when the output side is short-circuited). 2. Plot P_D against 25°C. 3. Connect Pd to the point corresponding to the 150°C with a straight line. 4. In design, take a vertical line from the maximum operating temperature (e.g., 75°C) to the derating curve. 5. Read off the value of P_D against the point at which the vertical line intersects the derating curve. This is taken as the maximum power dissipation DP_D. 6. $DP_D \div (V_{IN(MAX)} - V_{OUT}) = I_{OUT}$ at 75°C

Figure 4. The simple method to calculate PD

12. Definition of term

■ Characteristics

Each characteristic will be measured in a short period not to be influenced by joint temperature (Tj).

・Output Current (I_{OUT})
Normal output current that can be used. And a range of overheat protection does not operation.

・Maximum Output Current ($I_{OUT(MAX)}$)
The rated output current is specified under the condition where the output voltage drops 0.3V the value specified with I_{OUT}=5mA. The input voltage is set to $V_{OUT(TYP)}$+1V and the current is pulsed to minimize temperature effect.

・Dropout Voltage (V_{DROP})
The dropout voltage is the difference between the input voltage and the output voltage at which point the regulator starts to fall out of regulation. Below this value, the output voltage will fall as the input voltage is reduced. It is dependent upon the load current and the junction temperature.

・Line Regulation (LinReg)
Line regulation is the ability of the regulator to maintain a constant output voltage as the input voltage changes. The line regulation is specified as the input voltage is changed from $V_{IN}=V_{OUT(TYP)}$+1V to $V_{OUT(TYP)}$+6V. It is a pulse measurement to minimize temperature effect.

・Load Regulation (LoaReg)
Load regulation is the ability of the regulator to maintain a constant output voltage as the load current changes. It is a pulsed measurement to minimize temperature effects with the input voltage set to $V_{IN}=V_{OUT(TYP)}$+1V. The load regulation is specified output current step conditions of 5mA to 100mA.

・Ripple Rejection (R.R)
Ripple rejection is the ability of the regulator to attenuate the ripple content of the input voltage at the output. It is specified with 200mVrms, 1kHz super-imposed on the input voltage, where $V_{IN}=V_{OUT}$+1.5V. Ripple rejection is the ratio of the ripple content of the output vs. input and is expressed in dB.

・Standby Current ($I_{STANDBY}$)
Standby current is the current, which flows into the regulator when the output is turned off by the control function (V_{CONT}=0V).

■ Protections

・Over Current Protection
The over current sensor protects the device when there is excessive output current. It also protects the device if the output is accidentally connected to ground.

・Thermal Shutdown Protection
When the power loss of the regulator there are many, it is the ability to limit such that does not exceed the allowable power consumption. Output and the chip temperature reaches about 150°C is turned OFF. However, when the temperature of the chip is reduced, and the output is turned ON again.

13. Recommended External Circuit

■ Recommended External Circuit

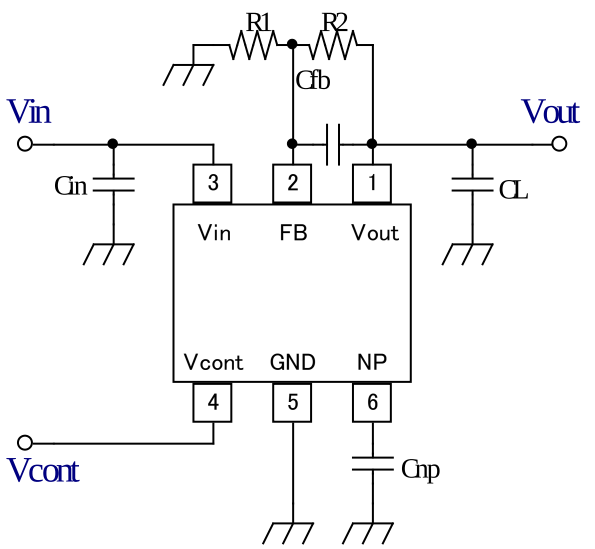
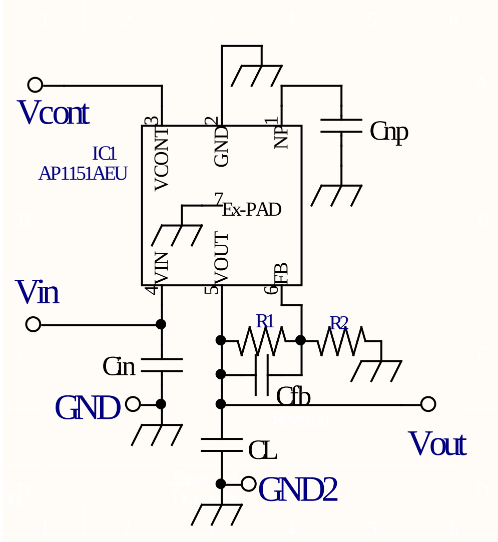
AP1151ADS (SOT23-6)	AP1151AEU (PLP1822-6)
	

Figure 5. External connection circuit example

Table2. Recommended external components example

Parts	min	typ	max	UNIT	備考
C_{IN}	-	1.0	-	μF	
C_L	-	1.0	-	μF	
C_{NP}	-	0.001	-	μF	
C_{FB}		100		pF	
R1	-	51	-	kΩ	$V_{OUT(TYP)}$=3.0V設定時
R2	-	68	-	kΩ	$V_{OUT(TYP)}$=3.0V設定時

Note 7. The above table of values is the recommended example. Please apply the optimal value on the check prior to the time of your on your board.

The output voltage is determined by the following formula.

$$V_{OUT(TYP)} = \frac{R_1 + R_2}{R_1} \times V_{FB}(1.27V)$$

PFeedback resistors R1, R2, please select the resistance to flow more than the current 10μA. The current value is fixed with $\frac{V_{FB}}{R1}$. In the actual application, either ceramic or tantalum capacitor can be used for C_{IN} and C_{OUT}. Please refer to 11.4 for more details. Resistance value of R2, be less than 510kΩ. In case of high output voltage, please adjust R1 value in order to make R2 value smaller than 510kΩ. FB terminal because impedance is high, making it susceptible to the influence of external noise and the like. By connecting the capacity C_{FB} between the V_{OUT} -FB terminal can reduce their impact, also it reduces output noise.

■ Recommended Layout

AP1151ADS (SOT23-6) AP1151AEU (PLP1622-6)

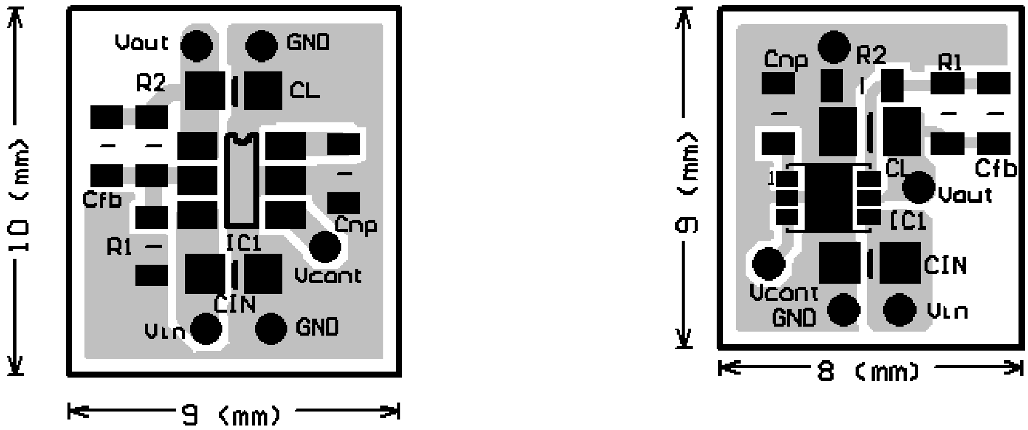


Figure 6. Layout pattern example

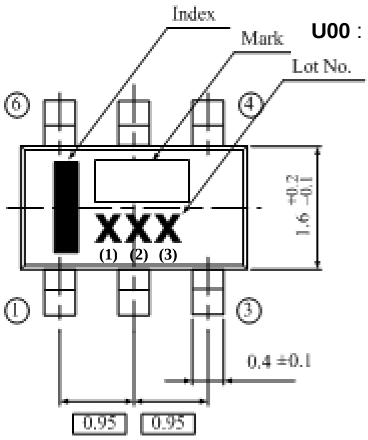
① Place the input capacitor C_{IN} as close as possible to the V_{IN} and GND.
② Place the output capacitor C_L as close as possible to the VOUT and GND.
③ Place the feedback resister R1, R2 as close as possible to the FB terminal. When connecting the output voltage V_{OUT} and the feedback resistor R2, please wiring from the vicinity of the + terminal output capacitor C_L.
④ Place the FB bypass capacitor C_{FB} as close as possible to the V_{OUT} pin and the FB terminal.
⑤ PCB wiring, so as to strengthen the GND area.
⑥ PLP1822-6 of Exposed-Pad has become a shared with the ground of the IC. Please connect to the PCB ground always. Vias (heat dissipation hole) is an effective heat dissipation to the PCB of each layer.

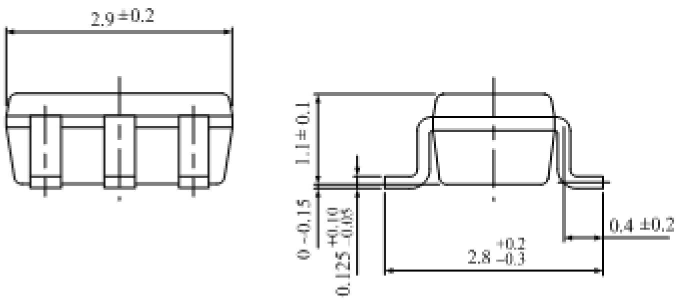
14. Package

■ Outline Dimensions

・SOT23-6

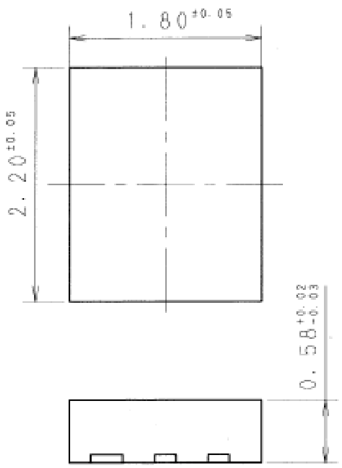
U00 : Product code
(1) Year code(last 1 digit) **(2)**Monthly code **(3)**Management code

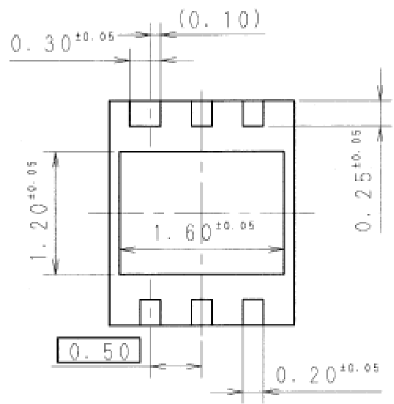




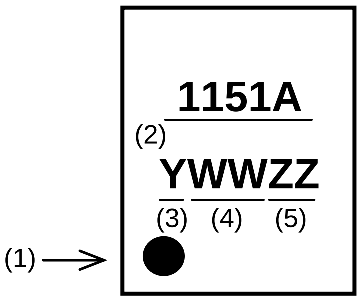
Unit: mm

・PLP1822-6





Unit：mm



(1) 1pin Indication
(2) Market No. (XX:Output Voltage code)
(3) Year code (last 1 digit)
(4) Week code
(5) Management code

15. Revise History

Date (YY/MM/DD)	Revision	Page	Contents
15/1/21	00	-	First edition
17/3/24	01	-	Completely revised as PLP1822-6 package is added

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