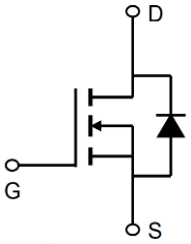
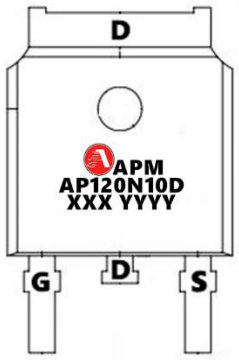
AP120N10D

100V N-Channel Enhancement Mode MOSFET

Description

The AP120N10D uses advanced **APM-SGT** technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a Battery protection or in other Switching application.





General Features

V_{DS} = 100V I_D =120A

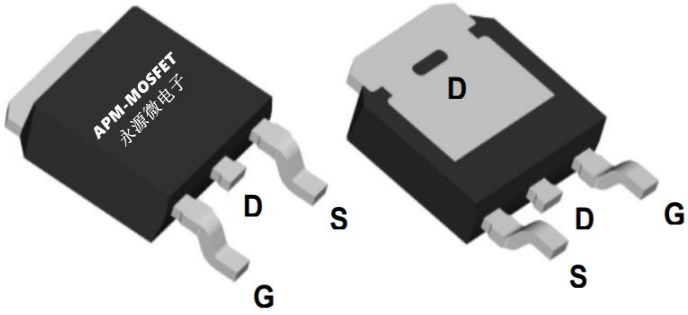
$R_{DS(ON)}$ < 7.5mΩ @ V_{GS}=10V **(Type：6.2mΩ)**

Application

DC/DC Converter

LED Backlighting

Power Management Switches



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP120N10D	TO-252-3L	AP120N10D XXX YYYY	2500

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	100	V
VGS	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V	120	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V	63.5	A
IDM	Pulsed Drain Current	340	A
EAS	Single Pulse Avalanche Energy	135.2	mJ
IAS	Avalanche Current	26	A
P_D@T_C=25℃	Total Power Dissipation[4]	104	W
TSTG	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
RθJA	Thermal Resistance Junction-Ambient	1.2	℃/W
RθJC	Thermal Resistance Junction-Case	62	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100	-	-	V
IGSS	Gate-Body Leakage Current	V_{DS}=0V, V_{GS} =±20V	-	-	±100	nA
IDSS	Zero Gate Voltage Drain Current T_J=25°C	V_{DS}=100V, V_{GS}=0V	-	-	1	μA
	Zero Gate Voltage Drain Current T_J=100°C		-	-	100	
VGS(th)	Gate-Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2.5	3.0	3.5	V
RDS(on)	Drain-Source on-Resistance[4]	V_{GS}=10V, I_D=20A	-	6.2	7.5	mΩ
gfs	Forward Transconductance[4]	V_{DS}=10V, I_D=20A	-	52	-	S
Ciss	Input Capacitance	V_{DS}= 50V, V_{GS}=0V, f=1MHz	-	1480	-	pF
Coss	Output Capacitance		-	736	-	
Crss	Reverse Transfer Capacitance		-	18	-	
R_G	Gate Resistance	f=1MHz	-	2.5	-	Ω
Q_g	Total Gate Charge	V_{GS}=10V, V_{DS}=50V, I_D=20A	-	23	-	nC
Qgs	Gate-Source Charge		-	6.6	-	
Qgd	Gate-Drain Charge		-	5.7	-	
td(on)	Turn-on Delay Time	V_{GS}=10V, V_{DD}=50V, R_G=3Ω, I_D=20A	-	9.3	-	ns
t_r	Rise Time		-	8.4	-	
td(off)	Turn-off Delay Time		-	18	-	
t_f	Fall Time		-	8.9	-	
trr	Body Diode Reverse Recovery Time	I_F=20A, di/dt=100A/μs	-	52	-	ns
Qrr	Body Diode Reverse Recovery Charge			87	-	nC
IS	Continuous Source Current T_C=25°C	I_S=20A, V_{GS}=0V	-	-	120	A
VSD	Diode Forward Voltage[4]		-	-	1.2	V

Notes:

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%

3、The EAS data shows Max. rating . The test condition is V_{DD}=50V, V_{GS}=10V, L=0.4mH, I_{AS}=42A

4、The power dissipation is limited by 150°C junction temperature

5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

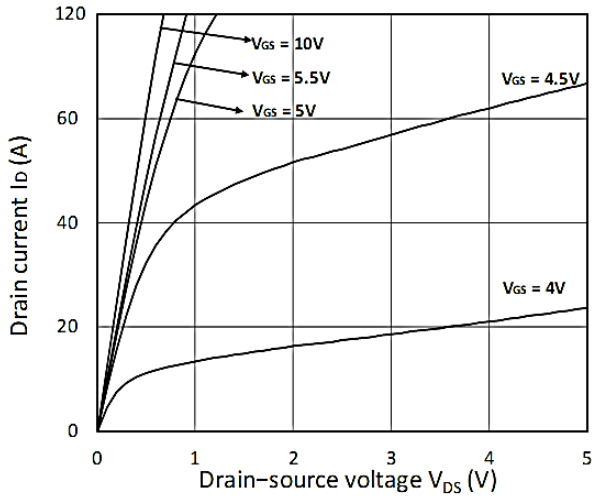


Figure 1. Output Characteristics

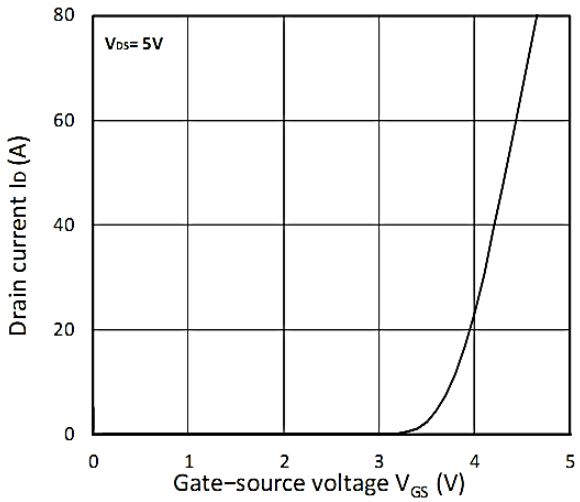


Figure 2. Transfer Characteristics

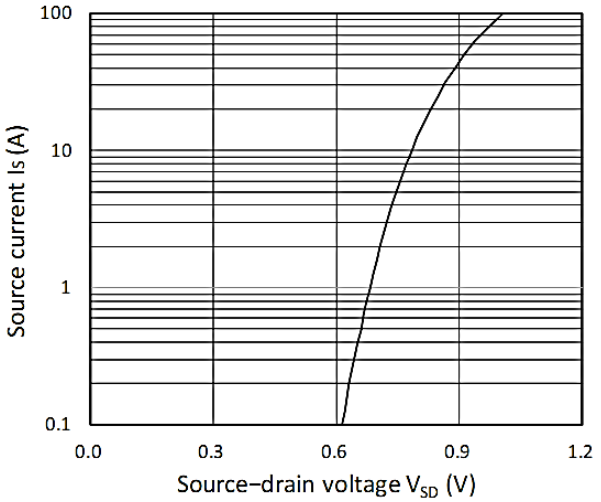


Figure 3. Forward Characteristics of Reverse

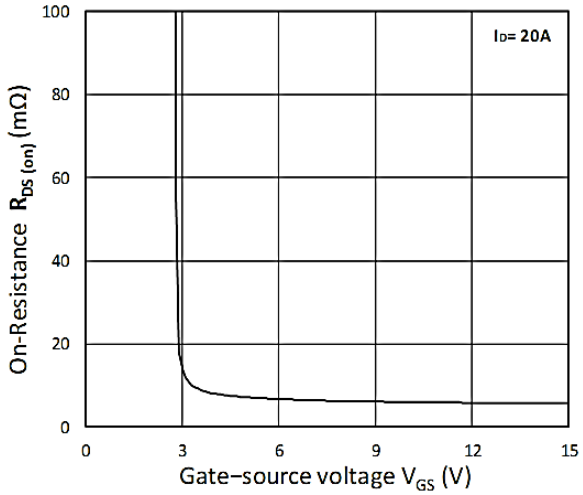


Figure 4. RDS(ON) vs. VGS

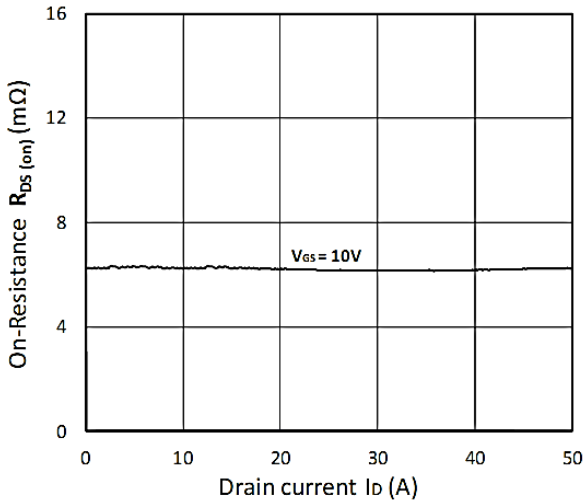


Figure 5. R DS(ON) vs. ID

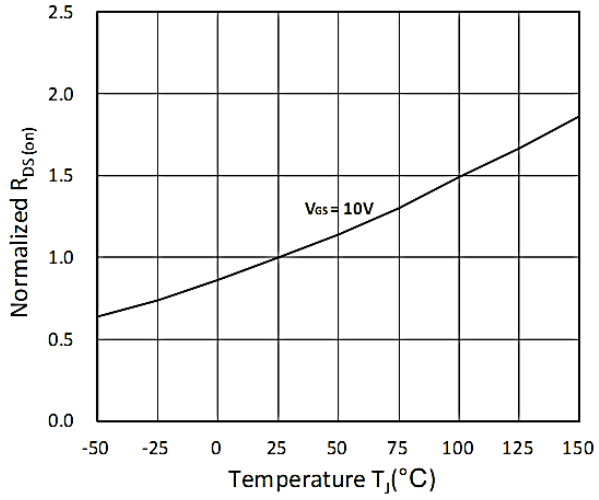


Figure 6. Normalized RDS(on) vs. Temperature

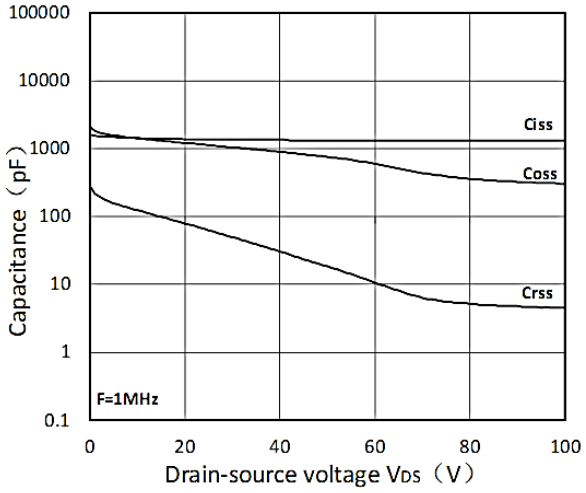


Figure 7. Capacitance Characteristics

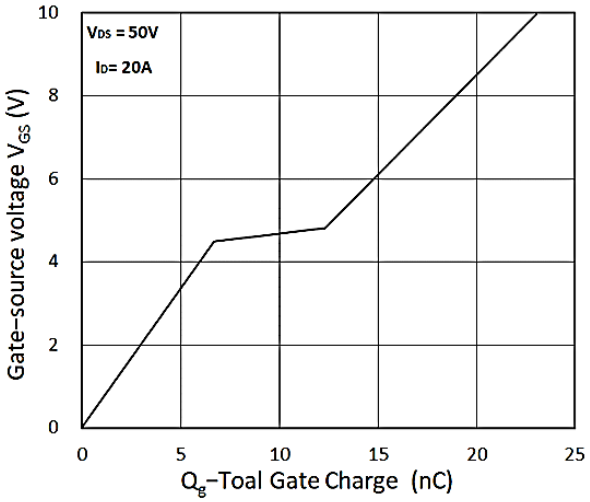


Figure 8. Gate Charge Characteristics

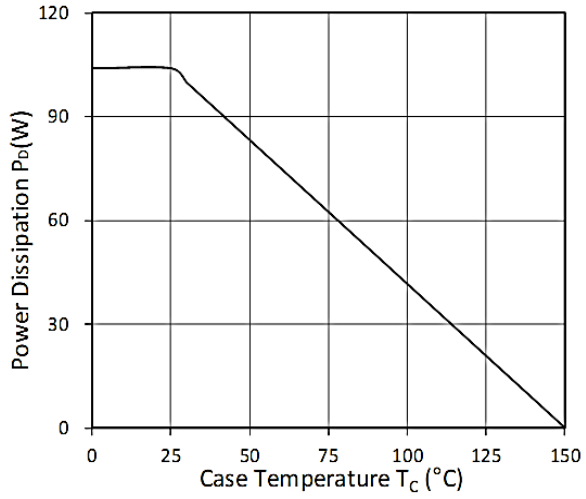


Figure 9. Power Dissipation

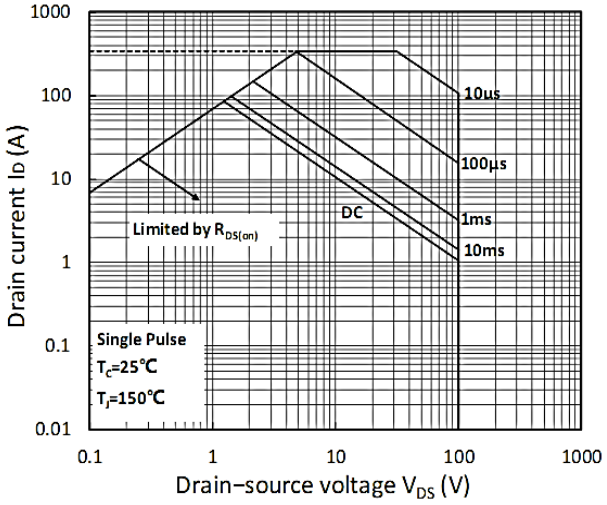


Figure10. Safe Operating Area

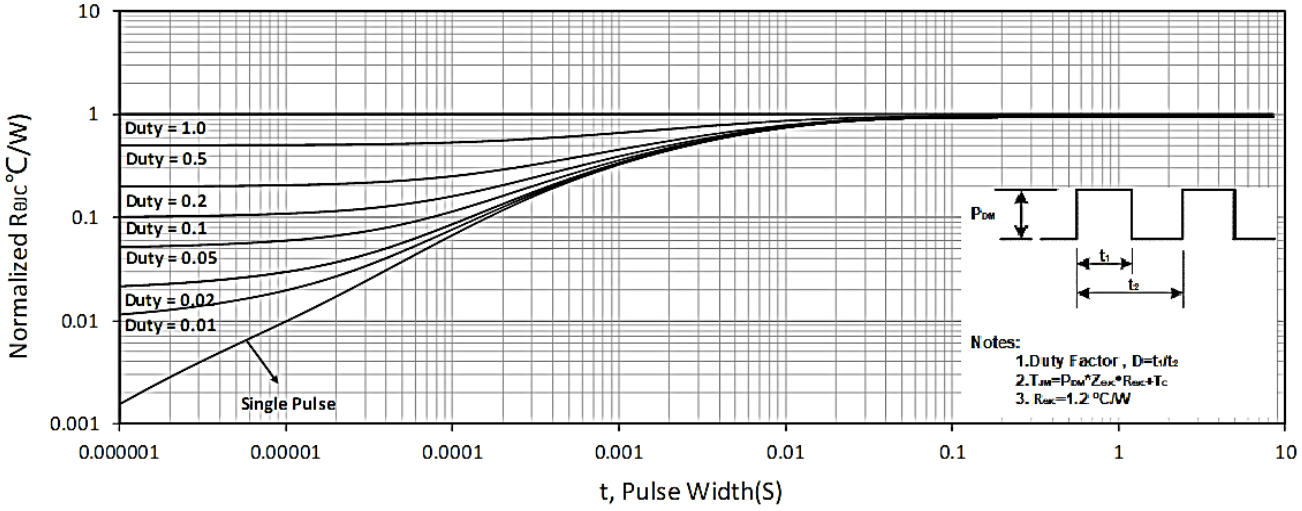
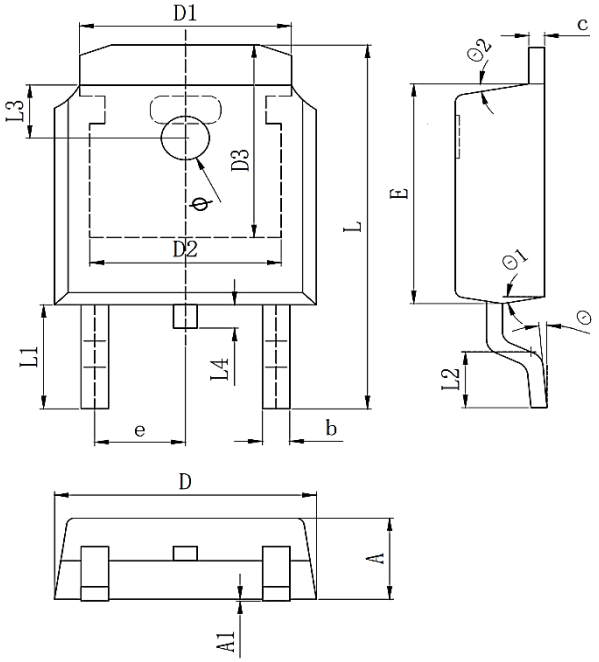


Figure 11. Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-TO-252-3L



Symbol	Dim in mm		
	Min	Typ	Max
A	2.1	2.3	2.5
A1	0	0.064	0.128
b	0.64	0.75	0.86
c	0.45	0.52	0.6
D	6.4	6.6	6.8
D1	5.33REF		
D2	4.83REF		
D3	5.25REF		
E	5.9	6.1	6.3
e	2.286TYP		
L	9.8	10.1	10.4
L1	2.888REF		
L2	1.4	1.5	1.7
L3	1.65REF		
L4	0.6	0.8	1
ϕ	1.1	1.2	1.3
θ	0°		10°
θ1	5°		10°
θ2	5°		10°

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100V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
REV1.0	2022/8/5	Initial release