3A SINK/SOURCE BUS TERMINATION REGULATOR

FEATURES

- **Ideal for DDR-I, DDR-II and DDR-III V_{TT} Applications**
- **Sink and Source 3A Continuous Current**
- **Integrated Power MOSFETs**
- **Generates Termination Voltage for SSTL_2, SSTL_18, HSTL, SCSI-2 and SCSI-3 Interfaces.**
- **High Accuracy Output Voltage at Full-Load**
- **Output Adjustment by Two External Resistors**
- **Low External Component Count**
- **Shutdown for Suspend to RAM (STR) Functionality with High-Impedance Output**
- **Current Limiting Protection**
- **On-Chip Thermal Protection**
- **Available in TO-252-5L & ESOP-8 Packages**
- **V_{IN} and V_{CNTL} No Power Sequence Issue**
- **RoHS Compliant and 100% Lead (Pb)-Free**

APPLICATION

- **Desktop PCs, Notebooks, and Workstations**
- **Graphics Card Memory Termination**
- **Set Top Boxes, Digital TVs, Printers**
- **Embedded Systems**
- **Active Termination Buses**
- **DDR-I, DDR-II and DDR-III Memory Systems**

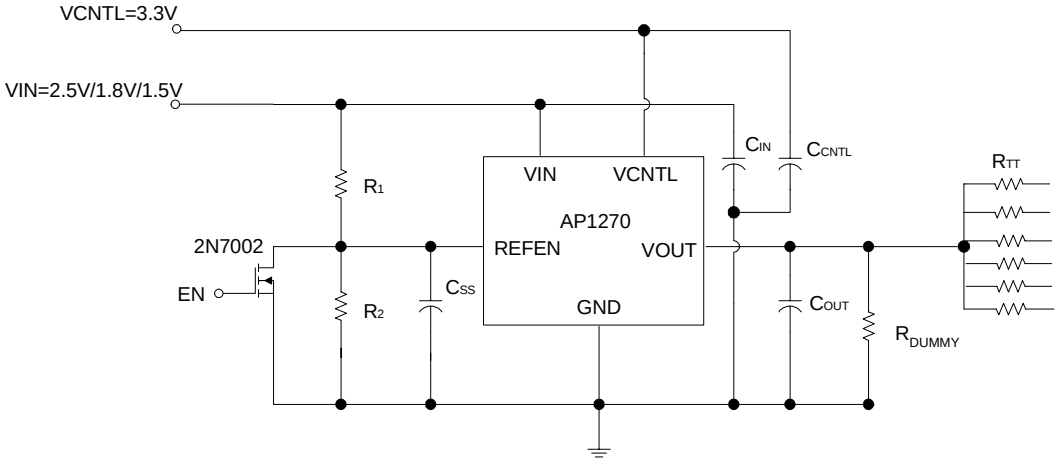
DESCRIPTIOON

The AP1270 is a simple, cost-effective and high-speed linear regulator designed to generate termination voltage in double data rate (DDR) memory system to comply with the JEDEC SSTL_2 and SSTL_18 or other specific interfaces such as HSTL, SCSI-2 and SCSI-3 etc. devices requirements. The regulator is capable of actively sinking or sourcing up to 3A while regulating an output voltage to within 40mV. The output termination voltage cab be tightly regulated to track $1/2V_{DDQ}$ by two external voltage divider resistors or the desired output voltage can be pro-grammed by externally forcing the REFEN pin voltage.

The AP1270 also incorporates a high-speed differential amplifier to provide ultra-fast response in line/load transient. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in bi-directions and on-chip thermal shut-down protection.

The AP1270 are available in the TO-252-5L & ESOP-8 (Exposed Pad) surface mount packages.

TYPICAL APPLICATION



$R_1 = R_2 = 100K\Omega$, $R_{TT} = 50\Omega$ / 33Ω / 25Ω
$C_{OUT,min}$ = 10uF (Ceramic) + 1000uF under the worst case testing condition
C_{SS} = 1µF, C_{IN} = 470µF(Low ESR), C_{CNTL} = 47µF

ABSOLUTE MAXIMUM RATINGS(Note1)

Input Voltage (V_{IN}) ---------- 6V

CNTL Pin Voltage (V_{CNTL}) ---------- 6V

Power Dissipation (P_D) ---------- Internally Limited

Storage Temperature Range (T_{ST}) ---------- -65 to +150°C

Lead Temperature (Soldering, 10sec.) ---------- 260°C

Thermal Resistance from Junction to Case (R_{thjc})

ESOP-8 28°C/W

TO-252-5L 6°C/W

Note1 : Exceeding the absolute maximum rating may damage the device.

OPERATING RATING(Note2)

Input Voltage (V_{IN}) ---------- 2.5V to 1.5V ±3%

CNTL Pin Voltage (V_{CNTL}) ---------- 5.5V or 3.3V ±5%

Junction Temperature Range (T_J) ---------- -40 to +125°C

Ambient Temperature Range (T_A) ---------- -40 to +85°C

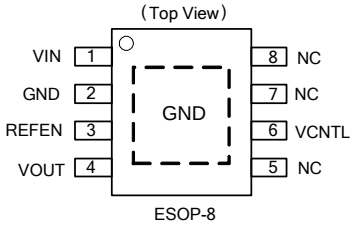
Note2 : The device is not guaranteed to function outside its operating conditions.

ORDERING / PACKAGE INFORMATION

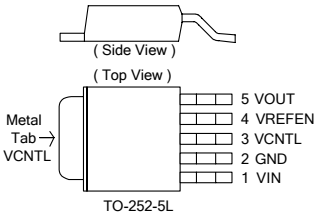
AP1270X-HF

Halogen-Free

MP : ESOP-8
H : TO-252-5L



R_{thja} = 75°C/W



R_{thja} = 40°C/W

ELECTRICAL SPECIFICATIONS

(V_{IN}=1.8V, V_{CNTL}=3.3V, V_{REFEN}=0.9V, C_{OUT}=10uF(Ceramic), T_A =25°C, unless otherwise specified)

Parameter	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Input						
VCNTL Operation Current	I_{CNTL}	I_{OUT} = 0A	-	1	2.5	mA
Standby Current	I_{STBY}	V_{REFEN} < 0.2V (Shutdown), R_{LOAD} = 180Ω	-	50	90	uA
Output (DDR / DDRII / DDRIII)						
Output Offset Voltage(Note3)	V_{OS}	I_{OUT} = 0A	-20	-	20	mV
Load Regulation(Note4)	ΔV_{Load}	I_{OUT} = 10mA ~ 3A	-20	-	20	
		I_{OUT} = -10mA ~ -3A	-20	-	20	
Protection						
Current Limit	I_{LIM}		3.2	-	-	A
Thermal Shutdown Temperature	T_{SD}	3.3V ≤ VCNTL ≤ 5V	130	160	-	°C
Thermal Shutdown Hysteresis	ΔT_{SD}	3.3V ≤ VCNTL ≤ 5V	-	30	-	
REFEN Shutdown						
Shutdown Threshold	V_{IH}	Enable	0.65	-	-	V
	V_{IL}	Shutdown	-	-	0.2	

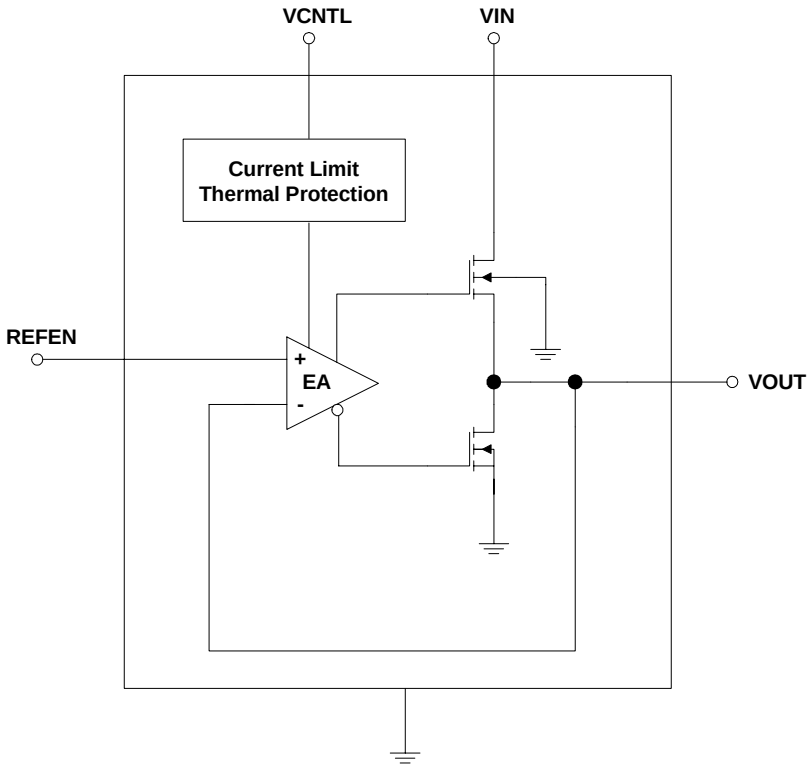
Note3. V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}.

Note4. Regulation is measured at constant junction temperature by using a 5ms current pulse. Devices are tested for load regulation in the load range from 0A to 3A.

PIN DESCRIPTIONS

PIN SYMBOL	PIN DESCRIPTION
V_{IN}	Power Input Voltage.
GND	Ground Pin
V_{OUT}	Output Voltage
V_{CNTL}	Gate Drive Voltage
REFEN	Reference Voltage Input and Chip Enable

BLOCK DIAGRAM



APPLICATION INFORMATION

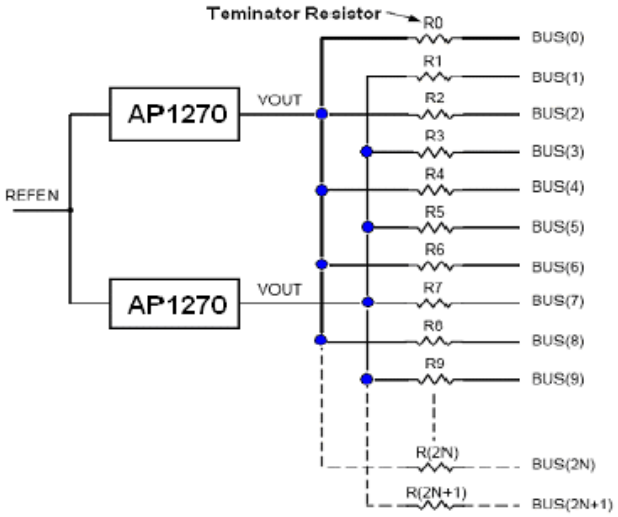
Input Capacitor and Layout Consideration

Place the input bypass capacitor as close as possible to the AP1270. A low ESR capacitor larger than 470uF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance.

Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between AP1270 and the preceding powe converter.

Consideration while designs the resistance of voltage divider

Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on V_{REFEN} is below 0.2V. In addition, the capacitor and voltage divider form the lowpass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.



Thermal Consideration

AP1270MP regulators have internal thermal limiting circuitry designed to protect the device during overload conditions.For continued operation, do not exceed maximum operation junction temperature 125°C. The power dissipation definition in device is:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{thja}$$

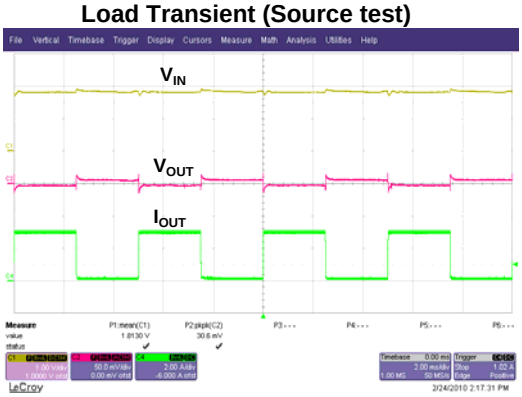
Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the R_{thja} is the junction to ambient thermal resistance. The junction to ambient thermal resistance (R_{thja} is layout dependent) for ESOP-8 package (Exposed Pad) is 75°C/W on standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula:

$$P_{D(MAX)} = (125^oC - 25^oC) / 75^oC/W = 1.33W$$

The thermal resistance R_{thja} of ESOP-8 (Exposed Pad) is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding copper under the expose pad of ESOP-8 package. We have to consider the copper couldn't stretch infinitely and avoid the tin overflow.

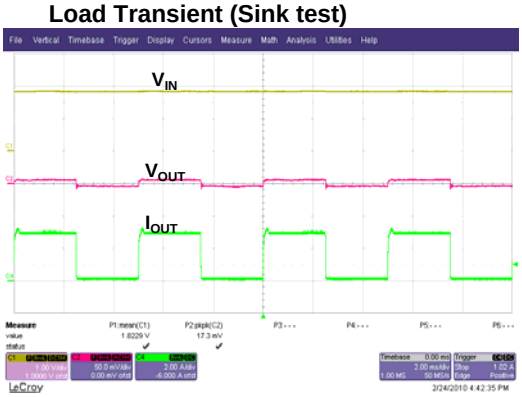
TYPICAL PERFORMANCE CHARACTERISTICS

Load Transient (Source test)



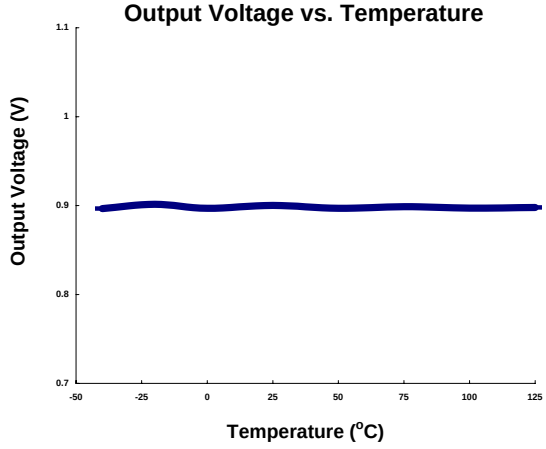
V_{IN} = 1.8V, V_{CNTL} = 3.3V
V_{REF} = 0.9V Supplied by a regulator

Load Transient (Sink test)



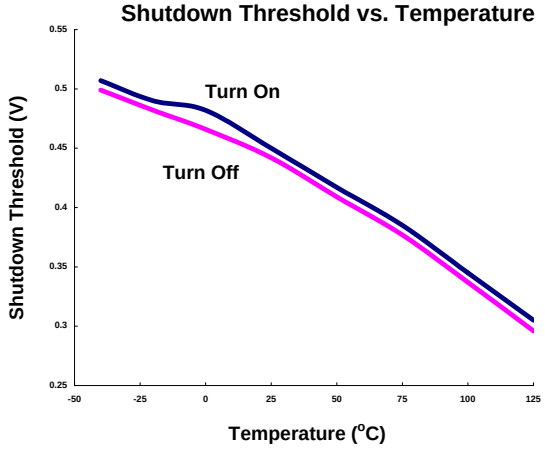
V_{IN} = 1.8V, V_{CNTL} = 3.3V
V_{REF} = 0.9V Supplied by a regulator

Output Voltage vs. Temperature



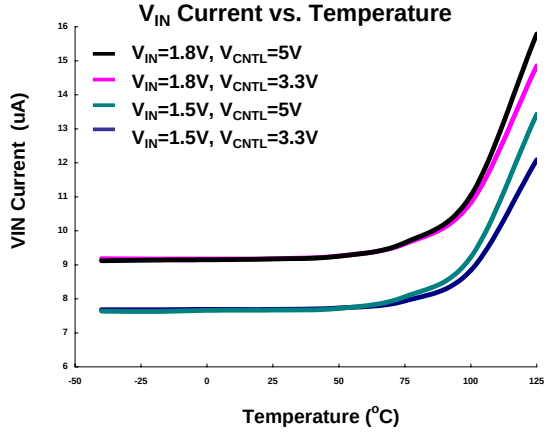
V_{IN} = 1.8V, V_{CNTL} = 3.3V, I_{OUT} = 0A, Source test

Shutdown Threshold vs. Temperature



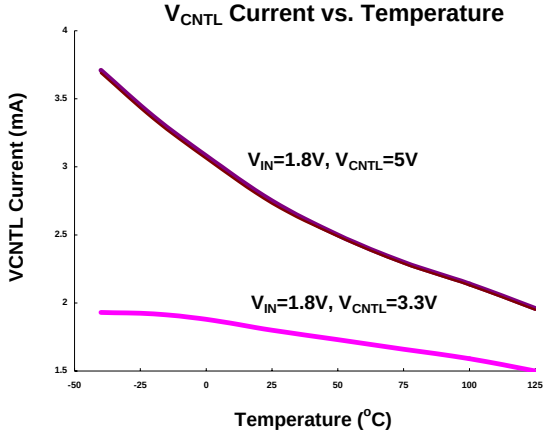
V_{IN} = 1.8V, V_{CNTL} = 3.3V, I_{OUT} = 10mA, Source test

V_{IN} Current vs. Temperature



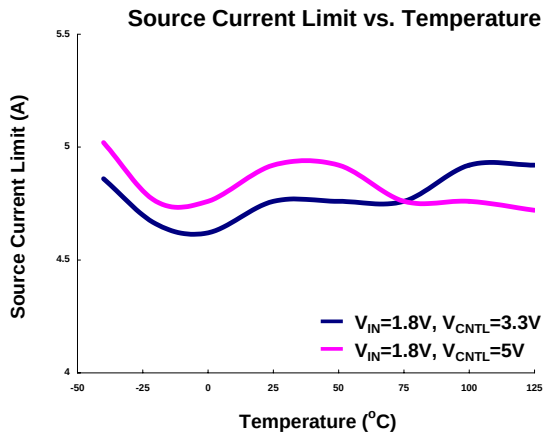
I_{OUT} = 0A, Source test

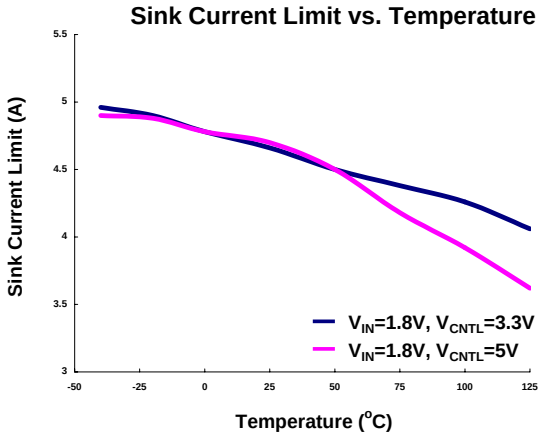
V_{CNTL} Current vs. Temperature



I_{OUT} = 0A, Source test

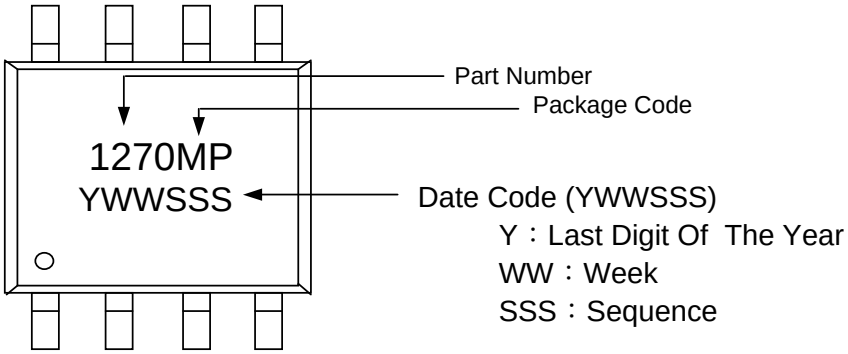
TYPICAL PERFORMANCE CHARACTERISTICS





MARKING INFORMATION

ESOP-8



TO-252-5L