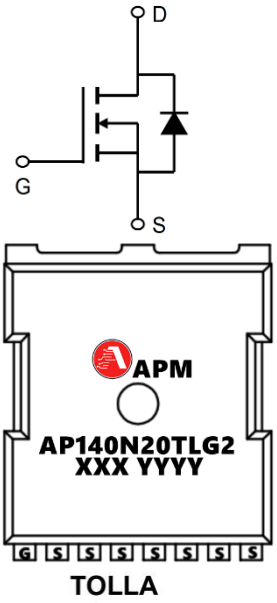
AP140N20TLG2

200V N-Channel Enhancement Mode MOSFET

Description

The AP140N20TLG2 uses advanced **APM-SGT**II technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

V_{DS} = 200V I_D =140A

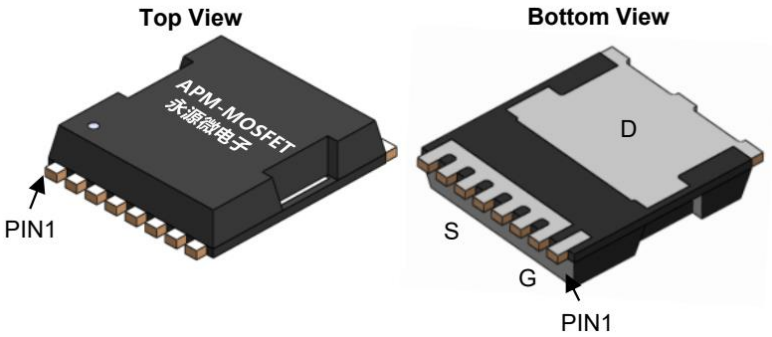
$R_{DS(ON)}$ < 11mΩ @ V_{GS}=10V **(Type：8.5mΩ)**

Application

DC/DC Converter

Power Management Switches

BMS/UPS



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP140N20TLG2	TOLLA-8L	AP140N20TLG2 XXX YYYY	200

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	200	V
VGS	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V	140	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V	75	A
IDM	Pulsed Drain Current	550	A
EAS	Single Pulse Avalanche Energy	2000	mJ
IAS	Avalanche Current	45	A
P_D@T_C=25℃	Total Power Dissipation[4]	278	W
TSTG	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
RθJA	Thermal Resistance Junction-Ambient	0.45	℃/W
RθJC	Thermal Resistance Junction-Case	40	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	ID = 250μA, VGS = 0V	200			V
IDSS	Zero Gate Voltage Drain Current	VDS = 160V, VGS = 0V			1.0	uA
IGSS	Gate-Body Leakage Current	VDS = 0V, VGS = ±20V			±100	nA
VGS(th)	Gate Threshold Voltage	VDS = VGS, ID = 250μA	2.5	3.3	4.5	V
RDS(ON)	Static Drain-Source ON-Resistance	VGS = 10V, ID = 20A		8.5	11	mΩ
gFS	Forward Transconductance	VDS = 5V, ID = 20A		55		S
Ciss	Input Capacitance	VGS = 0V, VDS = 100V, f = 1MHz		6792		pF
Coss	Output Capacitance			5090		pF
Crss	Reverse Transfer Capacitance			389		pF
Rg	Gate Resistance	VGS = 0V, VDS= 0V, f = 1MHz		3.4		Ω
Qg	Total Gate Charge (@ VGS = 10V)	VGS = 0 to 10V VDS = 100V, ID = 20A		80		nC
Qgs	Gate Source Charge			37		nC
Qgd	Gate Drain Charge			11.5		nC
tD(on)	Turn-On DelayTime	VGS = 10V, VDS = 100V RL = 5.0Ω, RGEN = 6Ω		38		ns
tr	Turn-On Rise Time			16		ns
tD(off)	Turn-Off DelayTime			43		ns
tf	Turn-Off Fall Time			10		ns
trr	Body Diode Reverse Recovery Time	IF=55A, dIF/dt = 100A/μs		163		ns
Qrr	Body Diode Reverse Recovery Charge	IF=55A, dIF/dt = 100A/μs		570		nC
VSD	Diode Forward Voltage	IS = 1A, VGS = 0V		0.67	1.0	V
IS	Diode Continuous Current	TC = 25°C			140	A

Notes:

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%

3、The EAS data shows Max. rating . The test condition is V_{DD}=50V, V_{GS}=10V, L=0.5mH, I_{AS}=45A

4、The power dissipation is limited by 150°C junction temperature

5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

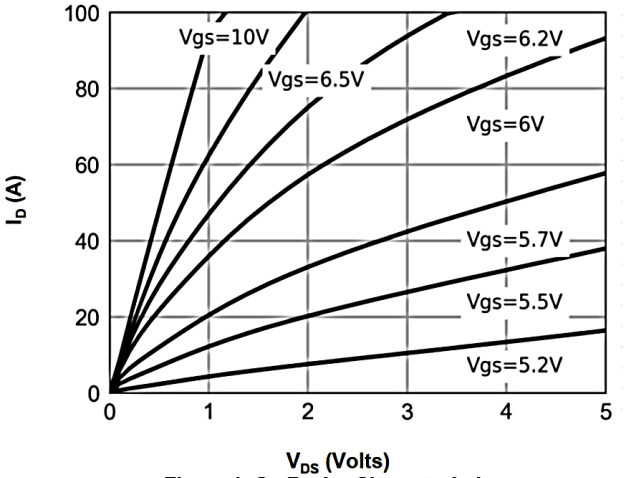


Figure 1: On-Region Characteristics

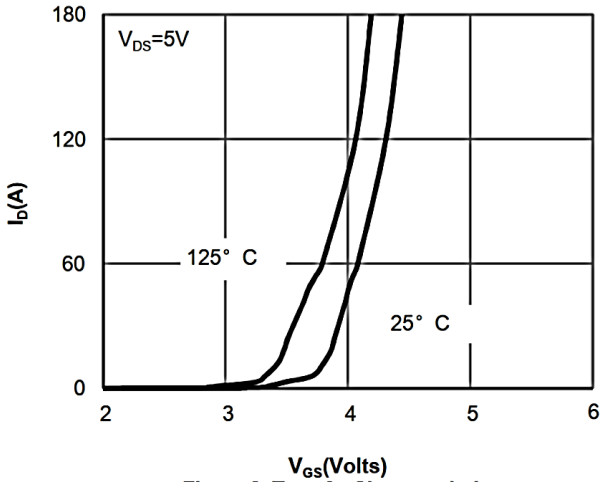


Figure 2: Transfer Characteristics

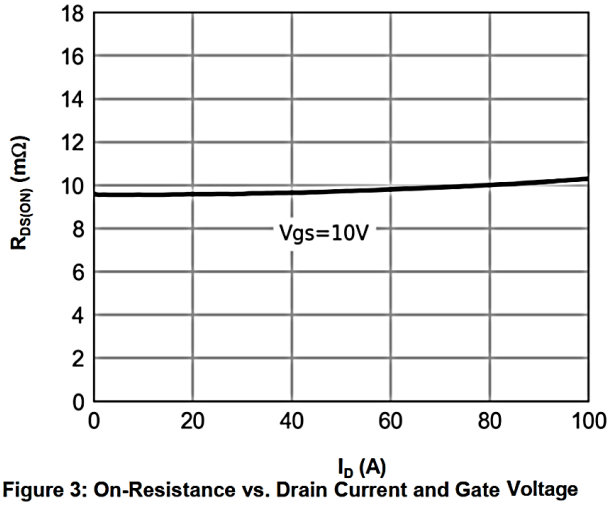


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

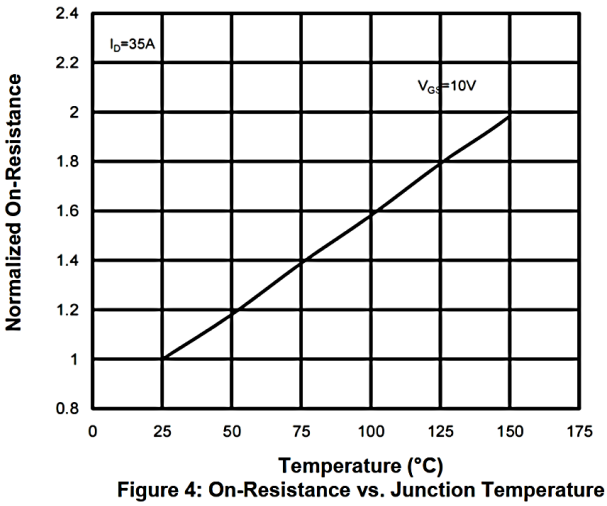


Figure 4: On-Resistance vs. Junction Temperature

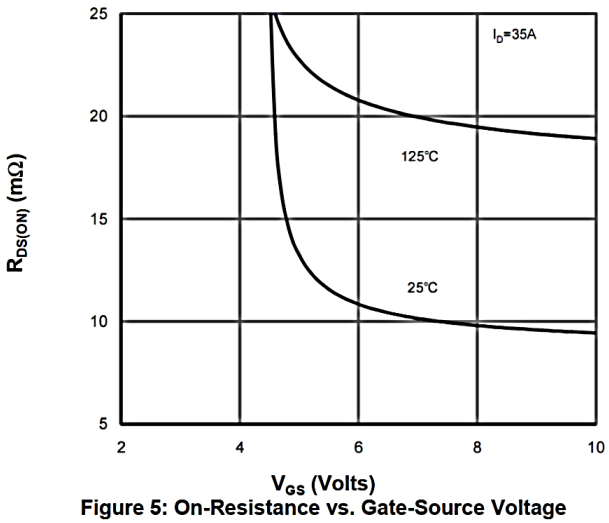


Figure 5: On-Resistance vs. Gate-Source Voltage

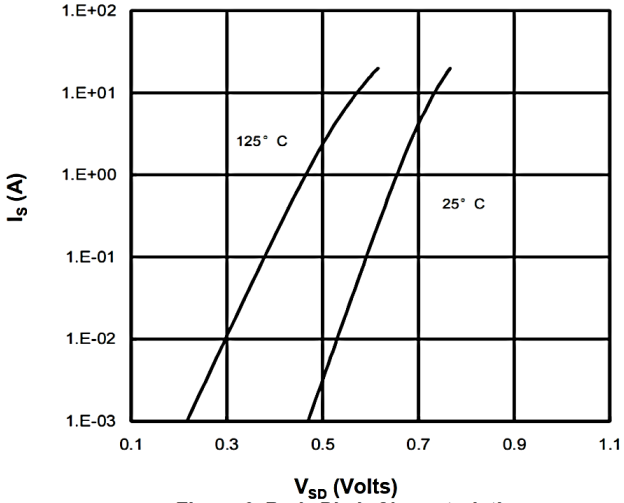


Figure 6: Body-Diode Characteristics

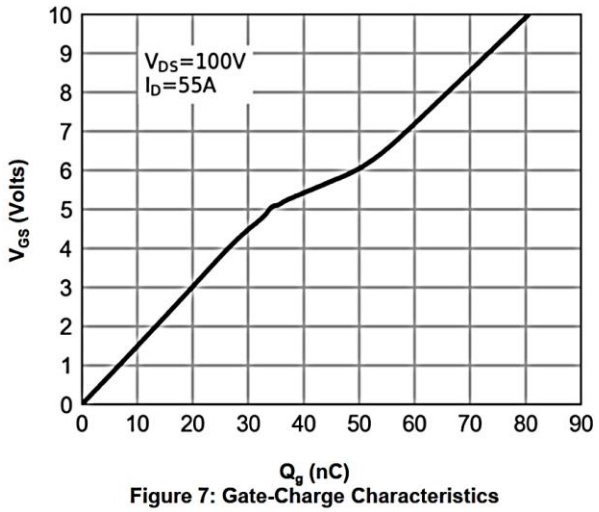


Figure 7: Gate-Charge Characteristics

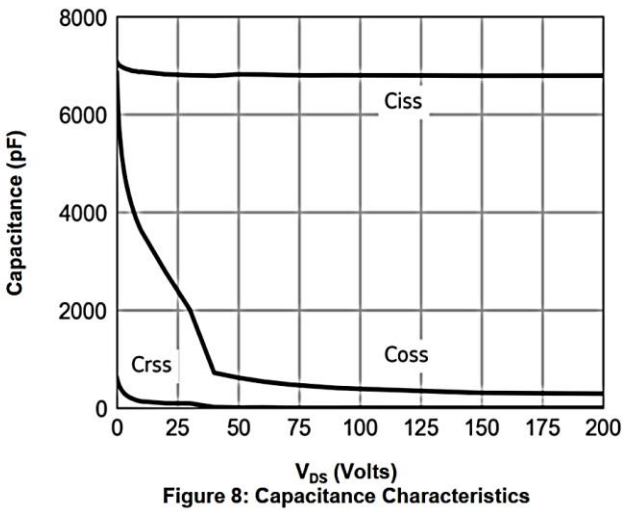


Figure 8: Capacitance Characteristics

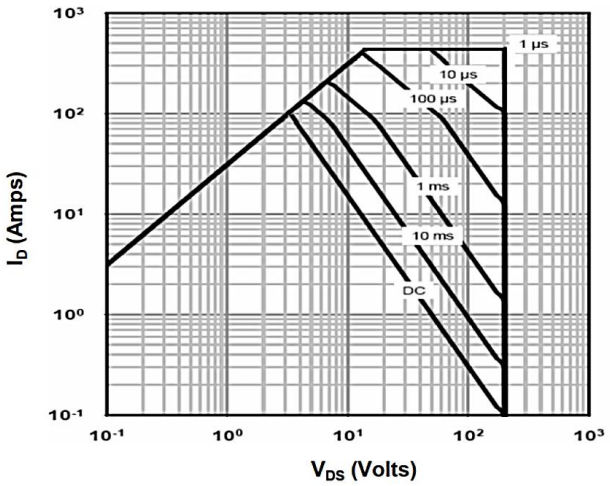
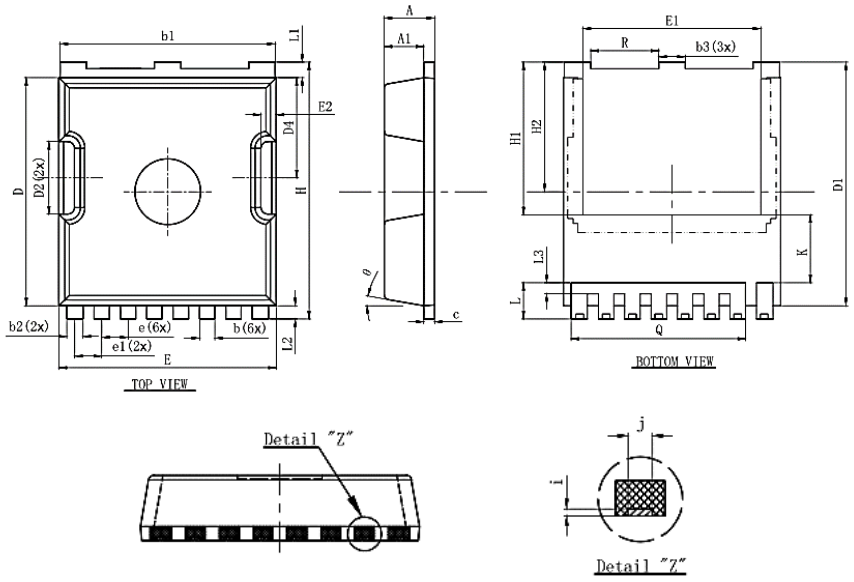


Figure 9: Maximum Forward Biased Safe Operating Area

Package Mechanical Data-TOLLA-8-XZ Single



Symbol	Dimensions In Millimeters		
	Min.	Nom	Max.
A	2.2	2.3	2.4
A1	1.7	1.8	1.9
b	0.6	0.7	0.8
b1	9.7	9.8	9.9
b2	0.65	0.75	0.85
b3	1.1	1.2	1.3
C	0.4	0.5	0.6
D	10.3	10.4	10.5
D1	11.0	11.1	11.2
D2	3.2	3.3	3.4
D4	4.47	4.57	4.67
E	9.8	9.9	10.0
E1	8.0	8.1	8.2
E2	0.5	0.6	0.7
e	1.200（BSC）		
e1	1.225（BSC）		
H	11.6	11.7	11.8
H1	6.95BSC		
H2	5.9BSC		
i	0.1REF		
j	0.350REF		
K	3.100REF		
L	1.55	1.65	1.75
L1	0.6	0.7	0.8
L2	0.5	0.6	0.7
L3	0.4	0.5	0.6
Q	7.95REF		
R	3.0	3.1	3.2
θ	10°REG		

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200V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
REV1.0	2023/3/5	Initial release