

## 20V N+P-Channel Enhancement Mode MOSFET

### Description

The AP15G02DF uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 20V$   $I_D = 15.5A$

$R_{DS(ON)} < 35m\Omega$  @  $V_{GS}=4.5V$  (Type: 22m $\Omega$ )

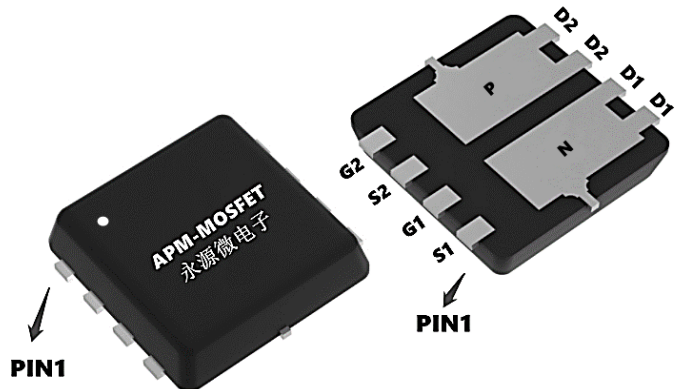
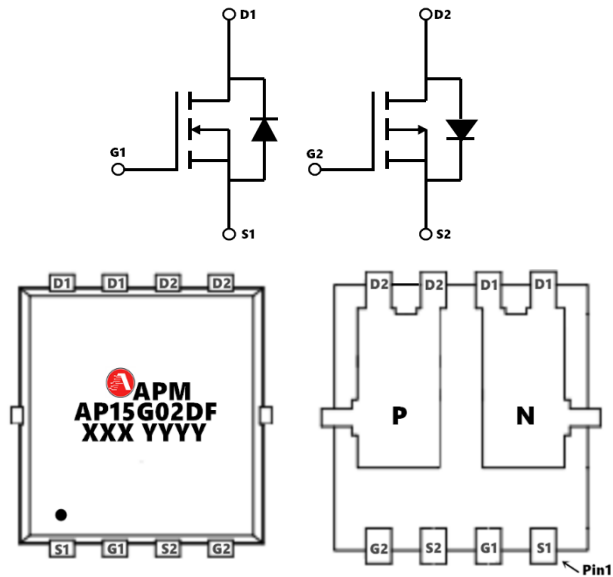
$V_{DS} = -20V$   $I_D = -14.8A$

$R_{DS(ON)} < 35m\Omega$  @  $V_{GS}=-4.5V$  (Type: 28m $\Omega$ )

### Application

High Frequency Circuit

low-power consumption



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP15G02DF	PDFN3*3-8L	AP15G02DF XXX YYYY	3000

### Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
$V_{DS}$	Drain-Source Voltage	20	-20	V
$V_{GS}$	Gate-Source Voltage	$\pm 12$	$\pm 12$	V
$I_D@T_A=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	15.5	-14.8	A
$I_D@T_A=70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	12.2	-11.5	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	48	-44	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	24	78	mJ
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation <sup>4</sup>	1.5		W
$T_{STG}$	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	85		$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	60		$^\circ\text{C/W}$

**20V N+P-Channel Enhancement Mode MOSFET**
**N-Electrical Characteristics ( $T_J=25^{\circ}\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V$ , $I_D=250\mu A$	20	22	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=4.5V$ , $I_D=3A$	---	22	35	m $\Omega$
		$V_{GS}=2.5V$ , $I_D=2A$	---	26	40	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$ , $I_D=250\mu A$	0.5	0.75	1.2	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=16V$ , $V_{GS}=0V$ , $T_J=25^{\circ}\text{C}$	---	---	1	uA
		$V_{DS}=16V$ , $V_{GS}=0V$ , $T_J=55^{\circ}\text{C}$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 12V$ , $V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=5V$ , $I_D=3A$	---	10.5	---	S
$Q_g$	Total Gate Charge (4.5V)	$V_{DS}=15V$ , $V_{GS}=4.5V$ , $I_D=3A$	---	4.6	---	nC
$Q_{gs}$	Gate-Source Charge		---	0.7	---	
$Q_{gd}$	Gate-Drain Charge		---	1.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=10V$ , $V_{GS}=4.5V$ , $R_G=3.3\Omega$ , $I_D=3A$	---	1.6	---	ns
$T_r$	Rise Time		---	42	---	
$T_{d(off)}$	Turn-Off Delay Time		---	14	---	
$T_f$	Fall Time		---	7	---	
$C_{iss}$	Input Capacitance	$V_{DS}=15V$ , $V_{GS}=0V$ , $f=1\text{MHz}$	---	310	---	pF
$C_{oss}$	Output Capacitance		---	49	---	
$C_{rss}$	Reverse Transfer Capacitance		---	35	---	
$I_S$	Continuous Source Current <sup>1,4</sup>	$V_G=V_D=0V$ , Force Current	---	---	3.6	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V$ , $I_S=1A$ , $T_J=25^{\circ}\text{C}$	---	---	1.2	V

**Note :**

- 1、The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper.
- 2、The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3、The power dissipation is limited by 150 $^{\circ}\text{C}$  junction temperature
- 4、The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

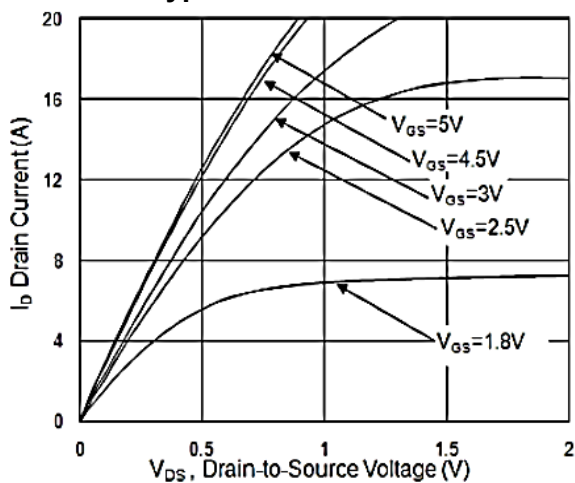
**20V N+P-Channel Enhancement Mode MOSFET**
**P-Electrical Characteristics ( $T_J=25^{\circ}\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V(BR)DSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20	-24	-	V
IDSS	Zero Gate Voltage Drain Current	$V_{DS}=-20V, V_{GS}=0V,$	-	-	-1	$\mu A$
IGSS	Gate to Body Leakage Current	$V_{DS}=0V, V_{GS}=\pm 12V$	-	-	$\pm 100$	nA
VGS(th)	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.4	-0.7	-1.0	V
RDS(on)	Static Drain-Source on-Resistance note2	$V_{GS}=-4.5V, I_D=-4.1A$	-	28	35	m $\Omega$
RDS(on)	Static Drain-Source on-Resistance note2	$V_{GS}=-2.5V, I_D=-3A$	-	35	42	m $\Omega$
Ciss	Input Capacitance	$V_{DS}=-10V, V_{GS}=0V,$ $f=1.0MHz$	-	830	-	pF
Coss	Output Capacitance		-	132	-	pF
Crss	Reverse Transfer Capacitance		-	85	-	pF
Qg	Total Gate Charge	$V_{DS}=-10V, I_D=-2A,$ $V_{GS}=-4.5V$	-	8.8	-	nC
Qgs	Gate-Source Charge		-	1.4	-	nC
Qgd	Gate-Drain("Miller") Charge		-	1.9	-	nC
td(on)	Turn-on Delay Time	$V_{DD}=-10V, I_D=-3.3A,$ $R_G=1\Omega, V_{GEN}=-4.5V$	-	10	-	ns
tr	Turn-on Rise Time		-	32	-	ns
td(off)	Turn-off Delay Time		-	50	-	ns
tf	Turn-off Fall Time		-	51	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-4.1	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-16	A
VSD	Drain to Source Diode Forward Voltage	$V_{GS}=0V, I_S=-4.1A$	-	-	-1.2	V

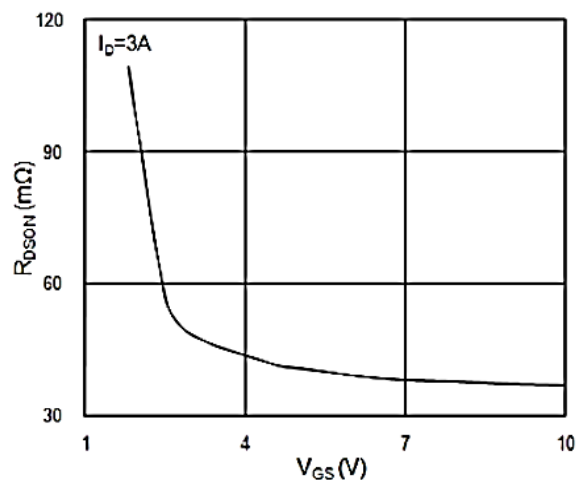
**Note :**

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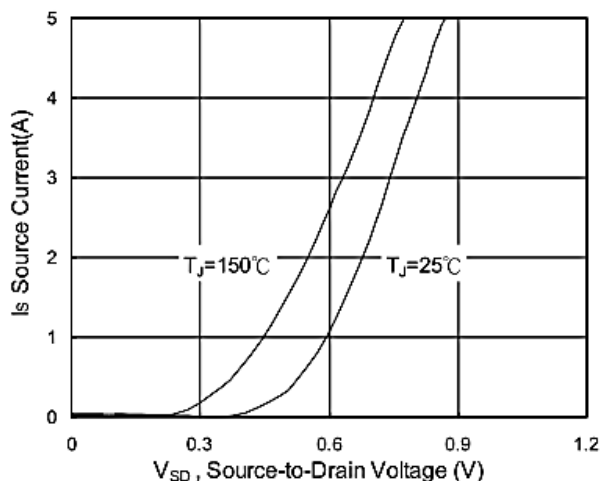
### N-Channel Typical Characteristics



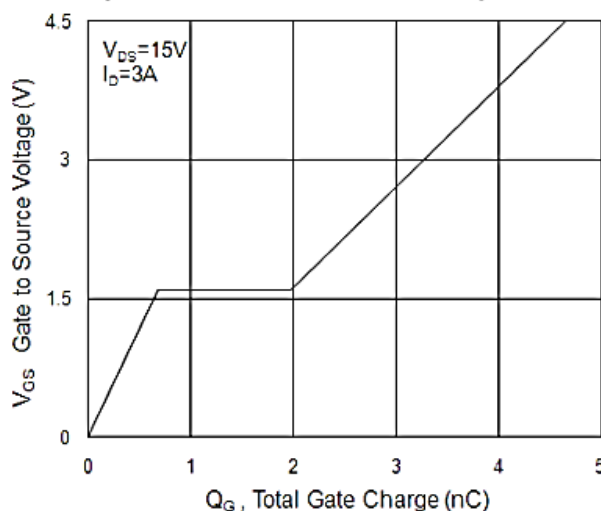
**Fig.1 Typical Output Characteristics**



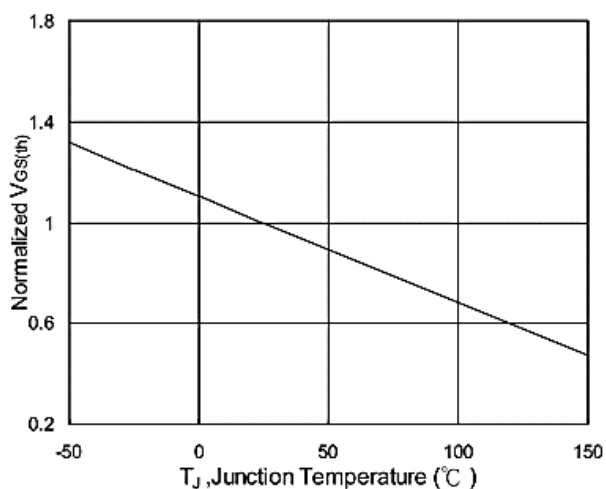
**Fig.2 On-Resistance vs. G-S Voltage**



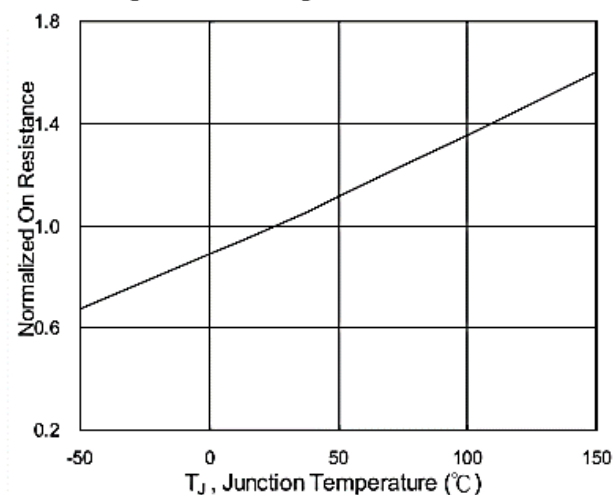
**Fig.3 Source Drain Forward Characteristics**



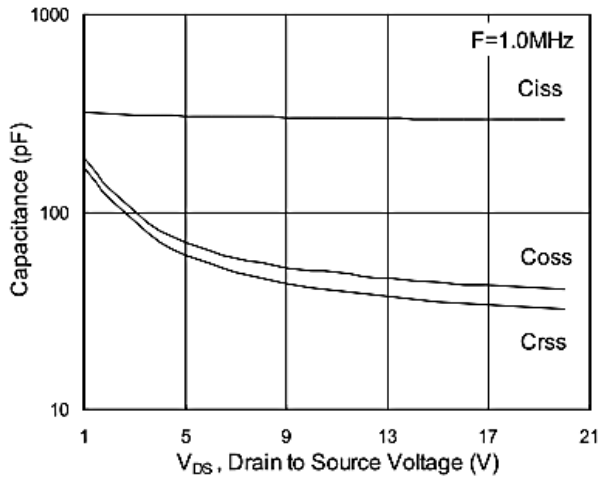
**Fig.4 Gate-Charge Characteristics**



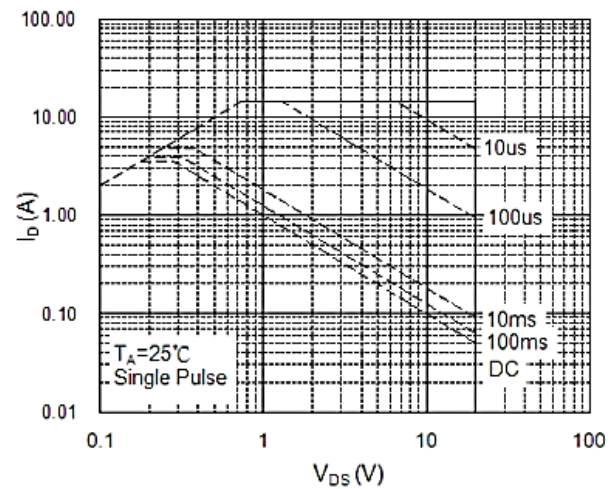
**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**



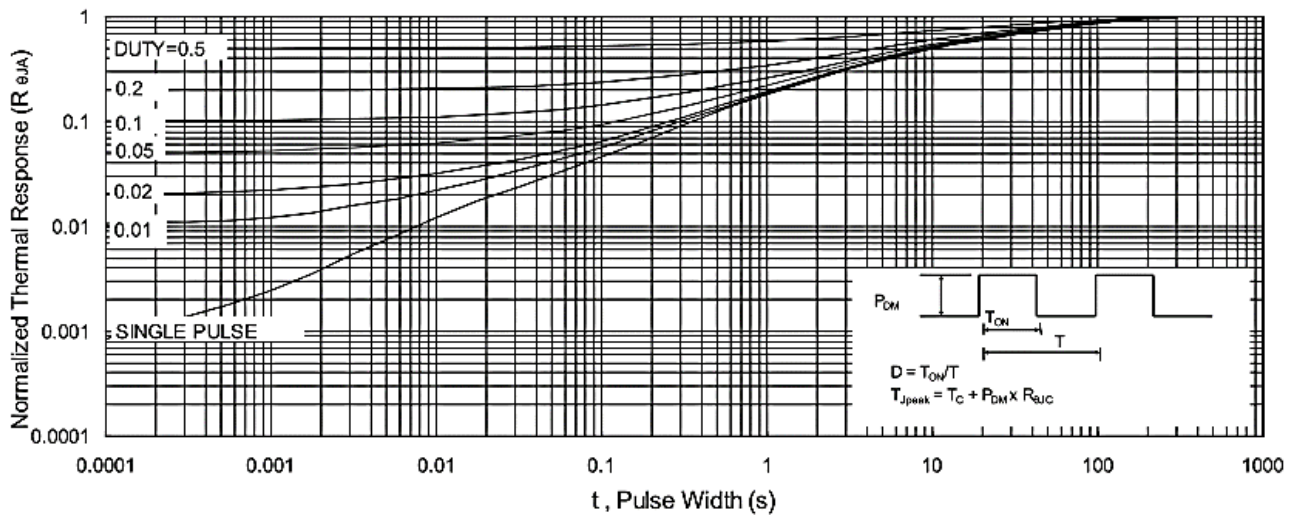
**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**



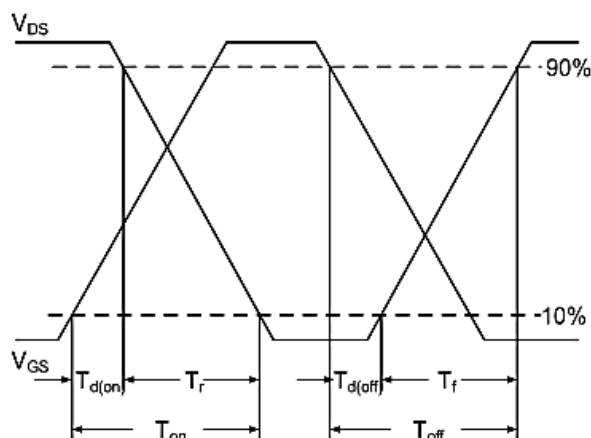
**Fig.7 Capacitance**



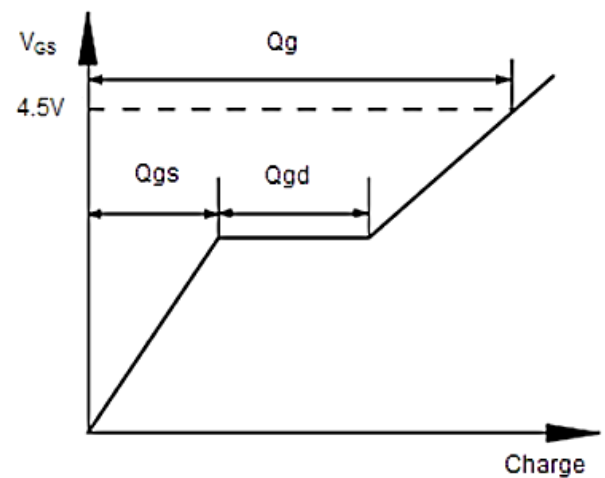
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

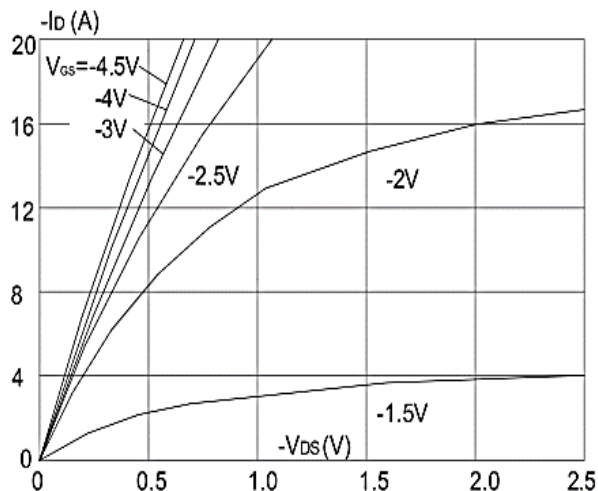


**Fig.10 Switching Time Waveform**

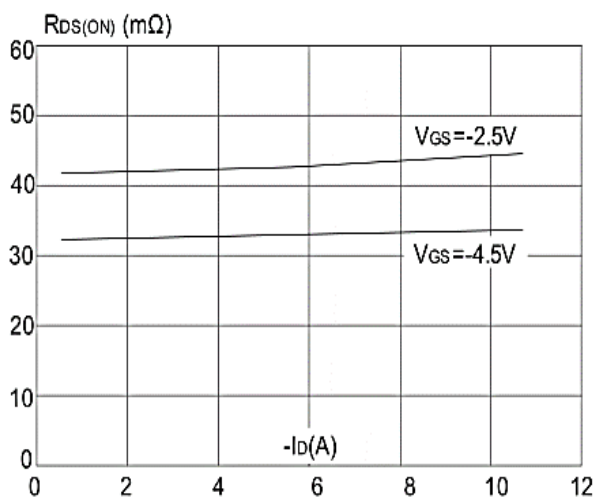


**Fig.11 Gate Charge Waveform**

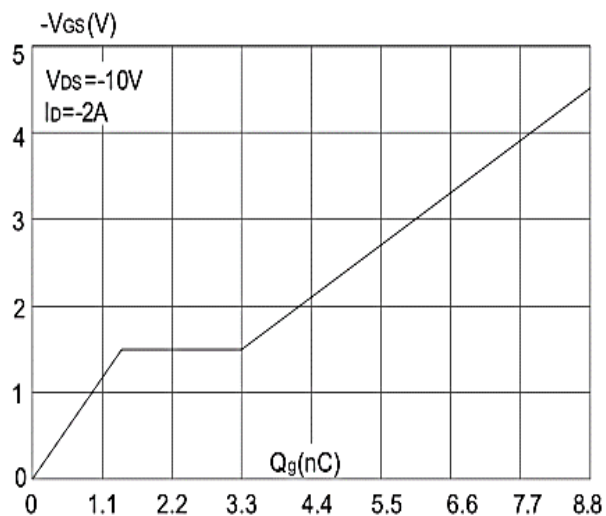
### P-Channel Typical Characteristics



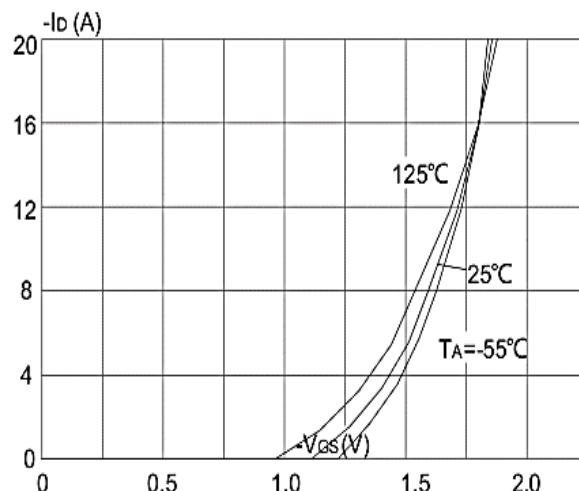
**Figure1: Output Characteristics**



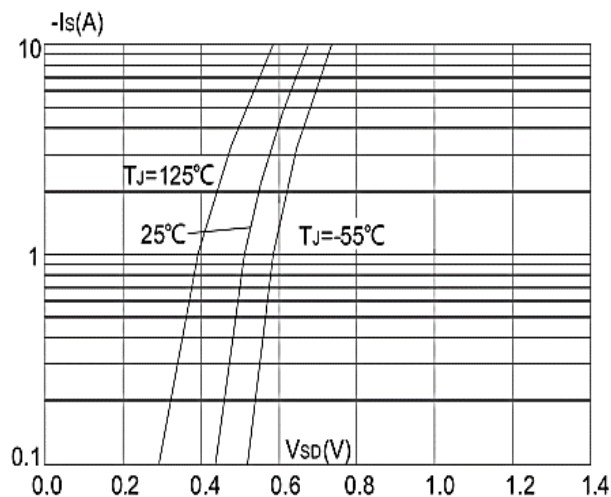
**Figure 3:On-resistance vs. Drain Current**



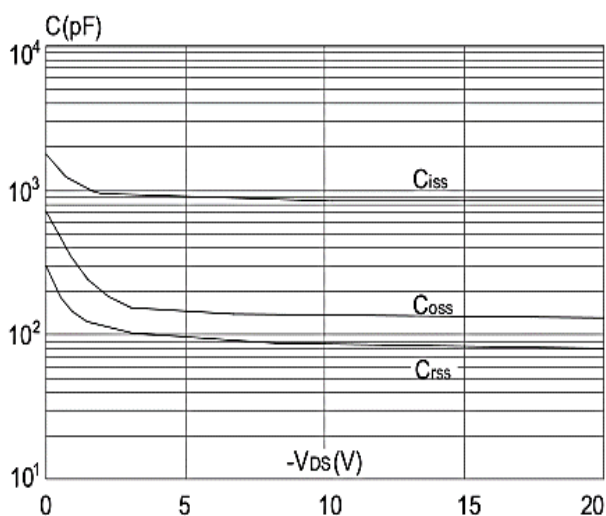
**Figure 5: Gate Charge Characteristics**



**Figure 2: Typical Transfer Characteristics**



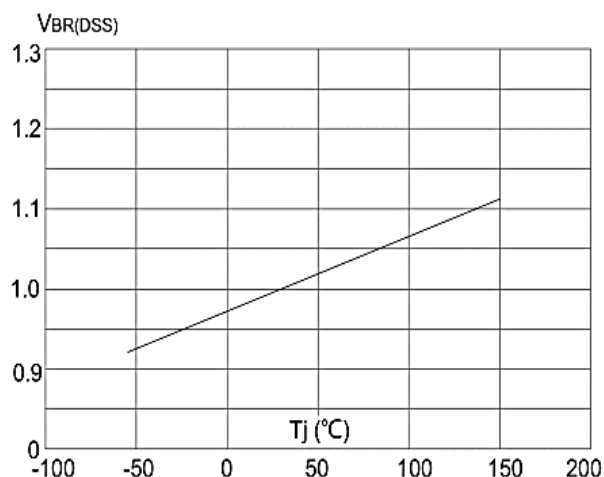
**Figure 4: Body Diode Characteristics**



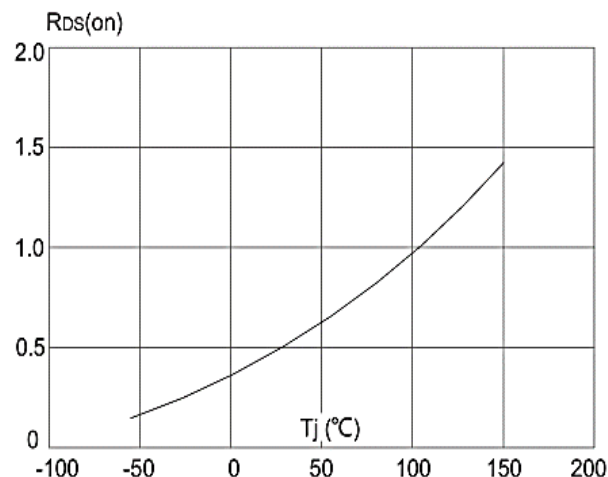
**Figure 6: Capacitance Characteristics**



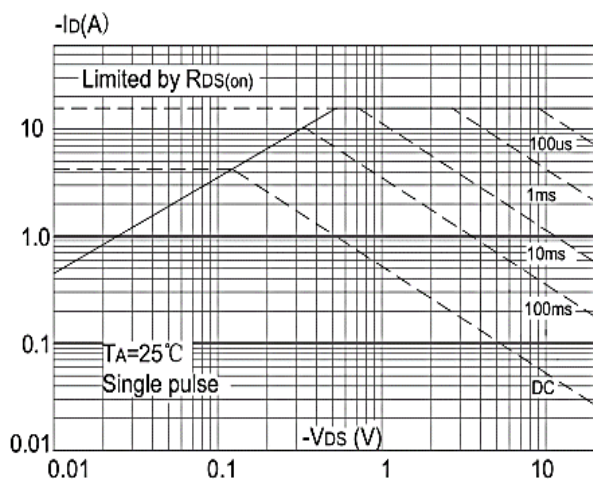
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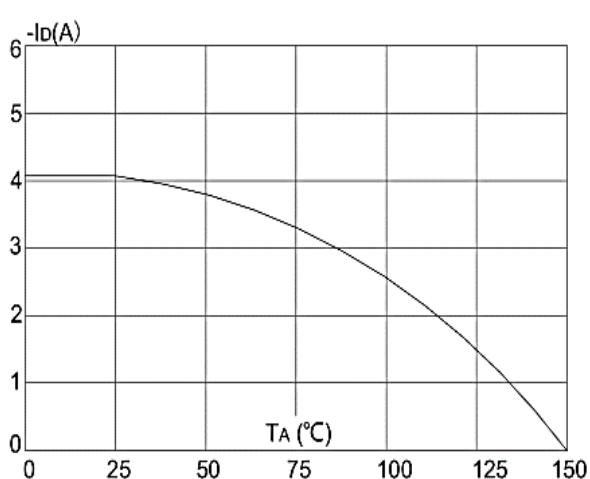
**Figure 7: Normalized Breakdown Voltage vs. Junction Temperature**



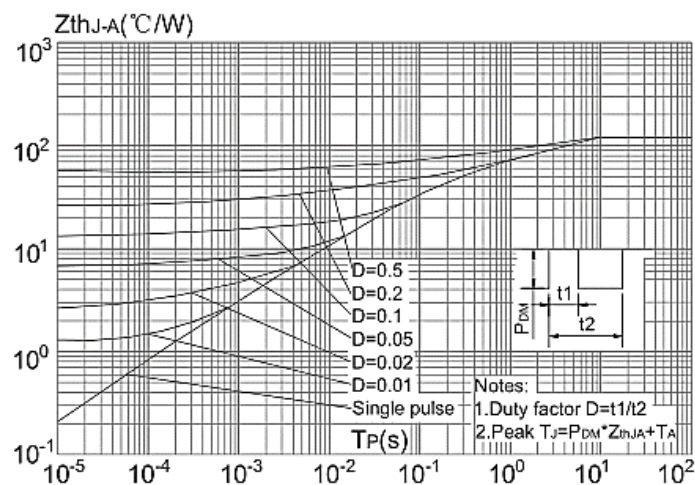
**Figure 8: Normalized on Resistance vs. Junction Temperature**



**Figure 9: Maximum Safe Operating Area**

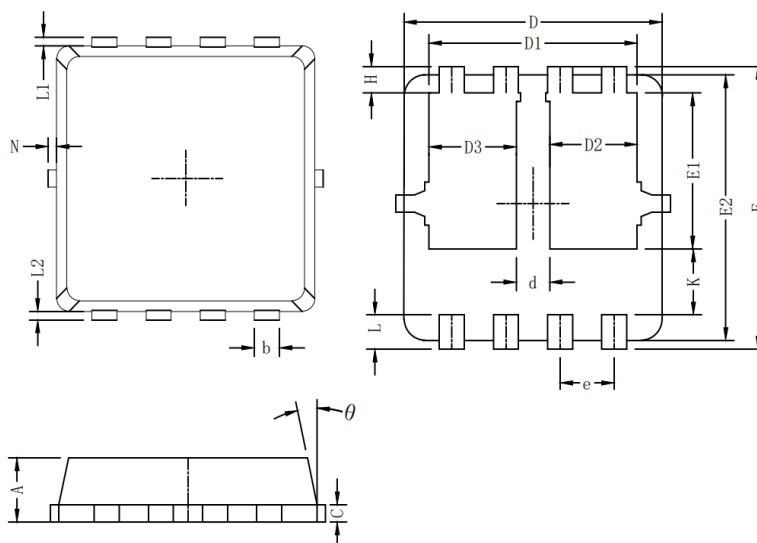


**Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature**



**Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient**

**Package Mechanical Data-PDFN3\*3-8L-Double**



Symbol	Dim in mm		
	Min	Typ	Max
A	0.6	0.75	0.9
b	0.2	0.3	0.4
C	0.15	0.2	0.25
D	3	3.1	3.2
D1	2.3	2.45	2.6
D2/D3	0.8	1	1.2
E	3.15	3.3	3.45
E1	1.43	1.73	1.93
E2	2.9	3.05	3.2
e	0.65BSC		
H	0.2	0.35	0.5
K	0.57	0.77	0.87
L	0.3	0.4	0.5
L1/L2	0.1REF		
θ	8°	10°	13°
N	0		0.15
d	0.3	0.4	0.5



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Edition	Date	Change
REV1.0	2024/1/21	Initial release

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