

100V N+N-Channel Enhancement Mode MOSFET

Description

The AP15H10S uses advanced **APM-SGT I I** technology

to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 100V$ $I_D = 15A$

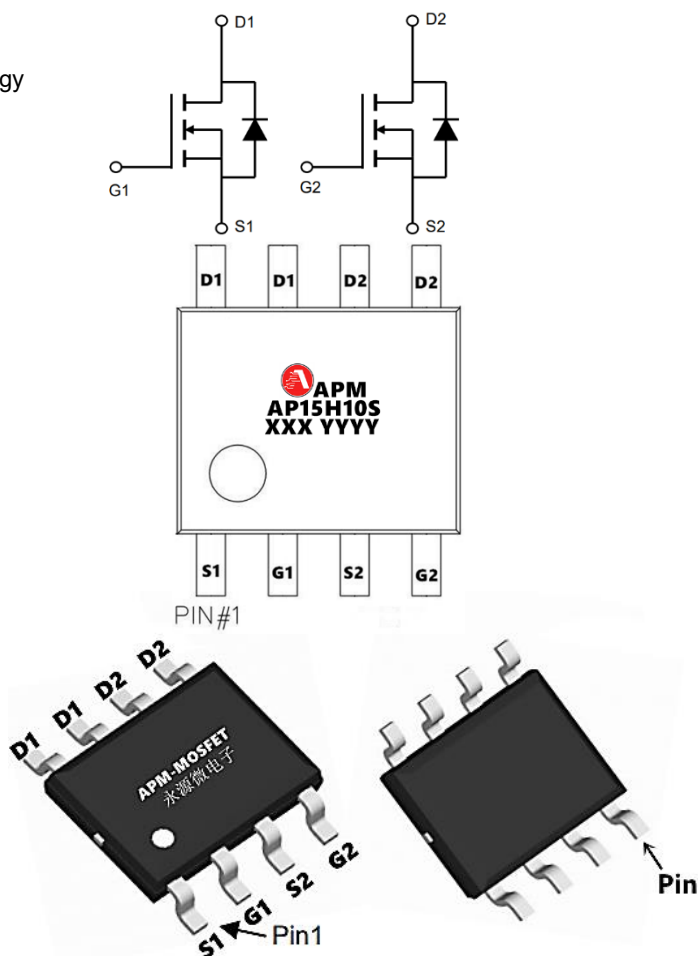
$R_{DS(ON)} < 53m\Omega$ @ $V_{GS}=10V$ (Type: **43mΩ**)

Application

DC/DC Converter

LED Backlighting

Power Management Switches



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP15H10S	SOP-8L	AP15H10S XXX YYYY	3000

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_c=25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	15	A
$I_D@T_c=100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	10	A
IDM	Pulsed Drain Current	60	A
EAS	Single Pulse Avalanche Energy	14.5	mJ
IAS	Avalanche Current	8.5	A
$P_D@T_c=25^\circ\text{C}$	Total Power Dissipation ⁴	35.7	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	3.5	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case	62	$^\circ\text{C/W}$

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Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	108	-	V
IDSS	Drain-Source Leakage Current	$V_{DS}=80V, V_{GS}=0V$	-	-	1	μA
IGSS	Gate to Body Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 100	nA
VGS(th)	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.7	2.5	V
RDS(on)	Static Drain-Source On-Resistance	$V_{GS}=10V, I_D=15A$	-	43	53	m Ω
		$V_{GS}=4.5V, I_D=10A$	-	60	80	m Ω
gfs	Forward Threshold Voltage	$V_{DS}=10V, I_D=20A$	-	7.5	-	S
Rg	Gate Resistance	$V_{DS}=V_{GS}=0V, f=1.0\text{MHz}$	-	1.75	-	Ω
Ciss	Input Capacitance	$V_{DS}=50V, V_{GS}=0V, f=1.0\text{MHz}$	-	390	-	pF
Coss	Output Capacitance		-	94	-	pF
Crss	Reverse Transfer Capacitance		-	3.3	-	pF
Qg	Total Gate Charge	$V_{DS}=50V, I_D=10A, V_{GS}=10V$	-	8.2	-	nC
Qgs	Gate-Source Charge		-	1.4	-	
Qgd	Gate-Drain("Miller") Charge		-	2.1	-	
td(on)	Turn-On Delay Time	$V_{DS}=50V, I_D=10A, R_G=3\Omega, V_{GS}=10V$	-	4.2	-	ns
tr	Turn-On Rise Time		-	4.9	-	
td(off)	Turn-Off Delay Time		-	13	-	
tr	Turn-Off Fall Time		-	4.8	-	
Is	Continuous Source Current		-	-	25	A
VSD	Diode Forward Voltage	$I_S=10A, V_{GS}=0V$	-	0.75	1.2	V
trr	Reverse Recovery Time	$I_{SD}=10A, dI_{SD}/dt=100A/\mu s$	-	2.2	-	ns
Qrr	Reverse Recovery Charge		-	34.4	-	nC

Notes:

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3、The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.5mH, I_{AS}=8.5A$
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

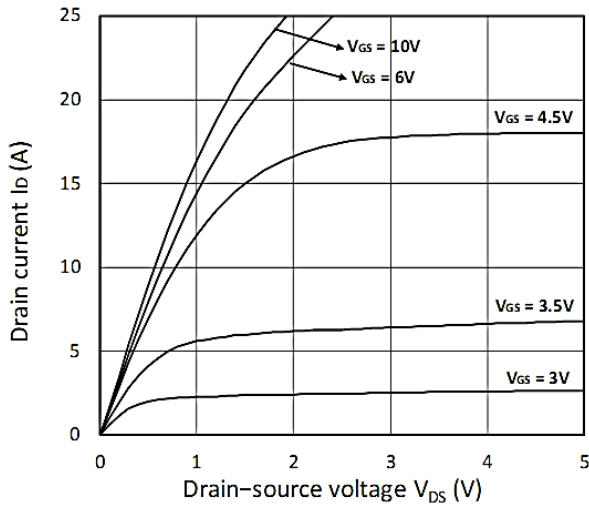


Figure 1. Output Characteristics

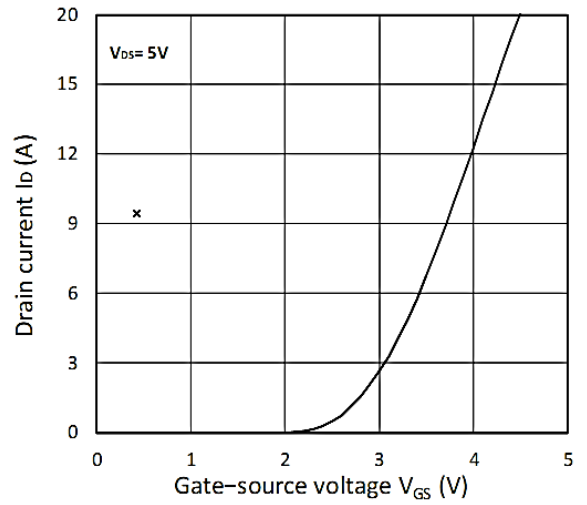


Figure 2. Transfer Characteristics

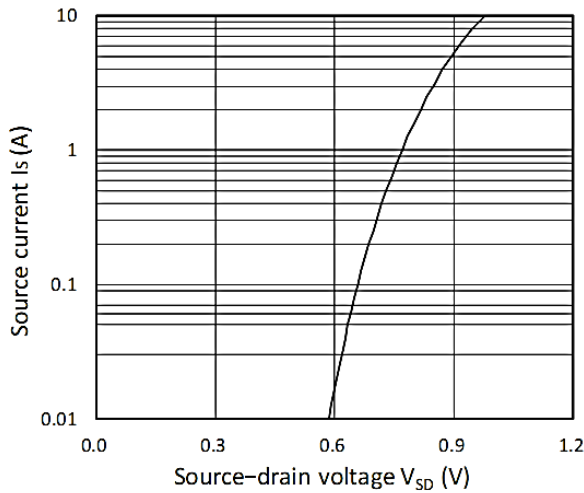


Figure 3. Forward Characteristics of Reverse

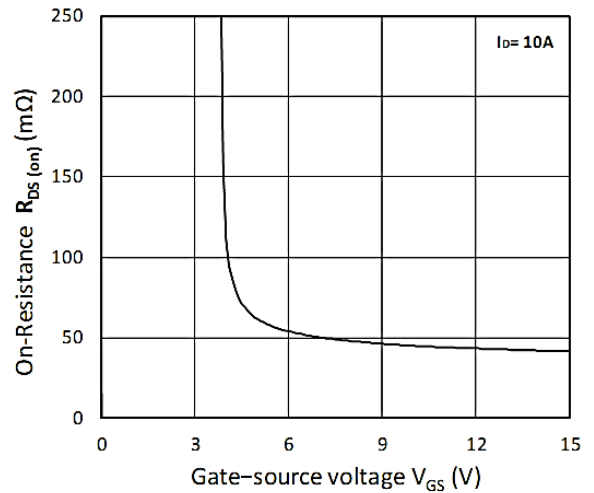


Figure 4. R_DS(ON) vs. V_GS

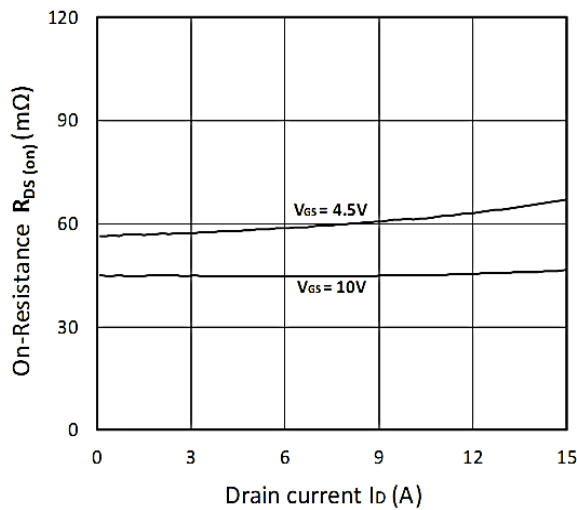


Figure 5. R_DS(ON) vs. I_D

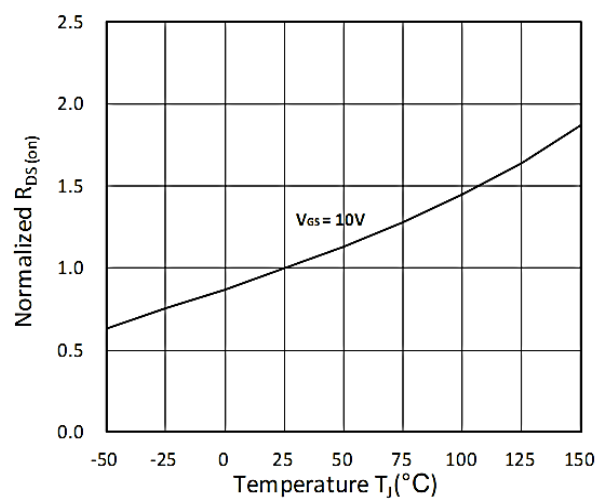


Figure 6. Normalized R_DS(on) vs. Temperature



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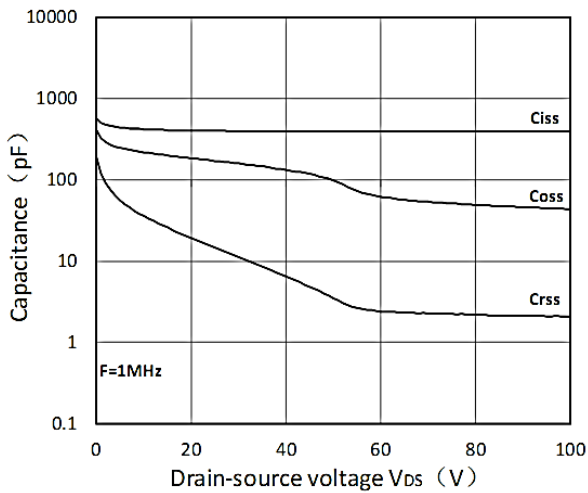


Figure 7. Capacitance Characteristics

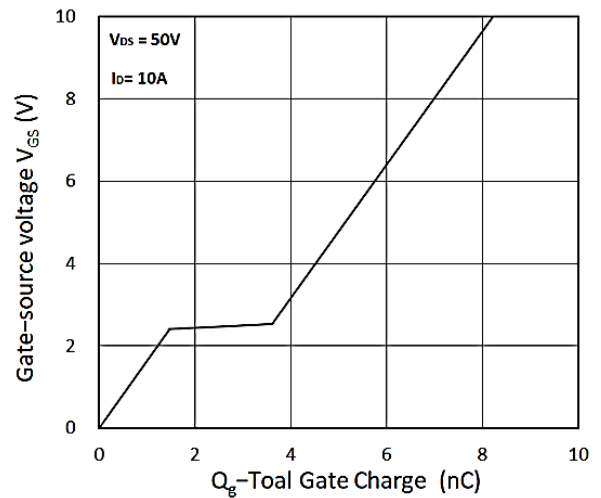


Figure 8. Gate Charge Characteristics

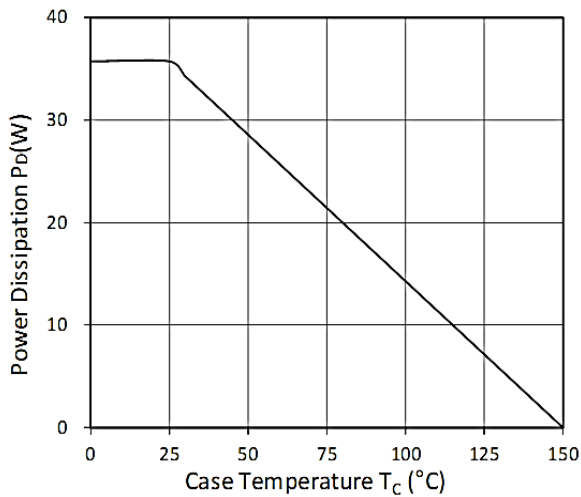


Figure 9. Power Dissipation

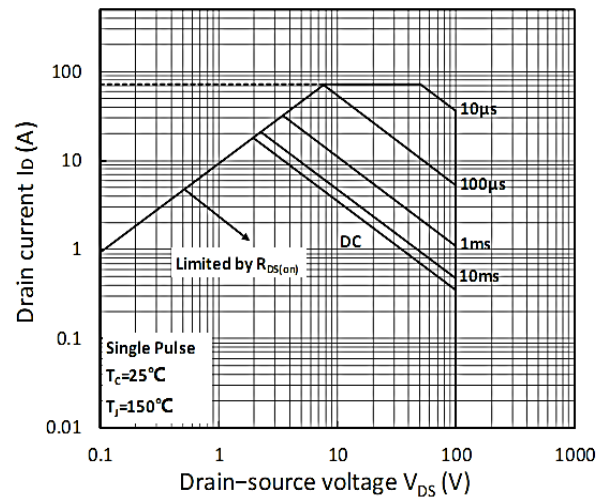


Figure 10. Safe Operating Area

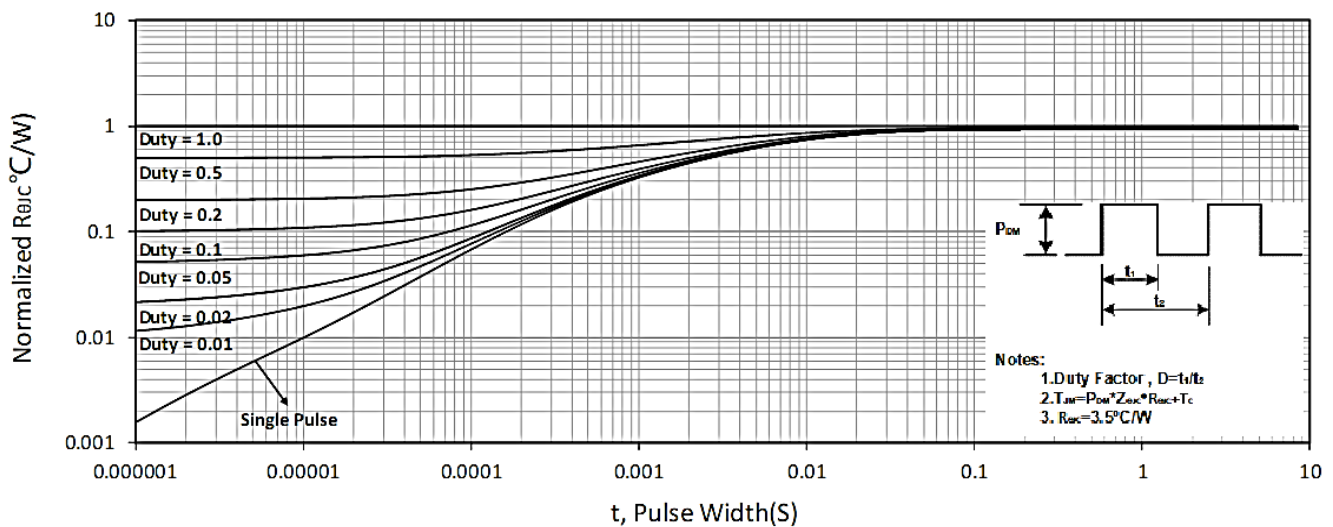
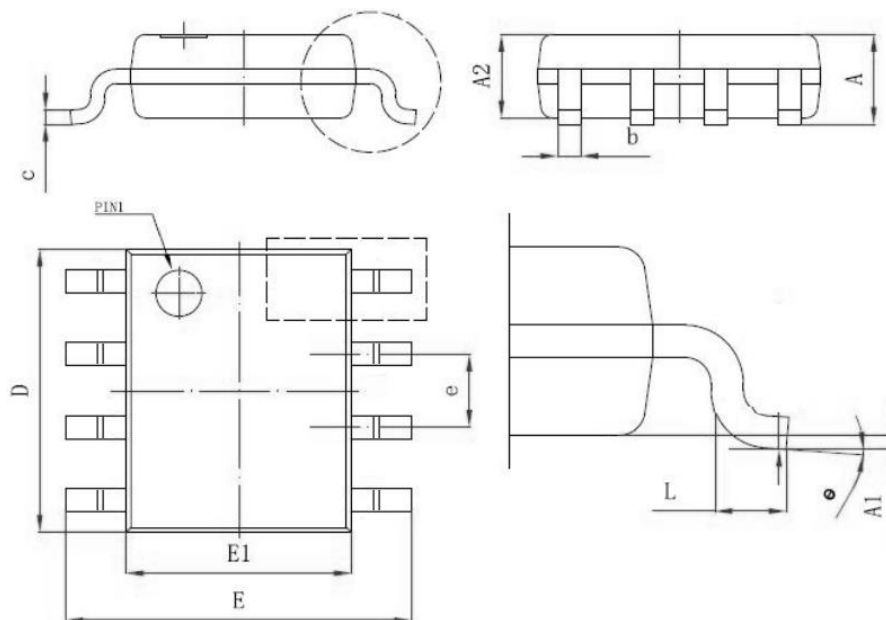


Figure 9 Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-SOP-8L



Symbol	Dim in mm		
	Min	Typ	Max
A	1.35	1.55	1.75
A1	0.02	0.15	0.25
A2	1.425	1.45	1.475
b	0.3	0.4	0.5
c	0.15	0.2	0.25
D	4.8	5	5.2
E	5.8	6	6.2
E1	3.8	4	4.2
e	1.27BSC		
L	0.4		1.27
θ	0°		8°

100V N+N-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
REV1.0	2023/11/10	Initial release

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