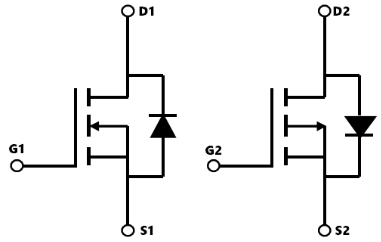
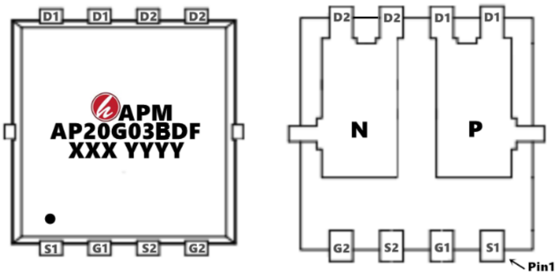
AP20G03BDF

30V N+P-Channel Enhancement Mode MOSFET

Description

The AP20G03BDF uses advanced **Trench III** technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.





General Features

V_{DS} = 30V I_D =20A

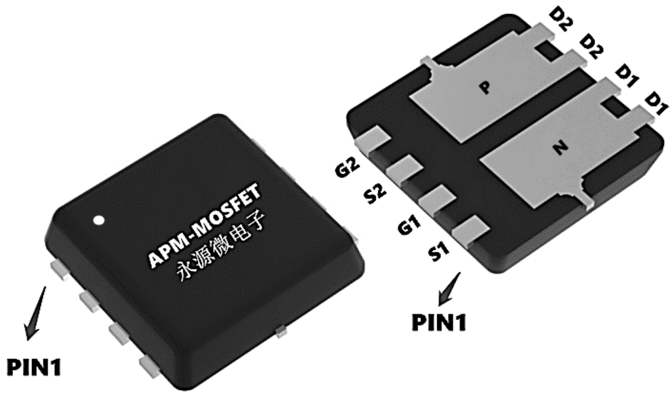
$R_{DS(ON)}$ <12mΩ @ V_{GS}=4.5V （**Type：8.5mΩ**）

V_{DS} = -20V I_D =-18.8A

$R_{DS(ON)}$ < 30mΩ @ V_{GS}=-4.5V（**Type：25mΩ**）

Application

High Frequency Circuit
low-power consumption



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP20G03BDF	PDFN3*3-8L	AP20G03BDF XXX YYYY	5000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
VDS	Drain-Source Voltage	30	-30	V
VGS	Gate-Source Voltage	±12	±12	V
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	20	-18.8	A
I_D@T_A=70℃	Continuous Drain Current, V_{GS} @ 10V[1]	16.2	-15.5	A
IDM	Pulsed Drain Current[2]	60	-54	A
EAS	Single Pulse Avalanche Energy[3]	85	78	mJ
P_D@T_A=25℃	Total Power Dissipation[4]	3.5	3.5	W
TSTG	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃
$R_{\theta}JA$	Thermal Resistance Junction-Ambient [1]	105		℃/W
$R_{\theta}JC$	Thermal Resistance Junction-Case[1]	50		℃/W

P-Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	VGS=0V, ID=250μA	30	-	-	V
IGSS	Gate-body Leakage current	VDS=0V, VGS=±12V	-	-	±100	nA
IDSS	Zero Gate Voltage Drain Current	VDS=30V, VGS=0V	-	-	1	μA
VGS(th)	Gate-Threshold Voltage	VDS=VGS, ID=250μA	0.5	0.75	1.2	V
RDS(on)	Drain-Source on-Resistance4	VGS=10V, ID=4A	-	7.5	10	mΩ
		VGS=4.5V, ID=3A	-	8.5	12	
		VGS=2.5V, ID=3A	-	11	22	
Ciss	Input Capacitance	VDS=15V, VGS=0V, f=1.0MHz	-	1850	-	pF
Coss	Output Capacitance		-	150	-	
Crss	Reverse Transfer Capacitance		-	124	-	
Rg	Gate Resistance	f=1MHz	-	3.2	-	Ω
Qg	Total Gate Charge	VGS=4.5V, VDS=15V, ID=10A	-	10	-	nC
Qgs	Gate-Source Charge		-	3.5	-	
Qgd	Gate-Drain Charge		-	2.2	-	
td(on)	Turn-on Delay Time	VGS=4.5V, VDD = 15V, ID=10A, RG = 3Ω	-	8	-	ns
tr	Rise Time		-	28	-	
td(off)	Turn-off Delay Time		-	15	-	
tf	Fall Time		-	7	-	
VSD	Diode Forward Voltage4	IS=1A, VGS = 0V	-	-	1.2	V
IS	Continuous Source Current TA=25°C				12.5	A

Note :

1、The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The power dissipation is limited by 150℃ junction temperature

4、The EAS data shows Max. rating . The test condition is V_{DD}=18V,RG=25Ω V_{GS}=4.5V,L=0.1mH,I_{AS}=11A

5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

P-Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	VGS = 0V, ID = -250μA	-30	-	-	V
IGSS	Gate-body Leakage current	VDS = 0V, VGS = ±20V	-	-	±100	nA
IDSS	Zero Gate Voltage Drain Current TJ=25°C	VDS = -30V, VGS = 0V	-	-	-1	μA
	Zero Gate Voltage Drain Current TJ=100°C		-	-	-100	
VGS(th)	Gate-Threshold Voltage	VDS = VGS, ID = -250μA	-0.7	-1.1	-1.5	V
RDS(on)	Drain-Source on-Resistance4	VGS = -10V, ID = -5A	-	18	25	mΩ
		VGS = -4.5V, ID = -3A	-	25	32	
		VGS = -4.5V, ID = -3A		52	65	
gfs	Forward Transconductance4	VDS = -10V, ID = -5A	-	13	-	S
Ciss	Input Capacitance	VDS = -15V, VGS =0V, f =1MHz	-	1005	-	pF
Coss	Output Capacitance		-	137	-	
Crss	Reverse Transfer Capacitance		-	113	-	
RG	Gate Resistance	f =1MHz	-	10	-	Ω
Qg	Total Gate Charge	VGS = -10V, VDS = -15V, ID= -5A	-	20	-	nC
Qgs	Gate-Source Charge		-	3	-	
Qgd	Gate-Drain Charge		-	5.5	-	
td(on)	Turn-on Delay Time	VGS = -10V, VDD = -15V, ID= -5A, RG= 3Ω	-	7.5	-	ns
tr	Rise Time		-	16	-	
td(off)	Turn-off Delay Time		-	49	-	
tf	Fall Time		-	32	-	
trr	Body Diode Reverse Recovery Time	IF = -5A, dIF/dt = 100A/μs	-	21	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	12.5	-	nC
VSD	Diode Forward Voltage4	IS = -5A, VGS = 0V	-	-	-1.2	V
IS	Continuous Source Current	TA=25°C	-	-	-7	A

Note :

1、The data tested by surface mounted on a 1 $inch^2$ FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The power dissipation is limited by 150℃ junction temperature

4、The EAS data shows Max. rating . The test condition is V_{DD}=18V,RG=25Ω V_{GS}=4.5V,L=0.1mH,I_{AS}=18A

5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Typical Characteristics

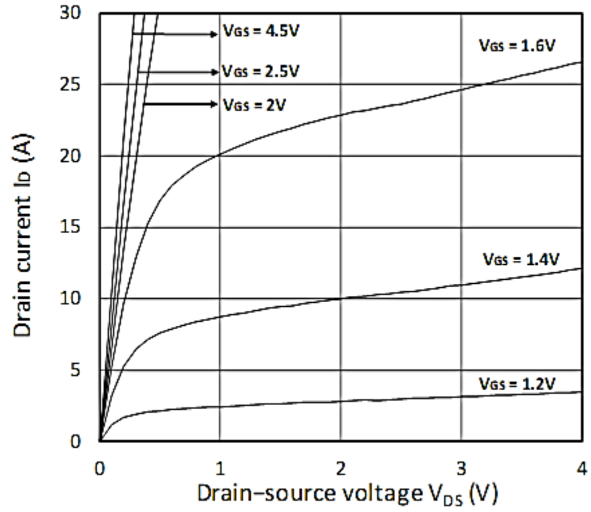


Figure 1. Output Characteristics

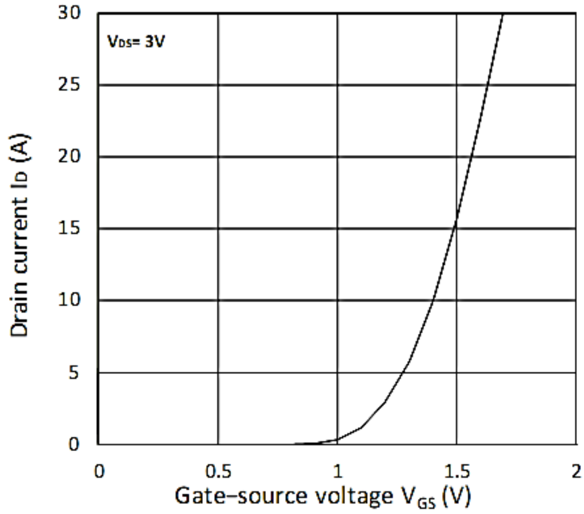


Figure 2. Transfer Characteristics

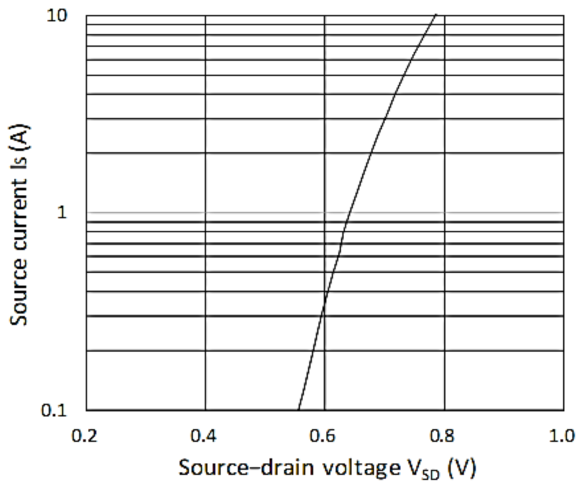


Figure 3. Forward Characteristics of Reverse

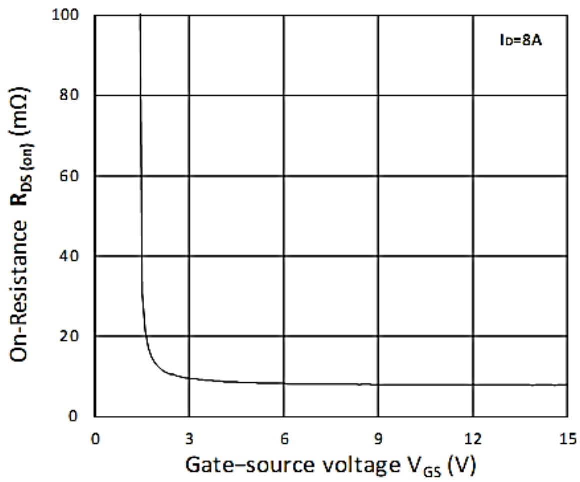


Figure 4. RDS(ON) vs. VGS

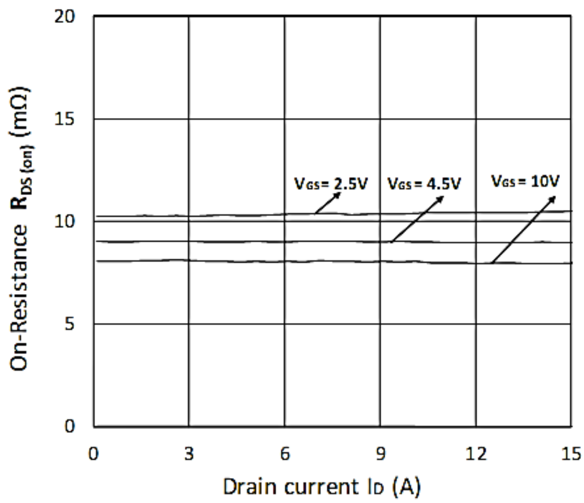


Figure 5. RDS(ON) vs. ID

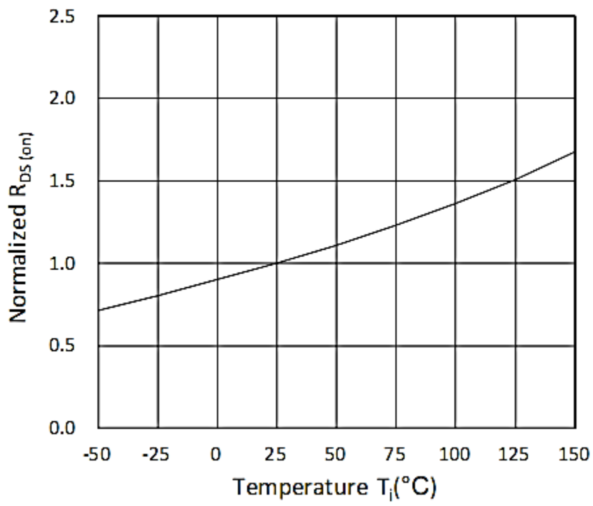


Figure 6. Normalized R DS(on) vs. Temperature

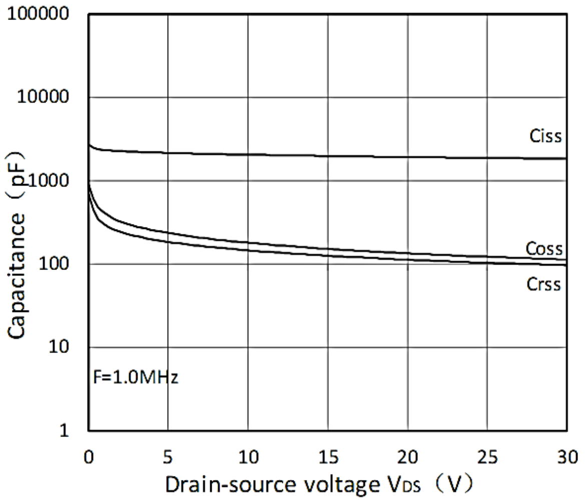


Figure 7. Capacitance Characteristics

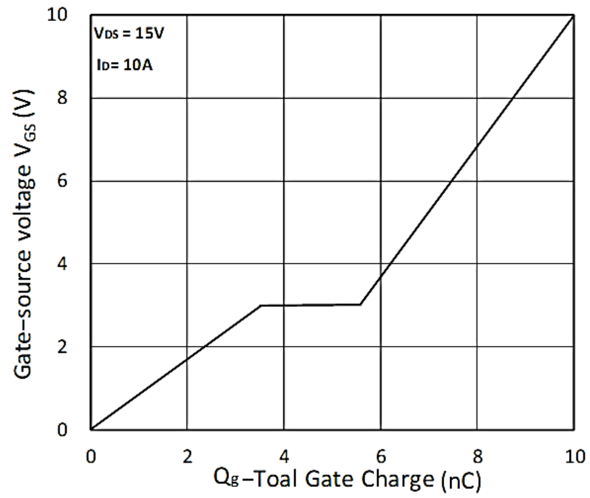


Figure 8. Gate Charge Characteristics

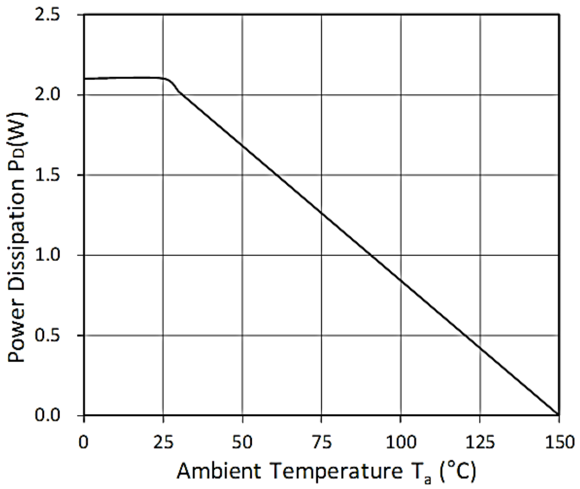


Figure 9. Power Dissipation

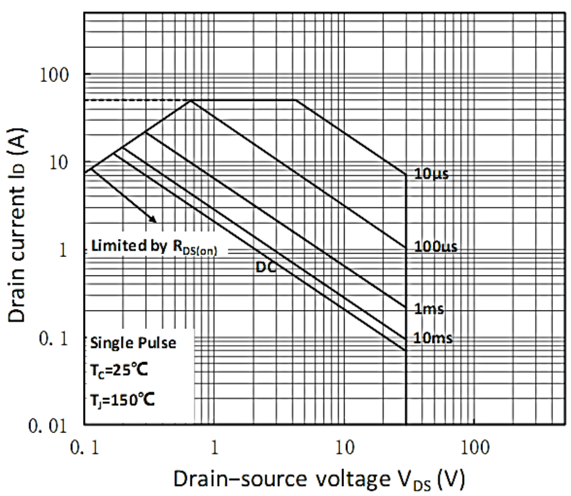


Figure10. Safe Operating Area

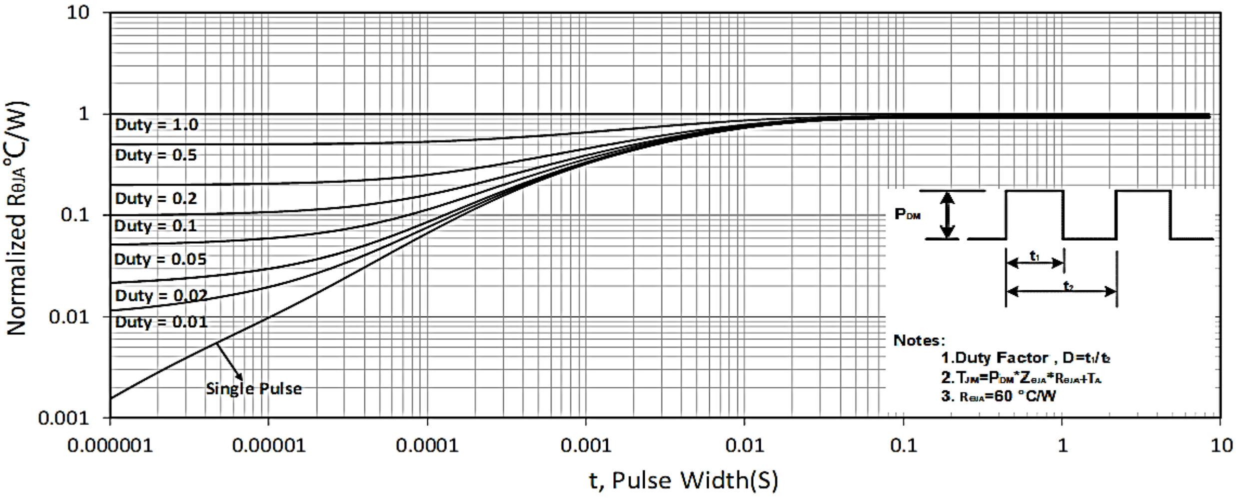


Figure 11. Normalized Maximum Transient Thermal Impedance

P-Typical Characteristics

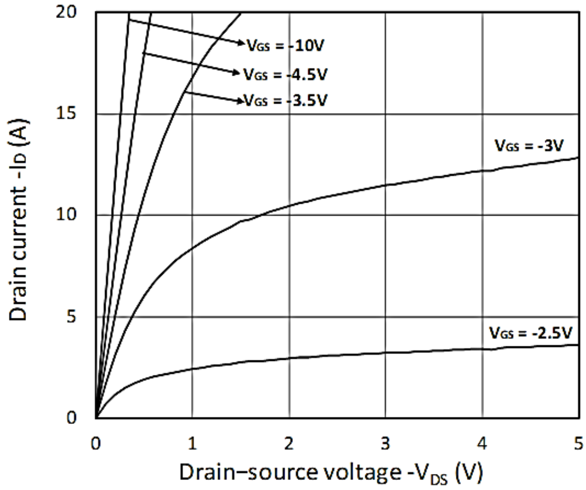


Figure 1. Output Characteristics

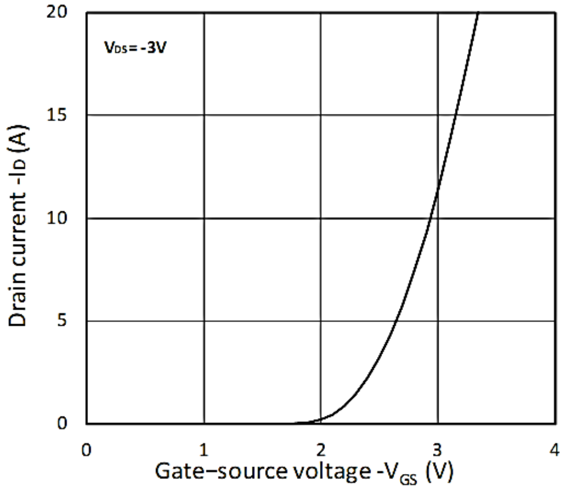


Figure 2. Transfer Characteristics

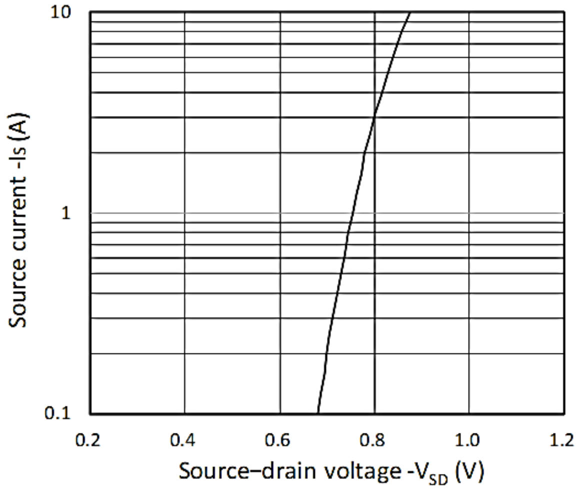


Figure 3. Forward Characteristics of Reverse

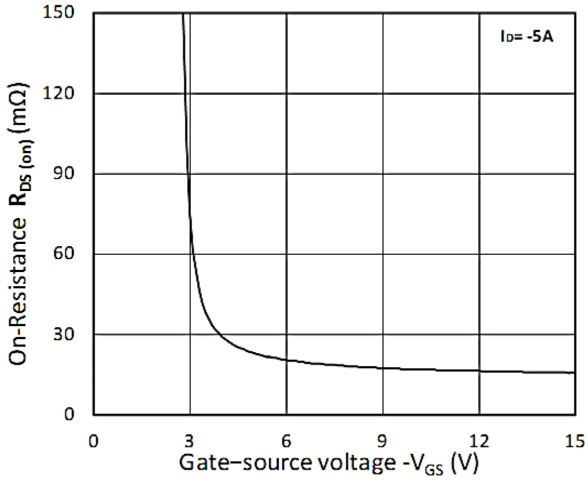


Figure 4. RDS(ON) vs. VGS

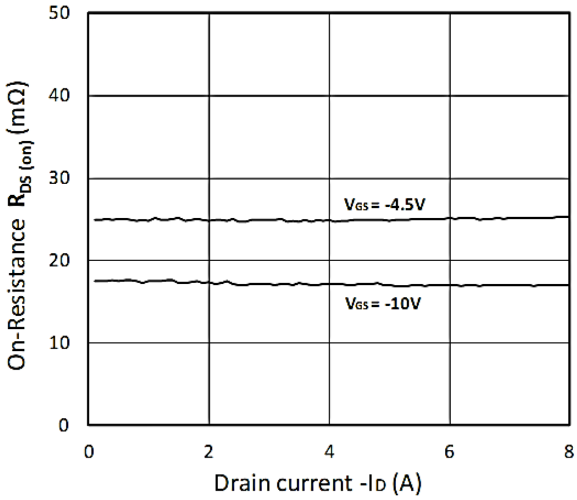


Figure 5. RDS(ON) vs. ID

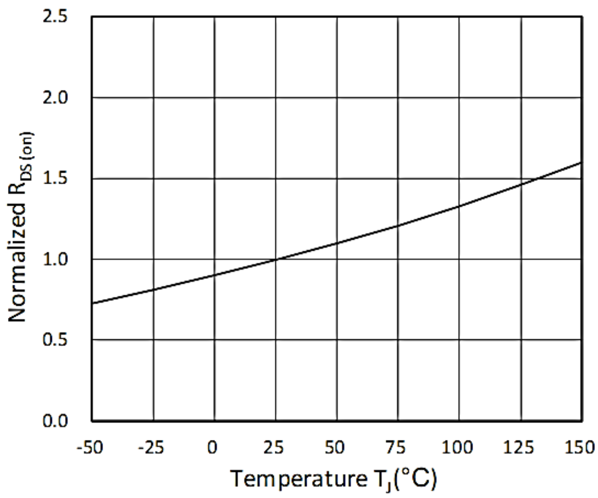


Figure 6. Normalized RDS(on) vs. Temperature

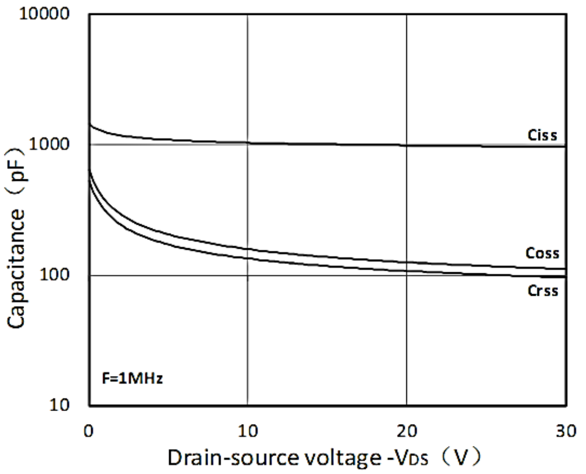


Figure 7. Capacitance Characteristics

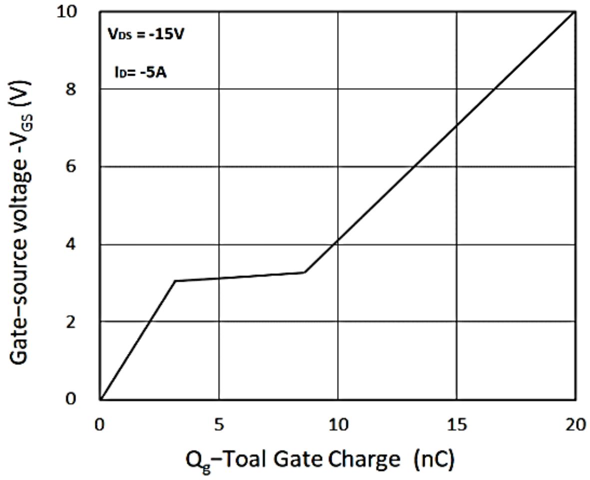


Figure 8. Gate Charge Characteristics

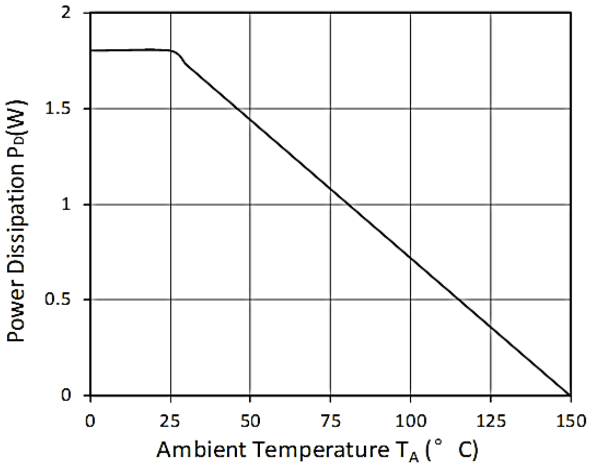


Figure 9. Power Dissipation

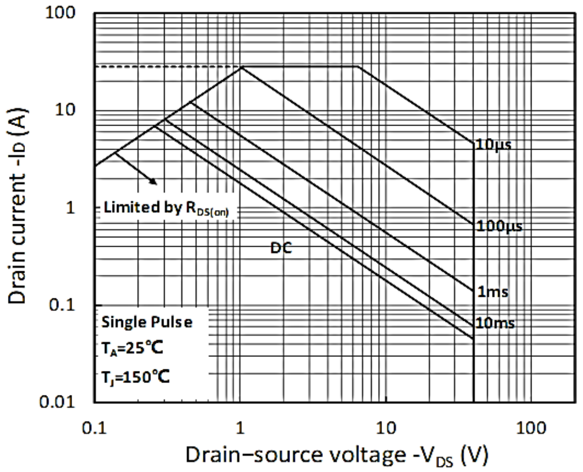


Figure10. Safe Operating Area

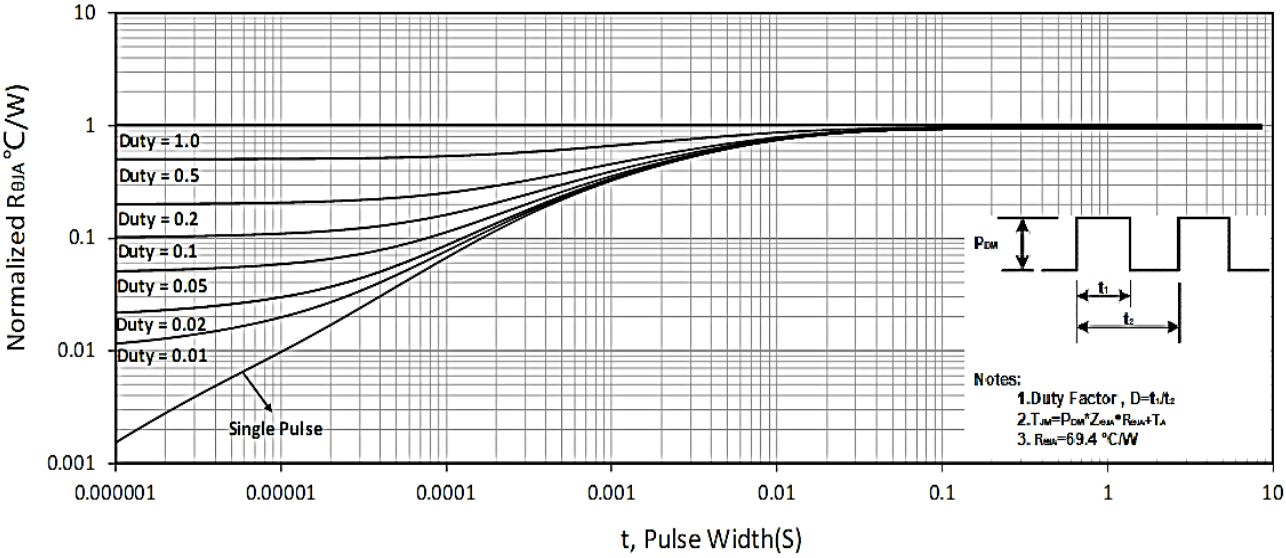
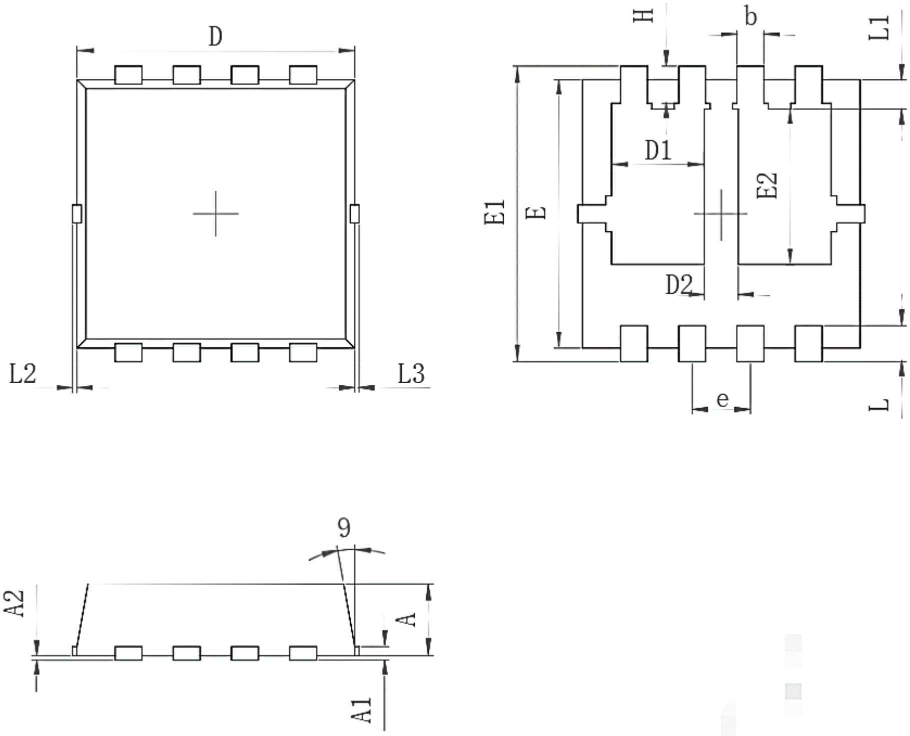
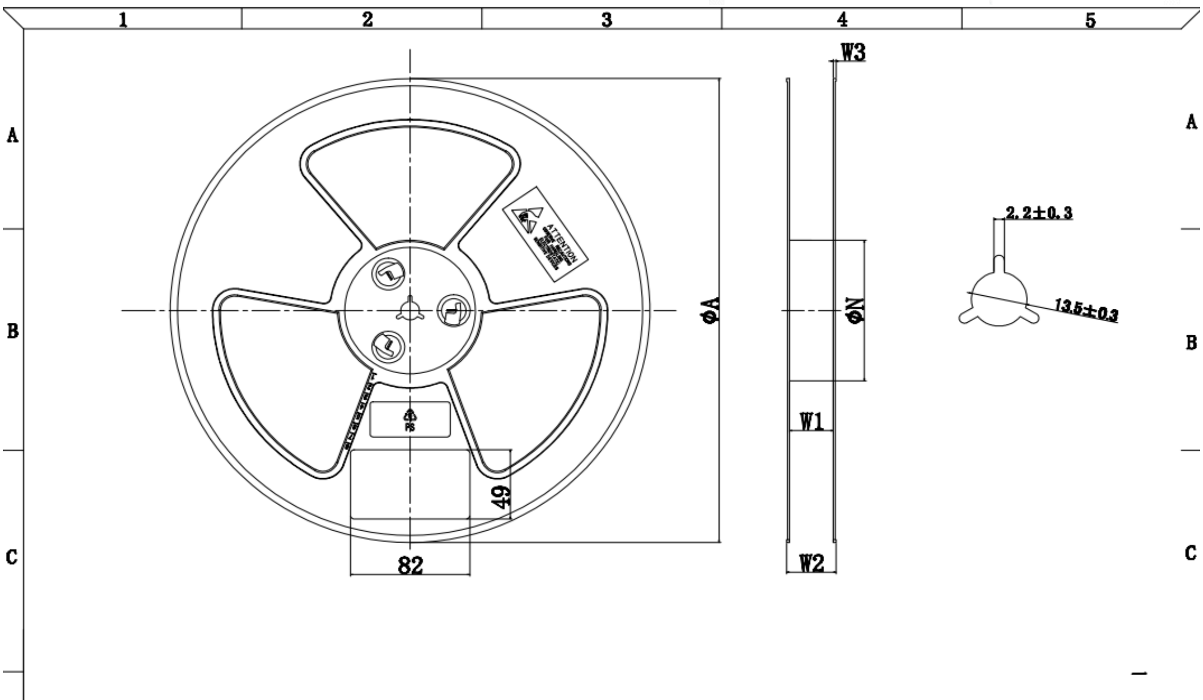


Figure11, Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-PDFN3*3-8L Double



SYMBOL	MILLIMETER	
	MIN	MAX
A	0.700	0.900
A1	0.152 REF.	
A2	0~0 05	
D	3.000	3.200
D1	0.935	1.135
D2	0.280	0.480
E	2.900	3.100
E1	3.150	3.450
E2	1.535	1.935
b	0.200	0.400
e	0.550	0.750
L	0.300	0.500
L1	0.180	0.480
L2	0~0.100	
L3	0~0 100	
H	0.315	0.515
9	8°	12°



名称	ΦA	ΦN	W1	W2	W3
13*12	330±2	100±2	12.4^{+2}_{-0}	16±1	1.8±0.3
13*16	330±2	100±2	16.4^{+2}_{-0}	20±1	1.8±0.3
13*24	330±2	100±2	24^{+2}_{-0}	28±1	1.8±0.3
13*32	330±2	100±2	32.4^{+2}_{-0}	36±1	1.8±0.3
13*44	330±2	100±2	44^{+2}_{-0}	48±1	1.8±0.3

注意：
1. 材料：聚苯乙烯
2. 平整度：最大允许3毫米
3. 所有尺寸为毫米
4. 表面电阻：$10^{5}-10^{11}$ Ω
5. 所有未注公差±0.25

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Edition	Date	Change
REV1.0	2023/3/21	Initial release