Description

The AP220309 is a 7mΩ, 4A load switch that switches a power rail ranging from 0.9V to 4.5V. It contains protection features for enhanced operation and reliability.

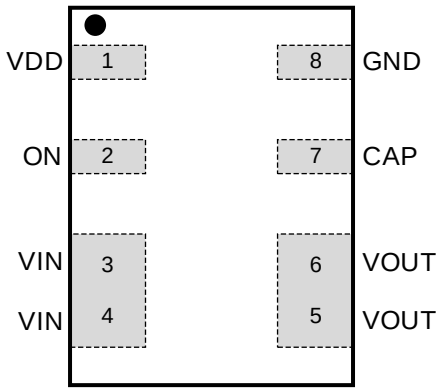
The device is packaged in the small 2.0mm x 1.5mm U-DFN2015-8 (Type AX) package.

Features

- Operating Voltage: 2.5V to 5.5V
- Operating Temperature: -20°C to +70°C
- 2.0mm x 1.5mm x 0.55mm U-DFN2015-8 (Type AX) Package
- Nominally Supports up to I_{OUT} = 4A
- Two Overcurrent Protection Modes
  - Short-Circuit Current Limit
  - Active Current Limit
- Overtemperature Protection
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Pin Assignments

(Top View)



U-DFN2015-8
(Type AX)

Applications

- Smartphones
- Tablets
- Notebooks

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Application Circuit

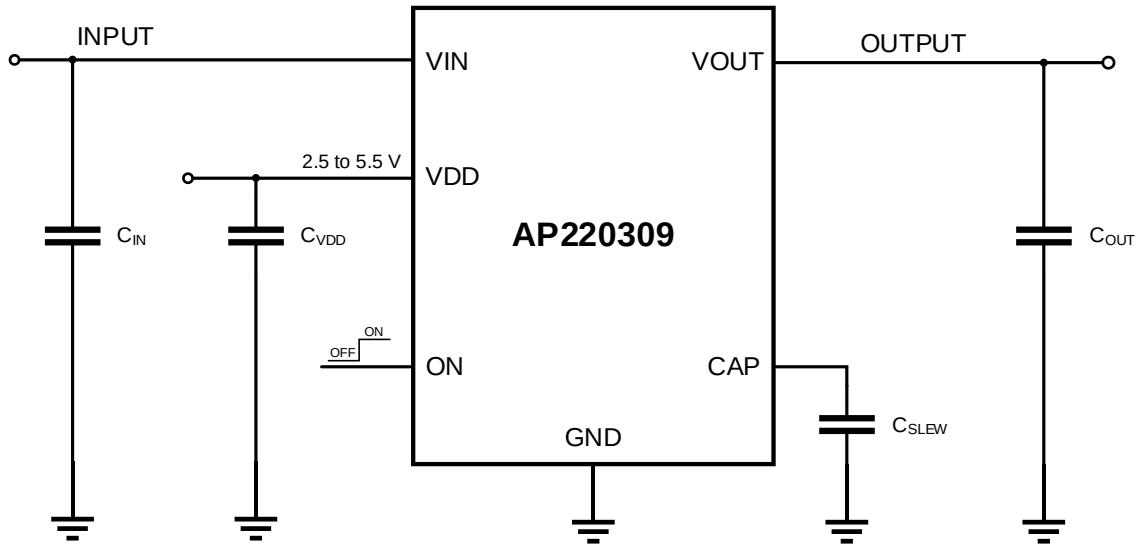


Figure 1. Typical AP220309 Application Circuit

Pin Descriptions

Pin Name	Pin Number	Type	Function
VDD	1	Power	Power supply. Assumes a 0.1µF or larger decoupling capacitor.
ON	2	Input	Turns on load switch, active High. There is an internal pulldown circuit to GND (up to 5MΩ).
VIN	3 – 4	MOSFET	Drain terminal connection for the load switch. Connect at minimum a low-ESR 10µF capacitor from this pin to GND.
VOUT	5 – 6	MOSFET	Source terminal connection for the load switch. Connect a low-ESR capacitor from this pin to GND.
CAP	7	Input	Connects to a low-ESR ceramic capacitor to set the V_{OUT} slew rate.
GND	8	GND	Ground.

Functional Block Diagram

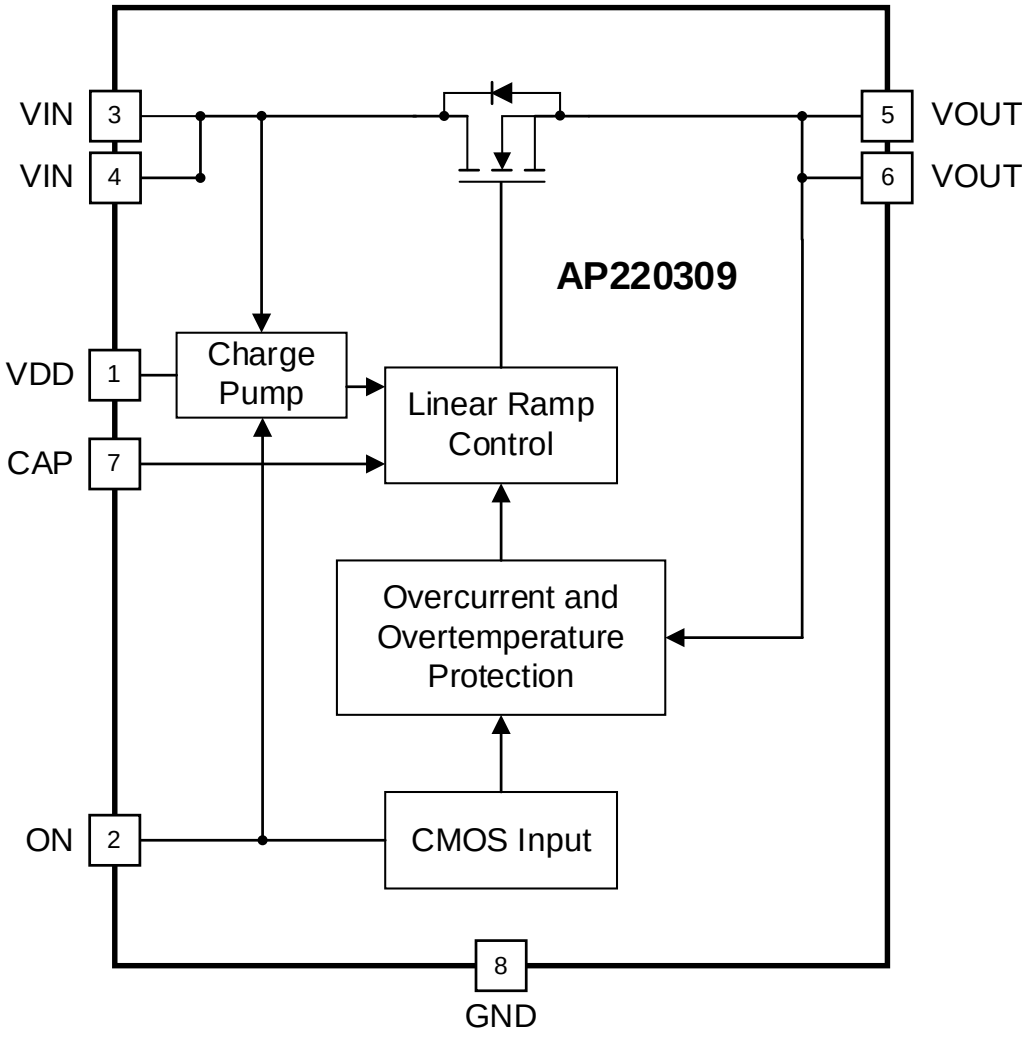


Figure 2. Functional Block Diagram

Absolute Maximum Ratings (Note 4) (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
V_{DD}	Power Supply	+7	V
W_{DIS}	Package Power Dissipation	1 (Target)	W
MOSFET $I_{OUT(PK)}$	Peak Current from Drain to Source	+6 (For no more than 1ms with 1% duty cycle)	A
T_{ST}	Storage Temperature	-65 to +150	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Model, per JEDEC Standard	±2000	V

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
5. Semiconductor devices are ESD sensitive and can be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Recommended Operating Conditions (Note 6) (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	2.5	5.5	V
V_{IN}	Input Voltage	0.9	4.5 ($V_{IN} \le V_{DD}$)	V
T_A	Operating Ambient Temperature	-20	+70	°C
I_{OUT}	Output Current (Continuous)	0	4	A
V_{IH}	ON Pin High Input Voltage	0.85	V_{DD}	V
V_{IL}	ON Pin Low Input Voltage	-0.3	0.4	V

Note: 6. The device performance is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics (@ T_A = -20°C to +70°C unless otherwise specified. Min/Max limits apply across the recommended operating and input voltage range, 2.5V to 5.5V, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{SHDN}	Input Shutdown Current	Disabled, I_{OUT} = 0A	—	—	100	nA
I_Q	Input Quiescent Current	Enabled, I_{OUT} = 0A	—	25	50	µA
RDSON	Switch On-Resistance	T_A = +25°C, I_{OUT} = 100mA	—	7.3	8.5	mΩ
		T_A = +70°C, I_{OUT} = 100mA	—	8.0	9.6	
		T_A = +85°C, I_{OUT} = 100mA	—	8.3	10.0	
t_{ON_Delay}	ON Delay Time	50% ON to V_{OUT} Ramp Start	—	230	500	µs
t_{ON}	Total Turn-On Time	50% ON to 90% V_{OUT}	Configurable (Note 7)			ms
		Example: V_{DD} = 5.5V, V_{IN} = 3.3V C_{SLEW} = 3.9nF, C_{OUT} = 10µF, R_{LOAD} = 20Ω	—	0.82	—	
$V_{OUT(SR)}$	Slew Rate	10% V_{OUT} to 90% V_{OUT}	Configurable (Note 7)			V/ms
		Example: V_{DD} = 5.5V, V_{IN} = 3.3V C_{SLEW} = 3.9nF, C_{OUT} = 10µF, R_{LOAD} = 20Ω	—	4.7	—	
C_{OUT}	Output Load Capacitance	C_{OUT} Connected from VOUT to GND	—	10	500	µF
I_{LIMIT}	Active Current Limit	V_{OUT} > 300mV	—	6.3	—	A
	Short-Circuit Current Limit	V_{OUT} < 300mV	—	0.5	—	
OTP	Overtemperature Protection	Threshold	—	+125	—	°C
		Hysteresis	—	+25	—	°C
		Shutoff Time	—	—	1	ms
t_{OFF_Delay}	OFF Delay Time	50% ON to V_{OUT} Fall Start V_{DD} = 5.5, V_{IN} = 3.3V, R_{LOAD} = 20Ω, No C_{OUT}	—	6	—	µs
$R_{Pulldown}$	ON Pulldown Resistance	V_{DD} = V_{ON} = 3.3V	—	5	—	MΩ

Note: 7. Refer to typical timing parameter vs. C_{SLEW} performance charts for additional information.

Typical Performance Characteristics (AP220309 @ T_A = +25°C unless otherwise specified.)

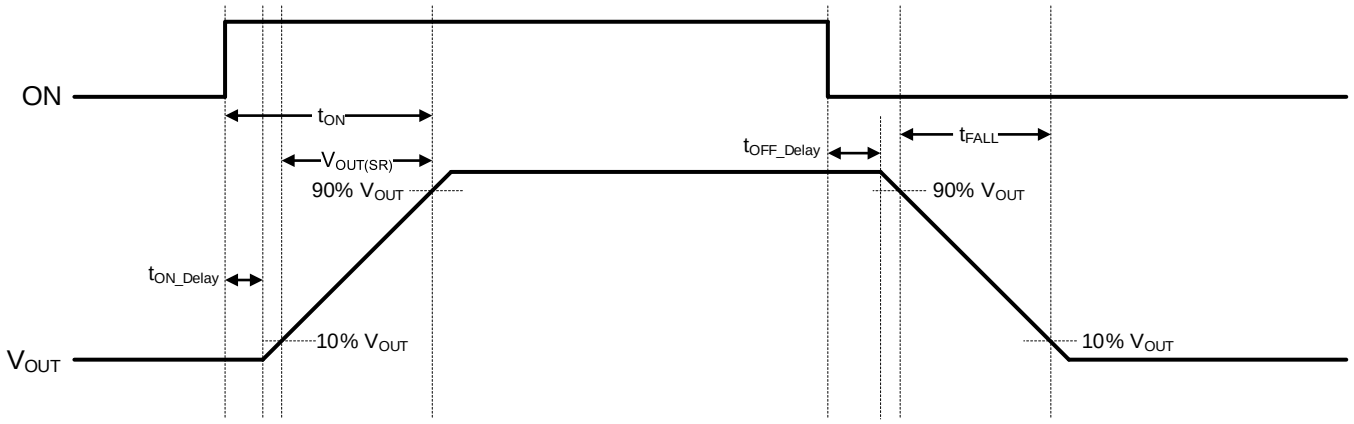


Figure 3. t_{ON_Delay}, $V_{OUT(SR)}$, and t_{ON} Timing Details

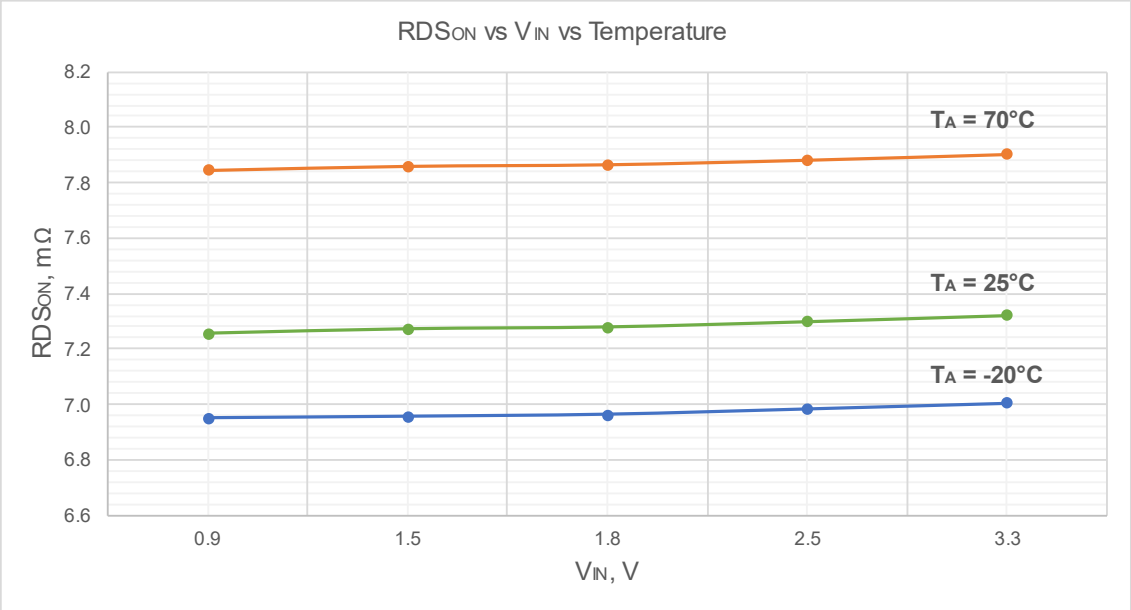


Figure 4. RDS_{ON} vs. V_{IN} and Temperature at V_{DD} = 3.3V and I_{OUT} = 100mA

Typical Performance Characteristics (AP220309 @ T_A = +25°C unless otherwise specified.) (continued)

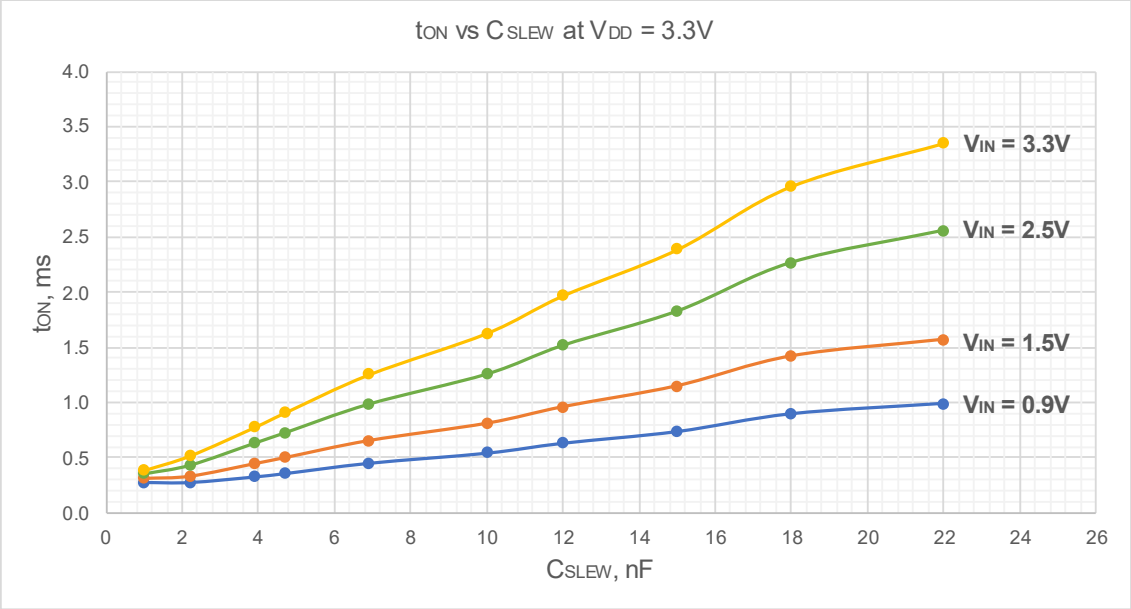


Figure 5. Total On Time vs. C_{SLEW} and V_{IN} at V_{DD} = 3.3V

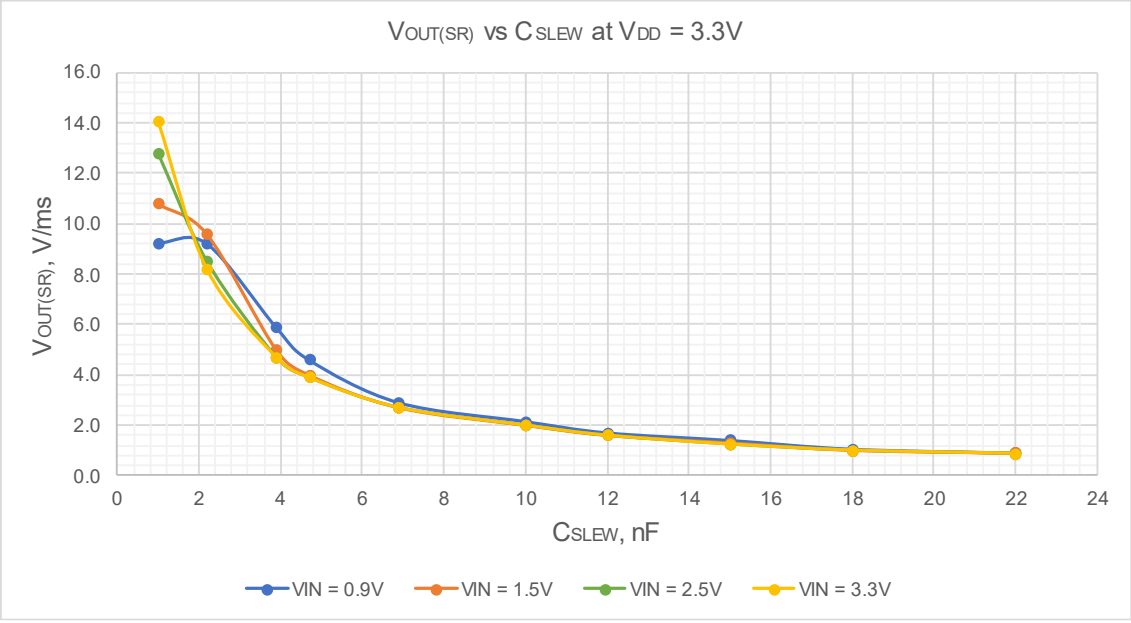


Figure 6. V_{OUT} Slew Rate vs. C_{SLEW} and V_{IN}

Application Information

1. Typical Operation

For correct operability per the AP220309 EC table, a proper power-up sequence must be applied. Apply V_{DD} first, followed by V_{IN}, then ON signal to power up the device. In order to control the inrush current from capacitive loads, set a desired linear output slew rate by placing a corresponding C_{SLEW} capacitor between CAP pin and GND. The greater the capacitor value at CAP pin, the slower the output ramp. Some typical operation waveforms are illustrated below.

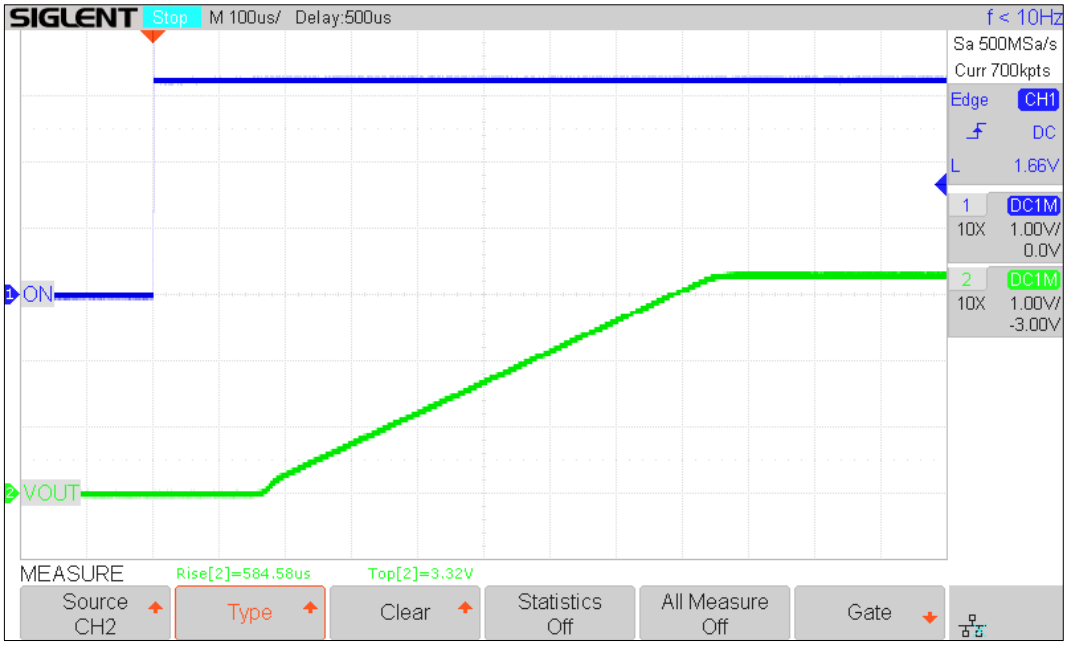


Figure 7. AP220309 Typical Power-Up Operation Waveform. V_{DD} = V_{IN} = 3.3V, R_{LOAD} = 20Ω, C_{OUT} = 10μF, C_{SLEW} = 3.9nF

Figure 8. AP220309 Typical Power-Down Operation Waveform. V_{DD} = V_{IN} = 3.3V, R_{LOAD} = 20Ω, C_{OUT} = 10μF, C_{SLEW} = 3.9nF

Application Information (continued)

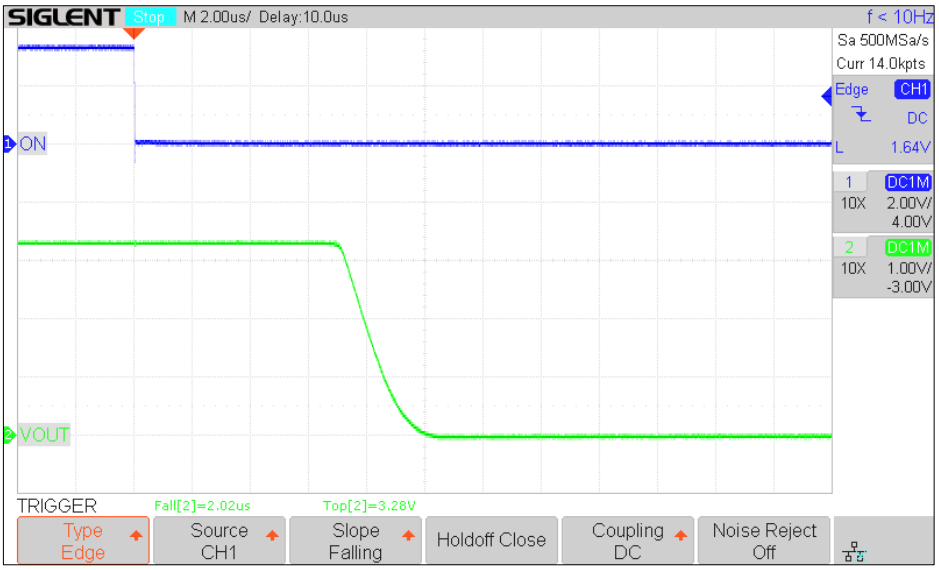


Figure 9. AP220309 Typical Power-Down Operation Waveform. V_{DD} = V_{IN} = 3.3V, R_{LOAD} = 20Ω, No C_{OUT}, C_{SLEW} = 3.9nF

2. Overtemperature Protection

The AP220309 features overtemperature protection. If the internal junction temperature of the AP220309 reaches +125°C, such as during an overcurrent event, the FET is shut off completely so the die can cool. Once the die temperature reaches approximately +100°C, overtemperature protection will be disabled and the FET will again be capable of conducting. This event will repeat for as long as the condition which causes the die to overheat exists.

3. Current-Limiting Operation

3A Active Current-Limiting Mode (With Overtemperature Protection)

In the event the current delivered from the VIN to VOUT in the AP220309 exceeds the I_{ACL} maximum current limit in the *Electrical Characteristics* table for more than a few microseconds, the AP220309 will limit the current to the I_{ACL} threshold by increasing the FET resistance. If this current is sustained, the device will overheat and trigger overtemperature protection.

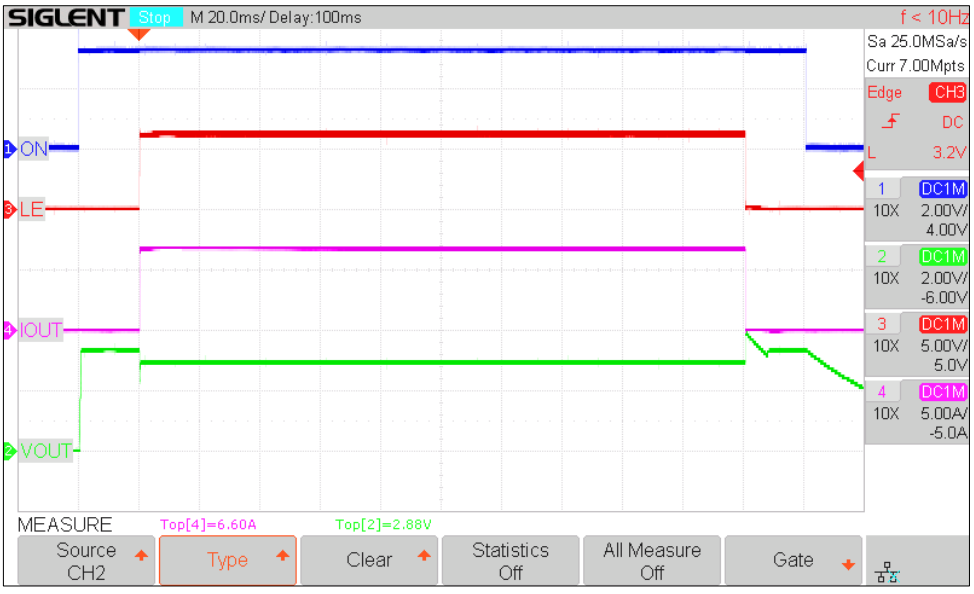


Figure 10. AP220309 ACL Operation Waveform. V_{DD} = V_{IN} = 3.3V, R_{LOAD} = 20Ω, C_{OUT} = 10µF, C_{SLEW} = 3.9nF. *Load Enable* signal applies additional 0.4Ω of load.

Application Information (continued)

3B Short-Circuit Current-Limiting Mode (With Overtemperature Protection)

The AP220309 also contains a short-circuit current limit, which will be triggered if V_{OUT} is externally limited to 300mV or less due to an improper solder connection or similar defect on the same node as the VOUT pin. During this event, the AP220309 will maintain the resistivity of the FET to limit the output current of the device to a typical value of 0.5A.

If the short-circuit event is resolved the AP220309 will continue its voltage ramp per the slew rate set by the capacitor on the CAP pin.

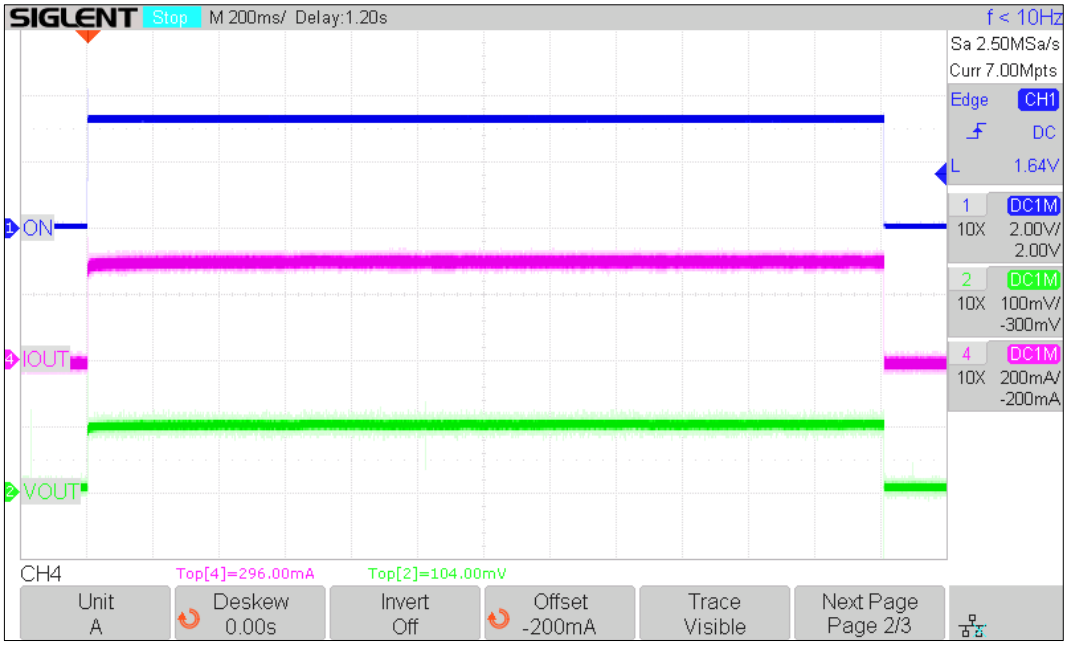


Figure 11. AP220309 SCL Operation Waveform. V_{DD} = V_{IN} = 3.3V, R_{LOAD} = 0.3Ω, C_{OUT} = 10µF, C_{SLEW} = 3.9nF

Note: Depending upon factors such as V_{IN}, the shorted value of V_{OUT}, and ambient temperature, the AP220309 may or may not dissipate enough power to trigger the overtemperature protection within the circuit. If the overtemperature protection occurs, the part will shut down and retry per the overtemperature detection description above.

Recommended Layout

It is important to have a proper PCB layout for high-performance device operation. The list below provides some basic rules for the PCB layout.

- Connect a 0.1μF capacitor from VDD pin to GND. It should be placed as close to the device as possible.
- Place high-quality low-ESR input C_{IN} (10μF min) and output C_{OUT} capacitors close to the device VIN and VOUT pins to minimize the effects of parasitic inductance.
- Make sure to have a solid Ground connection.
- All traces should be as short, wide, and direct as possible.
- VIN and VOUT pins have the most heat dissipation during high-current operations. Use polygon planes and/or 2oz. copper for VIN and VOUT connections.

The example below illustrates the described layout guidelines.

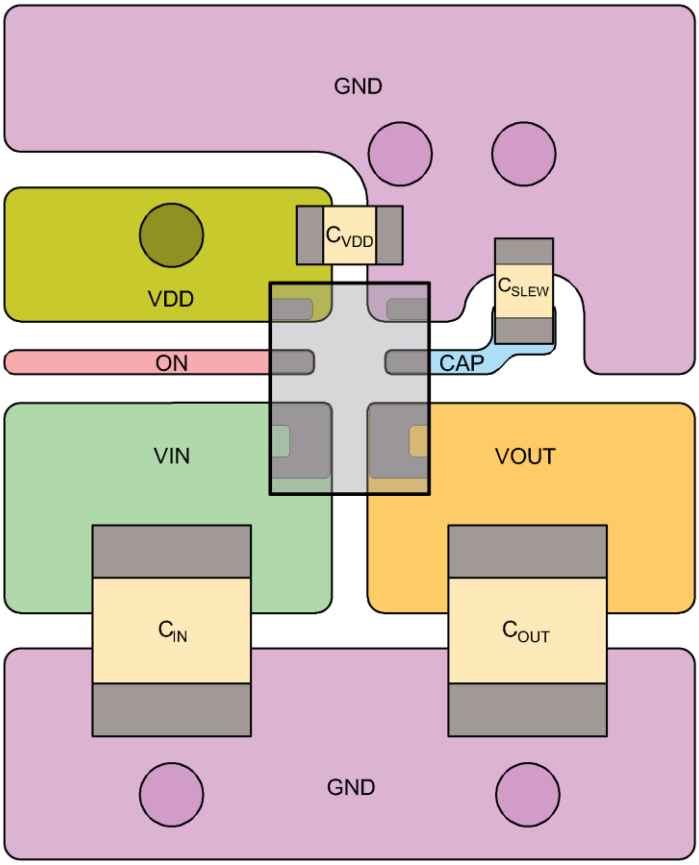
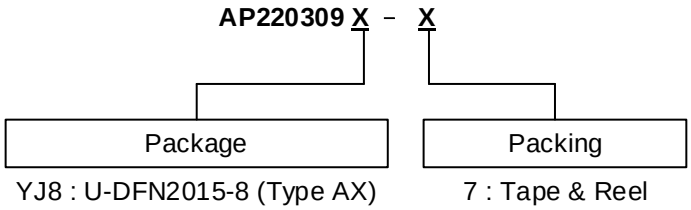


Figure 12. AP220309 Recommended Layout

Ordering Information

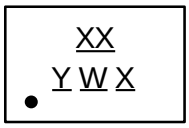


Orderable Part Number	Package	Package Code	Packing	
			Qty.	Carrier
AP220309YJ8-7	U-DFN2015-8 (Type AX)	YJ8	3,000	7" Tape and Reel

Marking Information

U-DFN2015-8 (Type AX)

(Top View)



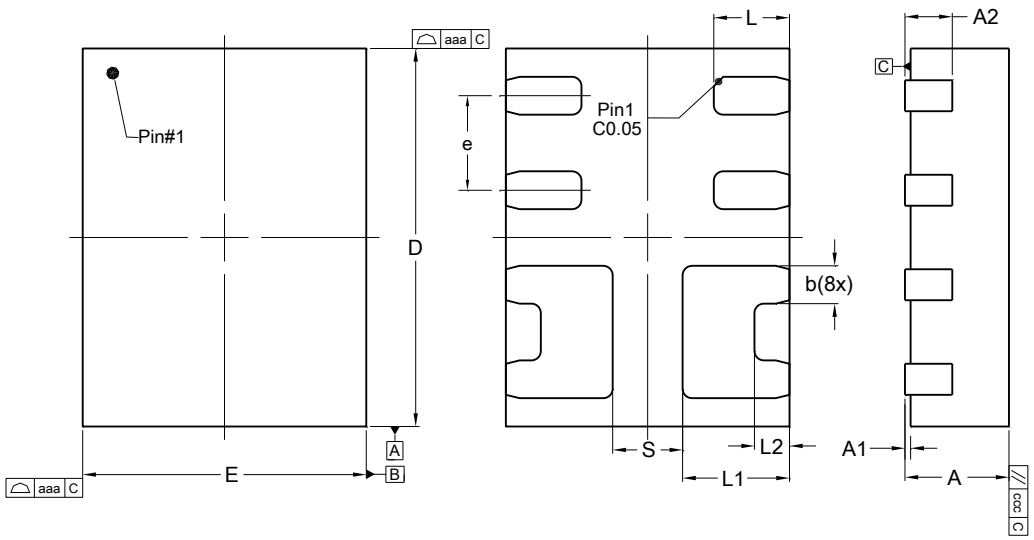
XX : Identification Code
Y : Year : 0 to 9 (ex: 5 = 2025)
W : Week : A to Z : week 1 to 26;
a to z : week 27 to 52; z represents week 52 and 53
X : Internal Code

Orderable Part Number	Package	Identification Code
AP220309YJ8-7	U-DFN2015-8 (Type AX)	D4

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2015-8 (Type AX)

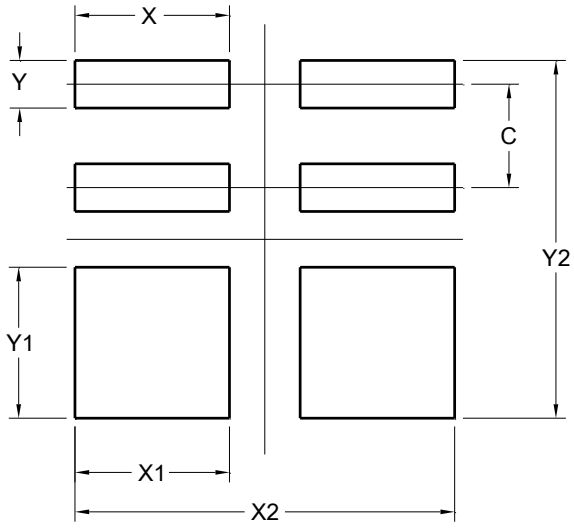


U-DFN2015-8 (Type AX)			
Dim	**Min**	**Max**	**Typ**
A	0.500	0.600	0.550
A1	-0.005	0.030	--
A2	0.225	0.275	0.250
b	0.175	0.225	0.200
D	1.95	2.05	2.00
E	1.45	1.55	1.50
e	0.500 BSC		
L	0.375	0.425	0.400
L1	0.515	0.615	0.565
L2	0.135	0.235	0.185
S	--	--	0.370
aaa	0.05		
ccc	0.05		
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2015-8 (Type AX)



Dimensions	Value (in mm)
C	0.500
X	0.580
X1	0.745
X2	1.830
Y	0.230
Y1	0.730
Y2	1.730

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu. Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.0059 grams (Approximate)

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