

3A DDR TERMINATION REGULATOR

AP2302

General Description

The AP2302 linear regulator is designed to meet the JEDEC specification SSTL-2 and SSTL-18 for termination of DDR-SDRAM. The regulator can sink or source up to 3A current continuously, offers enough current for most DDR applications. Output voltage is designed to track the reference voltage within a 2% (DDR I) and 3% (DDR II) tolerance for load regulation while preventing shooting through on the output stage. On-chip thermal limiting provides protection against a combination of high current and ambient temperature which would create an excessive junction temperature.

The AP2302, used in conjunction with series termination resistors, provides an excellent voltage source for active termination schemes of high speed transmission lines as those seen in high speed memory buses and distributed backplane designs.

The AP2302 is available in SOIC-8, TO-252-5L and TO-263-5L packages.

Features

- Support Both DDR I ($1.25V_{TT}$) and DDR II ($0.9V_{TT}$) Requirements
- Source and Sink Current up to 3A
- High Accuracy Output Voltage at Full-load
- Adjustable V_{OUT} by External Resistors
- Shutdown for Standby or Suspend Mode Operation with High-impedance Output

Applications

- DDR-SDRAM Termination
- DDR-II Termination
- SSTL-2 Termination

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Figure 1. Package Types of AP2302

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Pin Configuration

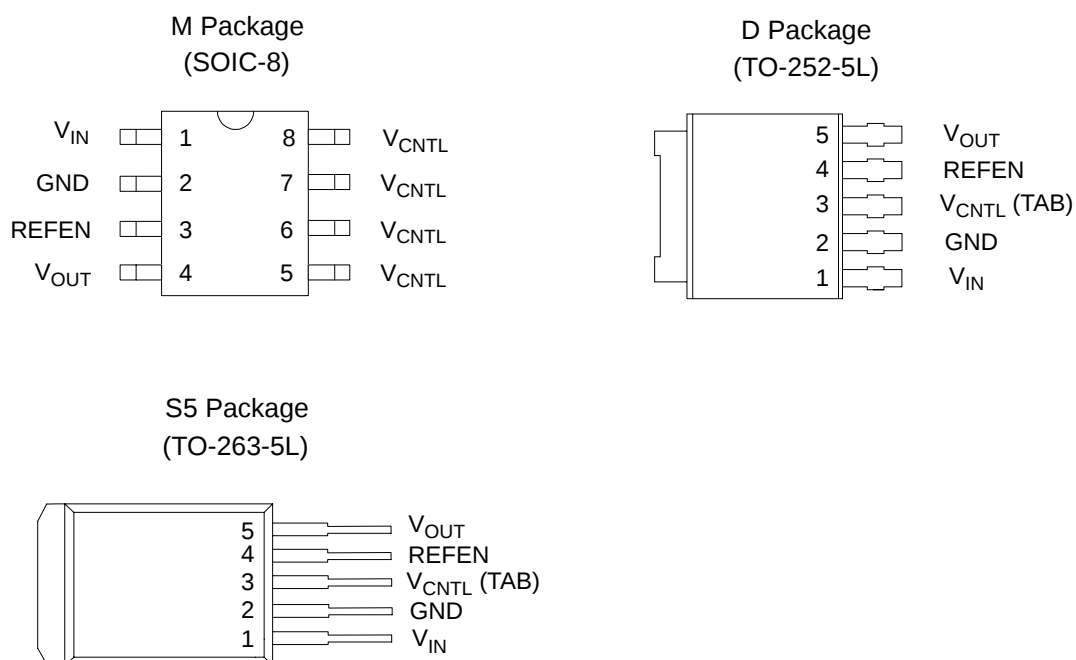


Figure 2. Pin Configuration of AP2302 (Top View)

Pin Description

Pin Number			Pin Name	Function
SOIC-8	TO-252-5L	TO-263-5L		
1	1	1	V_{IN}	Power Input
2	2	2	GND	Ground
3	4	4	REFEN	Reference Voltage Input and Chip Enable
4	5	5	V_{OUT}	Output Voltage
5, 6, 7, 8	3	3	V_{CNTL}	Supply Voltage for Internal Circuit (Internally Connected for SOIC-8), (TAB for TO-252-5L and TO-263-5L)



The block diagram illustrates the internal structure of the DC-DC converter, enclosed in a dashed box. The central component is the **OUTPUT CONTROL** block. It is connected to several functional blocks: **CURRENT LIMIT**, **BANDGAP**, **START UP**, and **THERMAL PROTECT**. The **OUTPUT CONTROL** block is also connected to the **V_{CNTL}** pin (pin 3 for 5-pin, pins 6, 7, 8 for 8-pin) and the **V_{IN}** pin (pin 1). The **OUTPUT CONTROL** block drives two MOSFETs, labeled **A(B)** (A for 5-pin, B for 8-pin), which are connected to the **V_{OUT}** pin (pin 5 for 4) and the **GND** pin (pin 2). The **REFEN** pin (pin 4 for 3) is connected to the **BANDGAP** block and the **START UP** block. The **THERMAL PROTECT** block is connected to the **OUTPUT CONTROL** block and the **GND** pin.

Figure 3. Functional Block Diagram of AP2302

AP2302 □ □ - □

Circuit Type ————— E1: Lead Free
Blank: Tin Lead

Package ————— TR: Tape and Reel
Blank: Tube

M: SOIC-8

D: TO-252-5L

S5: TO-263-5L

Package	Temperature Range	Part Number		Marking ID		Packing Type
		Tin Lead	Lead Free	Tin Lead	Lead Free	
SOIC-8	0 to 125°C	AP2302M	AP2302M-E1	2302M	2302M-E1	Tube
		AP2302MTR	AP2302MTR-E1	2302M	2302M-E1	Tape & Reel
TO-252-5L	0 to 125°C	AP2302D	AP2302D-E1	AP2302D	AP2302D-E1	Tube
		AP2302DTR	AP2302DTR-E1	AP2302D	AP2302D-E1	Tape & Reel
TO-263-5L	0 to 125°C	AP2302S5	AP2302S5-E1	AP2302S5	AP2302S5-E1	Tube
		AP2302S5TR	AP2302S5TR-E1	AP2302S5	AP2302S5-E1	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "E1" suffix in the part number, are RoHS compliant.

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Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Value		Unit
Supply Voltage for Internal Circuit	V_{CNTL}	7		V
Power Dissipation	P_D	Internally Limited		W
ESD (Human Body Model)	ESD	2		KV
Junction Temperature	T_J	150		°C
Storage Temperature Range	T_{STG}	-65 to 150		°C
Lead Temperature (Soldering, 10sec)	T_{LEAD}	260		°C
Package Thermal Resistance (Free Air)	θ_{JA}	SOIC-8	160	°C/W
		TO-252-5L	130	
		TO-263-5L	90	

Note 1: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage for Internal Circuit		V_{CNTL} (Note 2, 3)		3.3	6	V
Power Input	DDR I	V_{IN}	1.6	2.5	V_{CNTL}	V
	DDR II			1.8		
Junction Temperature		T_J	0		125	°C

Note 2: Keep $V_{CNTL} \geq V_{IN}$ in power on and power off sequences.

Note 3: For safe operation, V_{CNTL} MUST be tied to 3.3V rather than 5V.

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Electrical Characteristics

($T_J=25^{\circ}\text{C}$, $V_{IN}=2.5\text{V}$, $V_{CNTL}=3.3\text{V}$, $V_{REFEN}=1.25\text{V}$, $C_{OUT}=10\mu\text{F}$ (Ceramic), unless otherwise specified.)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Output Offset Voltage		V _{OS}	I _L =0A (Note 4)	-20	0	20	mV
Load Regulation	DDR I	ΔV _{OUT} / V _{OUT}	I _L =0 to 1.5A		0.8	2	%
			I _L =0 to -1.5A		0.8	2	
	DDR II		I _L =0 to 1.5A		1.2	3	
			I _L =0 to -1.5A		1.2	3	
Quiescent Current of V _{CNTL}		I _Q	No Load		3	5	mA
Leakage Current in Shutdown Mode		I _{SHDN}	V _{REFEN} <0.2V, R _L =180Ω		3	6	μA
Protection							
Current Limit		I _{LIMIT}		3			A
Thermal Shutdown Temperature		T _{SHDN}	3.3V≤V _{CNTL} ≤5V		150		°C
Thermal Shutdown Hysteresis					50		°C
Shutdown Function							
Shutdown Threshold Trigger			Output=High	0.8			V
			Output=Low			0.2	

Note 4: V_{OS} is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN} .

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Typical Performance Characteristics

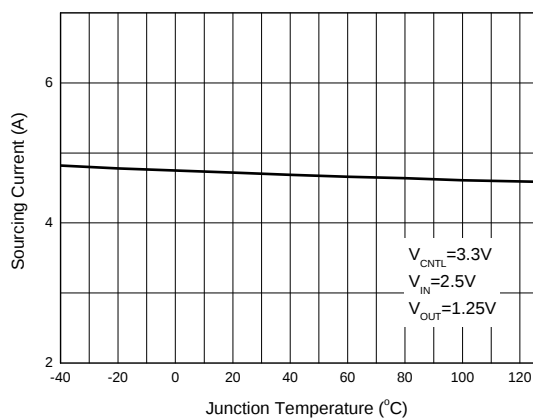


Figure 4. Sourcing Current vs. Junction Temperature

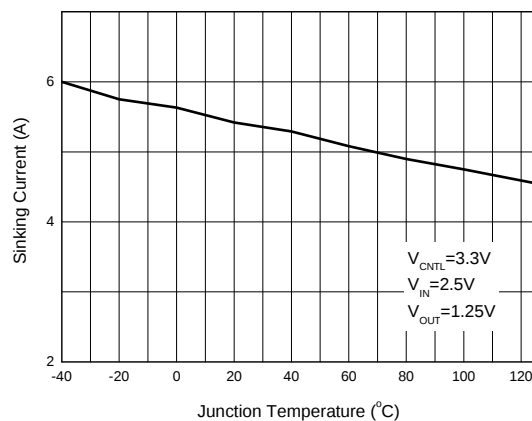


Figure 5. Sinking Current vs. Junction Temperature

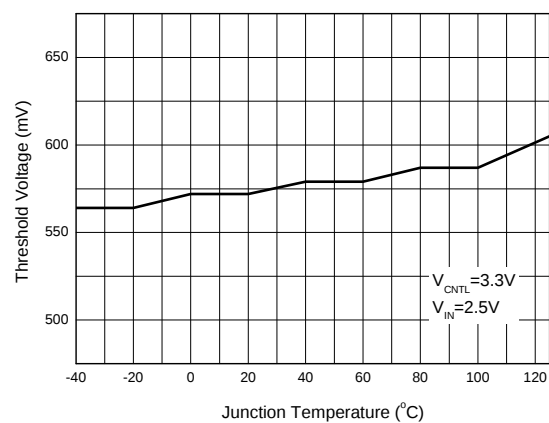


Figure 6. Threshold Voltage vs. Junction Temperature

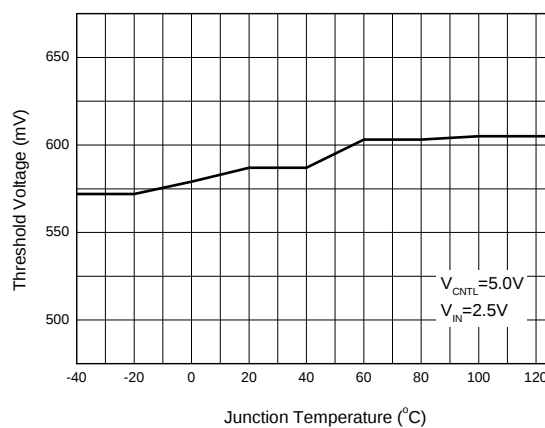


Figure 7. Threshold Voltage vs. Junction Temperature

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Typical Performance Characteristics (Continued)

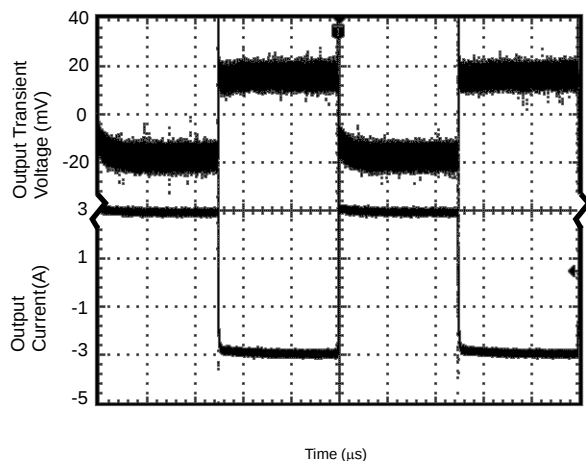


Figure 8. 0.9V_{TT} at 3A Transient Response
(Conditions: V_{IN}=2.5V, V_{CNTL}=3.3V, C_{OUT}=10μF)

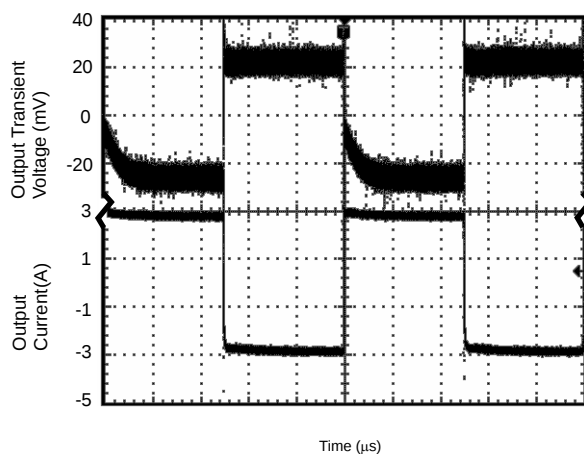


Figure 9. 1.25V_{TT} at 3A Transient Response
(Conditions: V_{IN}=2.5V, V_{CNTL}=3.3V, C_{OUT}=10μF)

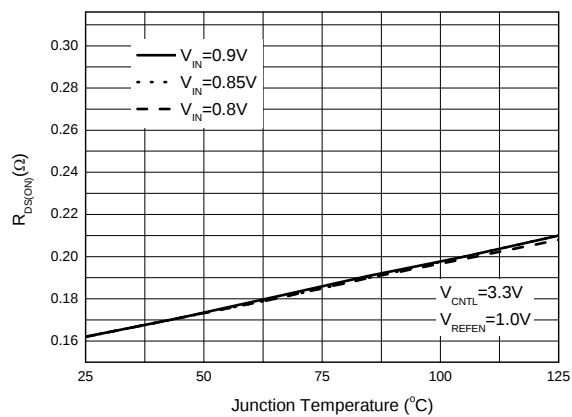


Figure 10. R_{DS(on)} vs. Junction Temperature

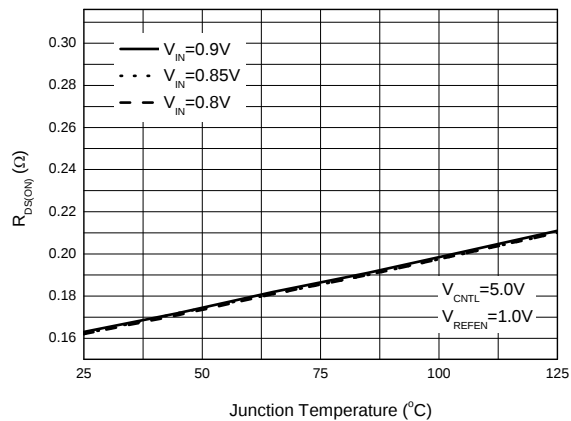


Figure 11. R_{DS(on)} vs. Junction Temperature

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Typical Performance Characteristics (Continued)

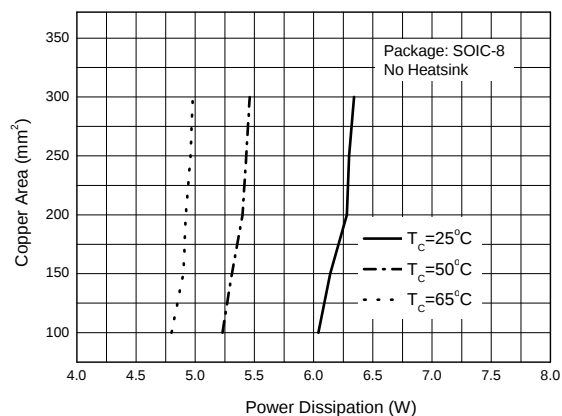


Figure 12. Copper Area vs. Power Dissipation

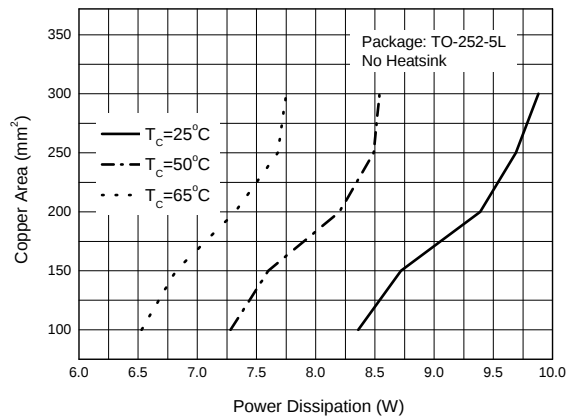


Figure 13. Copper Area vs. Power Dissipation

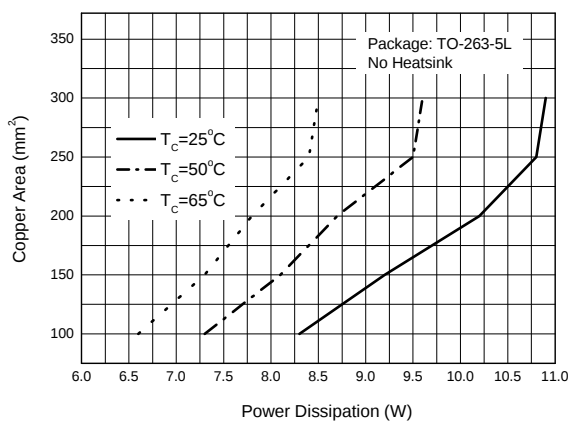


Figure 14. Copper Area vs. Power Dissipation

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Typical Application

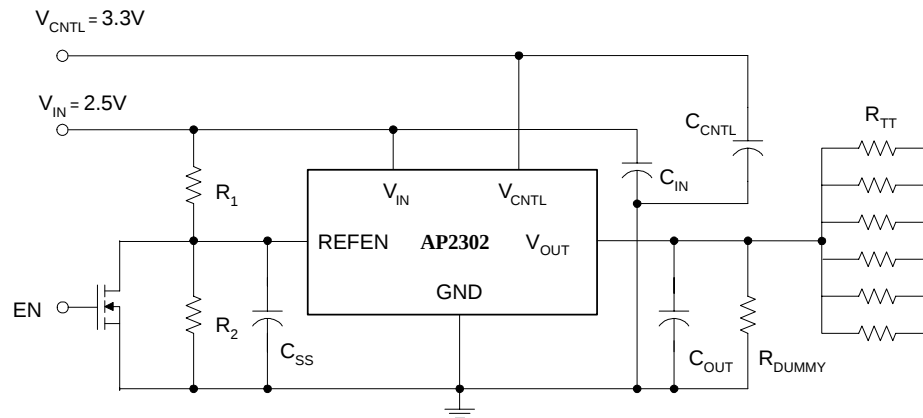
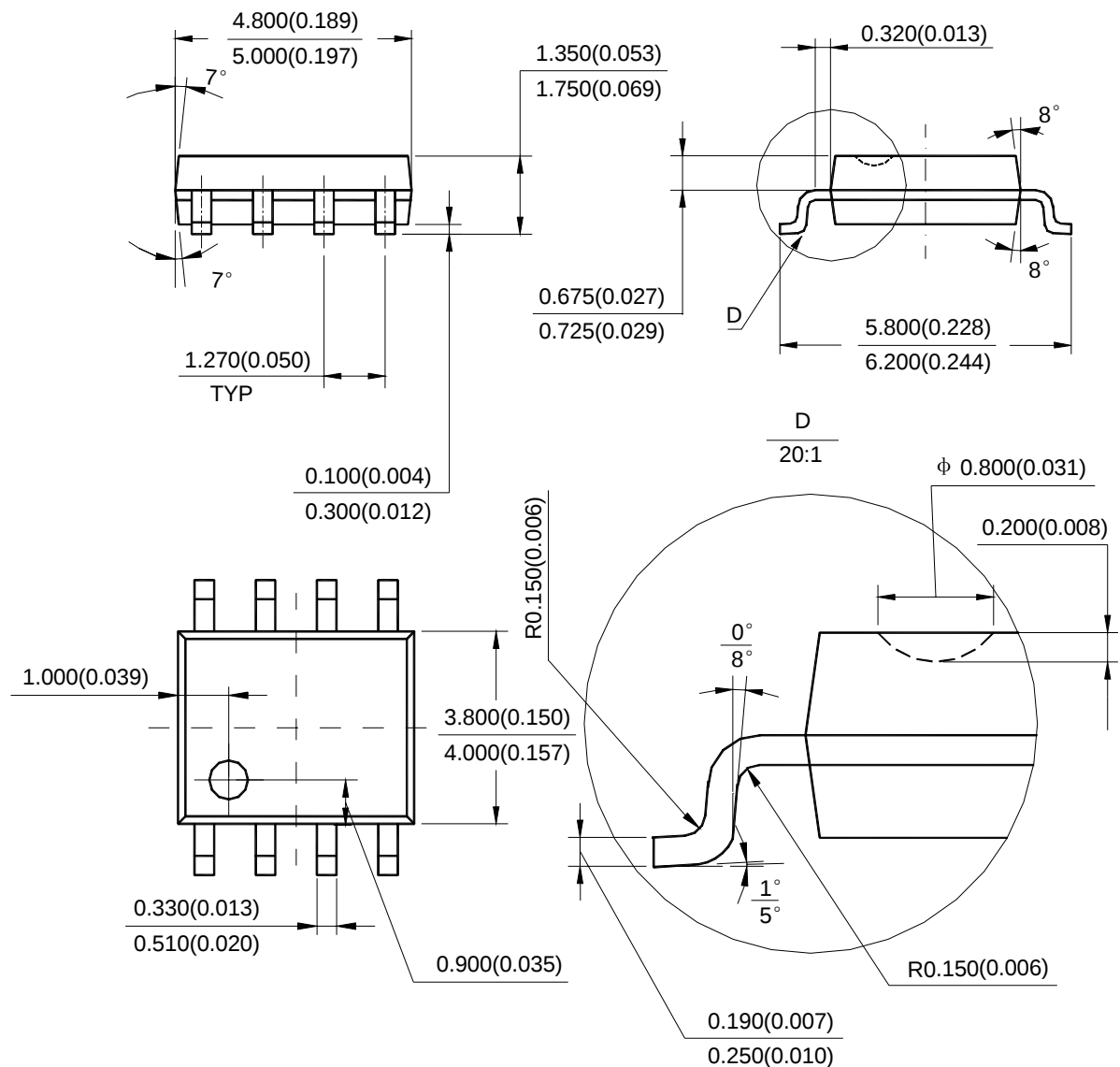


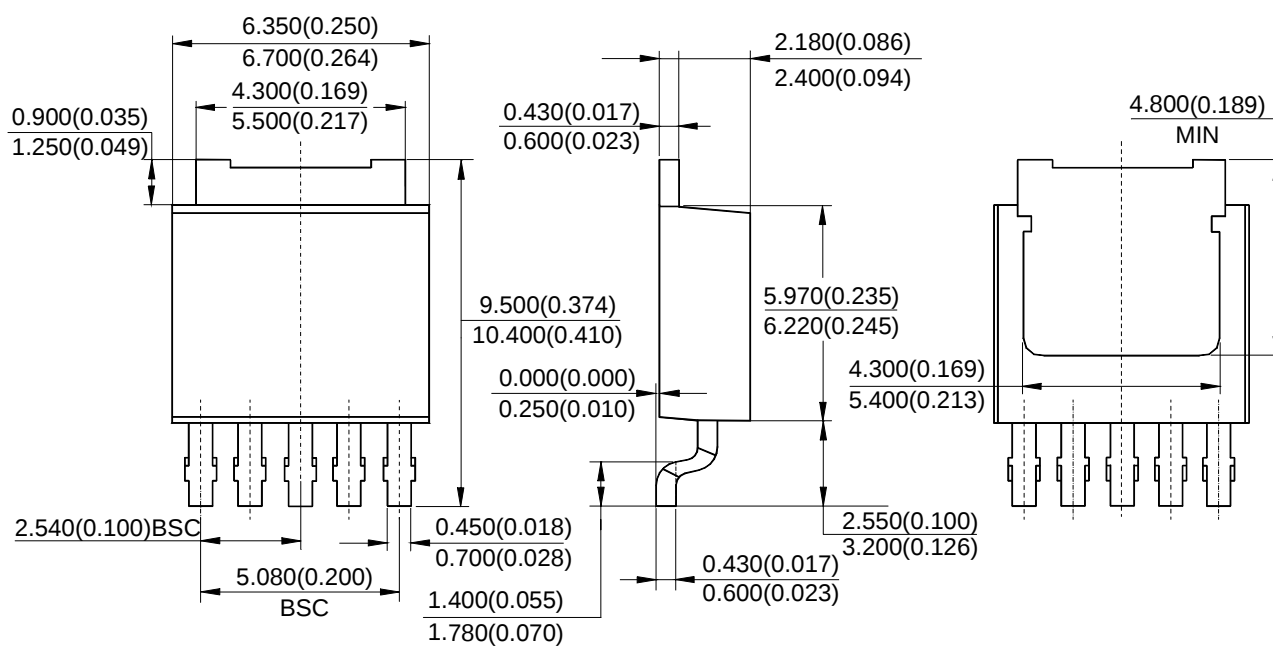
Figure 15. Typical Application of AP2302

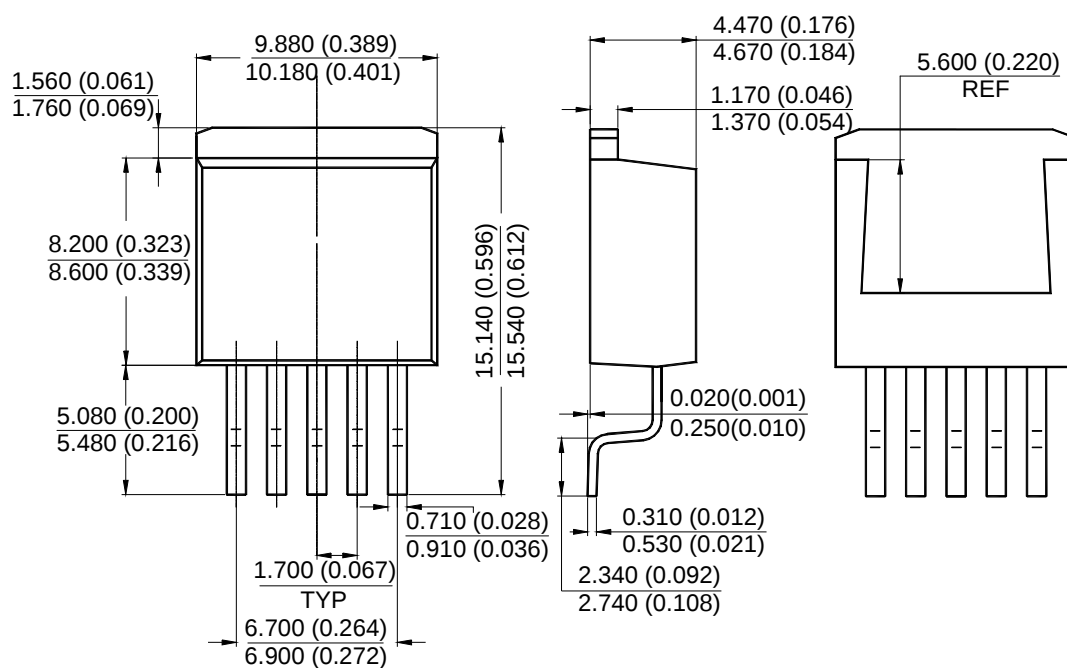
$R_1=R_2=100\text{K}\Omega$, $R_{TT}=50\Omega / 33\Omega / 25\Omega$

$R_{DUMMY}=1\text{K}\Omega$, as for V_{OUT} discharge when V_{IN} is not present but V_{CNTL} is present

$C_{SS}=1\mu\text{F}$, $C_{IN}=470\mu\text{F}$, $C_{CNTL}=47\mu\text{F}$, $C_{OUT}=470\mu\text{F}$

**3A DDR TERMINATION REGULATOR****AP2302****Mechanical Dimensions****SOIC-8****Unit: mm(inch)**

**3A DDR TERMINATION REGULATOR****AP2302****Mechanical Dimensions (Continued)****TO-252-5L****Unit: mm(inch)**

**3A DDR TERMINATION REGULATOR****AP2302****Mechanical Dimensions (Continued)****TO-263-5L****Unit: mm(inch)**



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MAIN SITE

BCD Semiconductor Manufacturing Limited

- Wafer Fab

Shanghai SIM-BCD Semiconductor Manufacturing Limited

800, Yi Shan Road, Shanghai 200233, China

Tel: +86-21-6485 1491, Fax: +86-21-5450 0008

BCD Semiconductor Manufacturing Limited

- IC Design Group

Advanced Analog Circuits (Shanghai) Corporation

8F, Zone B, 900, Yi Shan Road, Shanghai 200233, China

Tel: +86-21-6495 9539, Fax: +86-21-6485 9673

REGIONAL SALES OFFICE

Shenzhen Office

Shanghai SIM-BCD Semiconductor Manufacturing Co., Ltd. Shenzhen Office

Advanced Analog Circuits (Shanghai) Corporation Shenzhen Office

27B, Tower C, 2070, Middle Shen Nan Road, Shenzhen 518031, China

Tel: +86-755-8368 3987, Fax: +86-755-8368 3166

Taiwan Office

BCD Semiconductor (Taiwan) Company Limited

4F, 298-1, Rui Guang Road, Nei-Hu District, Taipei,

Taiwan

Tel: +886-2-2656 2808, Fax: +886-2-2656 2806

USA Office

BCD Semiconductor Corporation

3170 De La Cruz Blvd., Suite 105, Santa Clara,

CA 95054-2411, U.S.A

Tel: +1-408-988 6388, Fax: +1-408-988 6386