

-20V P-Channel Enhancement Mode MOSFET

Description

The AP2305CI uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = -20V$ $I_D = -6.0A$

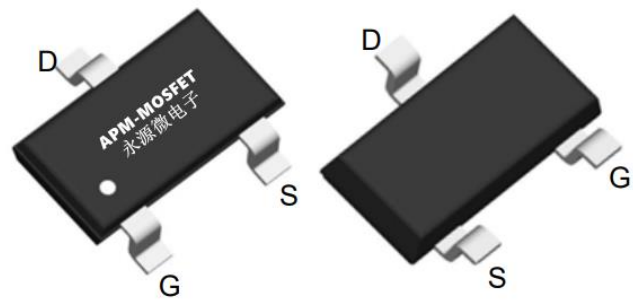
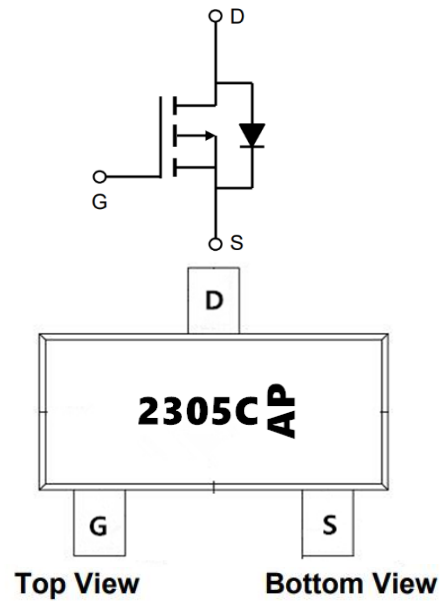
$R_{DS(ON)} < 40m\Omega$ @ $V_{GS} = -4.5V$ (Type: **33mΩ**)

Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP2305CI	SOT23L	2305C-AP	3000

Absolute Maximum Ratings ($T_c = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-Source Voltage	± 12	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V^1$	-6.0	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V^1$	-4.5	A
I_{DM}	Pulsed Drain Current ²	-18	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation ³	3.81	W
$P_D @ T_A = 70^\circ C$	Total Power Dissipation ³	0.74	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	125	$^\circ C/W$
$R_{\theta JC}$	Thermal resistance, junction-case	6.8	$^\circ C/W$

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Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	I _D = -250μA, V _{GS} = 0V	-20	-	-	V
IDSS	Zero Gate Voltage Drain Current	V _{DS} = -20V, V _{GS} = 0V	-	-	1.0	μA
IGSS	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-0.5	-0.6	-1.0	V
RDS(ON)	Static Drain-Source ON-Resistance ⁽³⁾	V _{GS} = -4.5V, I _D = -4A	-	33	40	mΩ
		V _{GS} = -2.5V, I _D = -3A	-	40	66	mΩ
Ciss	Input Capacitance	V _{GS} = 0V, V _{DS} = -10V, f = 1MHz	-	534	-	pF
Coss	Output Capacitance		-	62	-	pF
Crss	Reverse Transfer Capacitance		-	50	-	pF
Q _g	Total Gate Charge	V _{GS} = 0 to -4.5V V _{DS} = -10V, I _D = -2A	-	5.6	-	nC
Q _{gs}	Gate Source Charge		-	1	-	nC
Q _{gd}	Gate Drain("Miller") Charge		-	1	-	nC
td(on)	Turn-On DelayTime	V _{GS} = -4.5V, V _{DD} = -10V I _D = -2A, R _{GEN} = 3Ω	-	5	-	ns
t _r	Turn-On Rise Time		-	21	-	ns
td(off)	Turn-Off DelayTime		-	110	-	ns
t _f	Turn-Off Fall Time		-	239	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-3	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-12	A
VSD	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _S = -4.2A	-	-	-1.2	V
trr	Body Diode Reverse Recovery Time	I _F = -2A, di/dt = 100A/us	-	64	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	10	-	nC

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width Δ 300us , duty cycle Δ 2%
- 3、 The power dissipation is limited by 150°C junction temperature
- 4、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

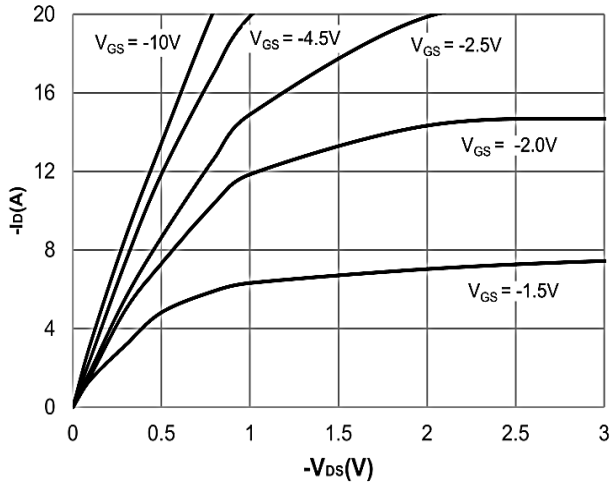


Figure 1: Output Characteristics

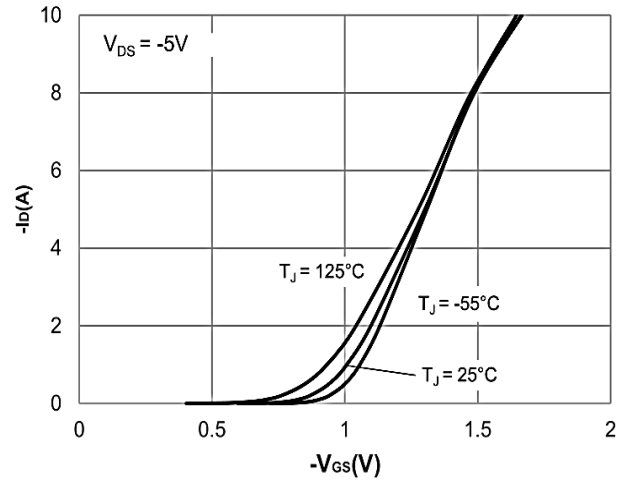


Figure 2: Typical Transfer Characteristics

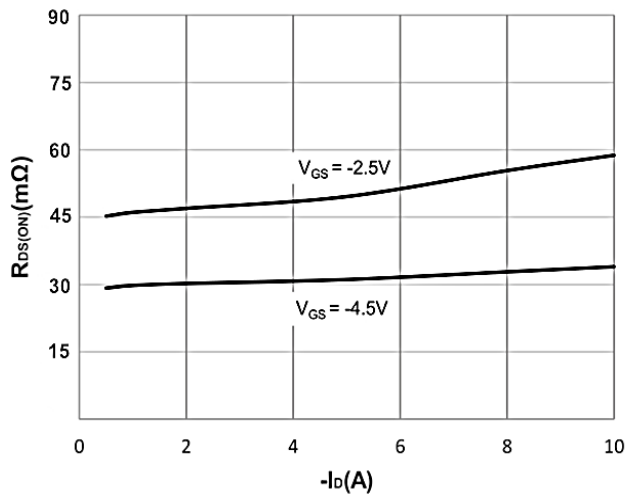


Figure 3: On-resistance vs. Drain Current

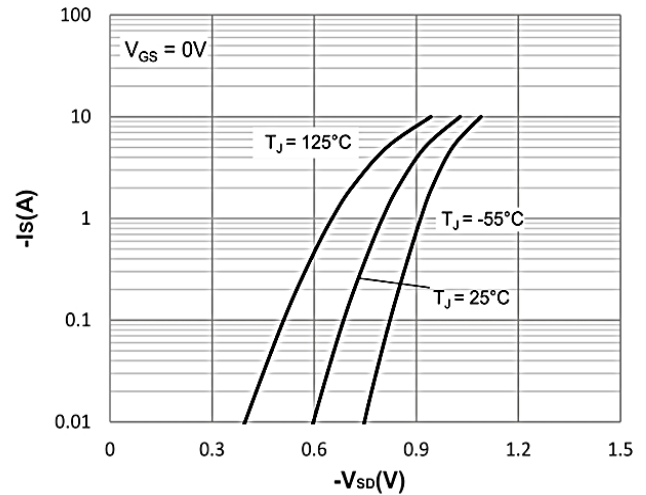


Figure 4: Body Diode Characteristics

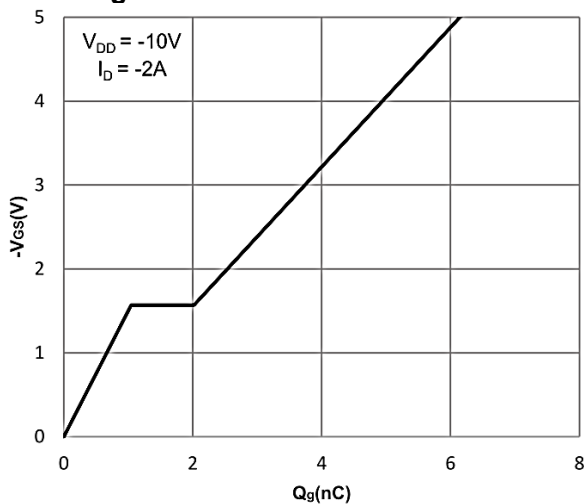


Figure 5: Gate Charge Characteristics

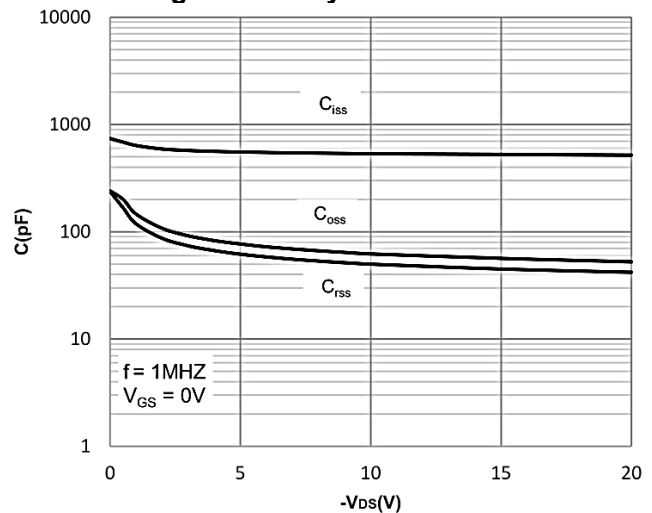


Figure 6: Capacitance Characteristics

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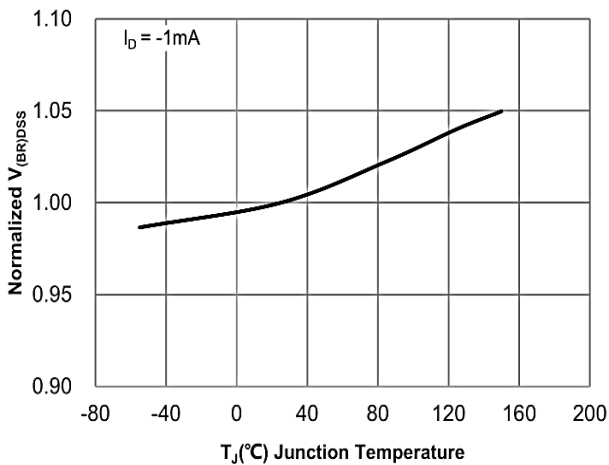


Figure 7: Normalized Breakdown voltage vs.

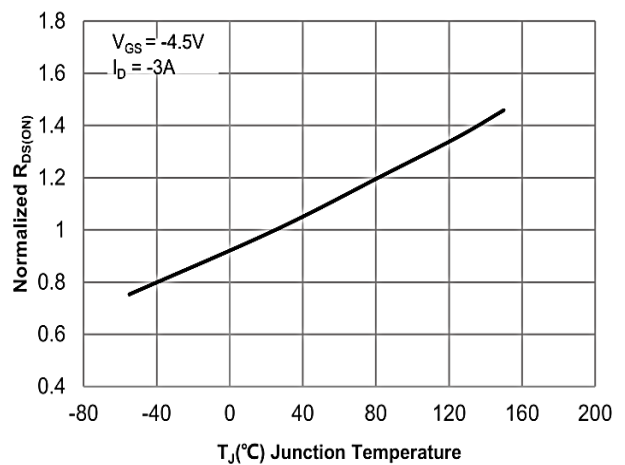


Figure 8: Normalized on Resistance vs.

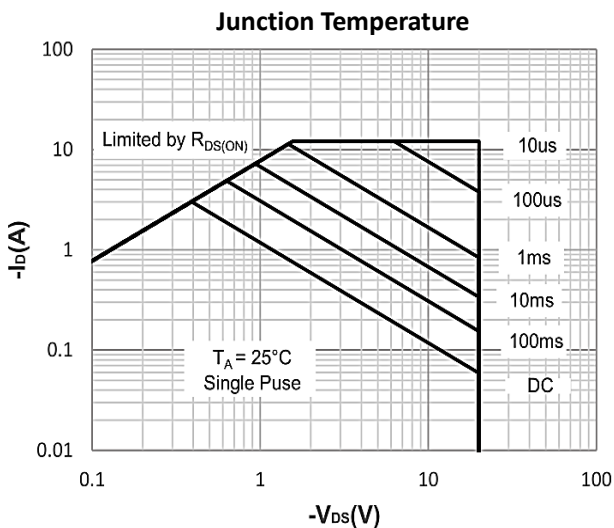


Figure 9: Maximum Safe Operating Area

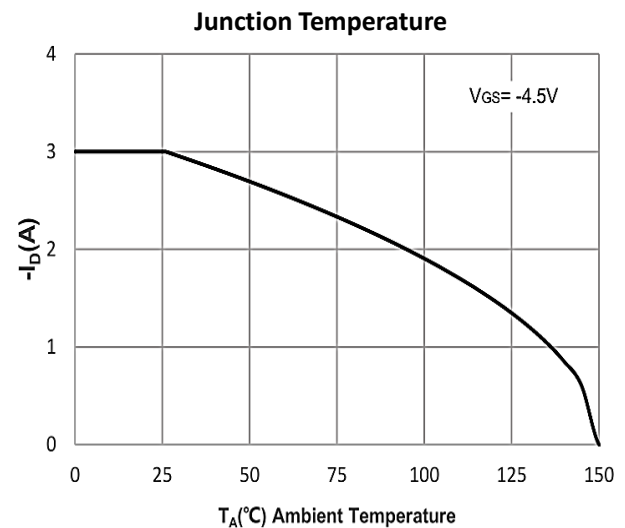


Figure 10: Maximum Continuous Drian Current

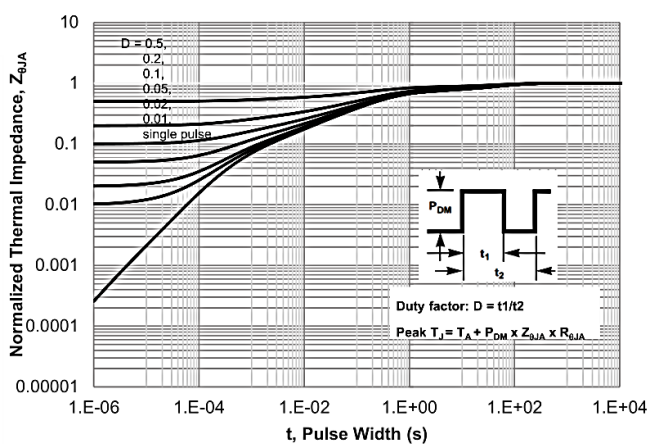


Figure 11: Normalized Maximum Transient Thermal Impedance

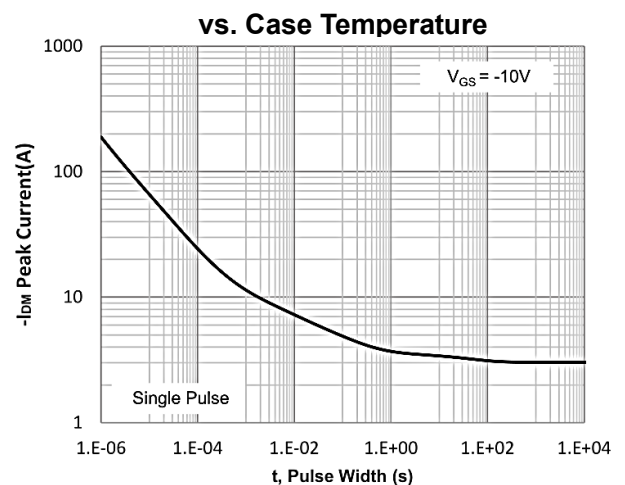
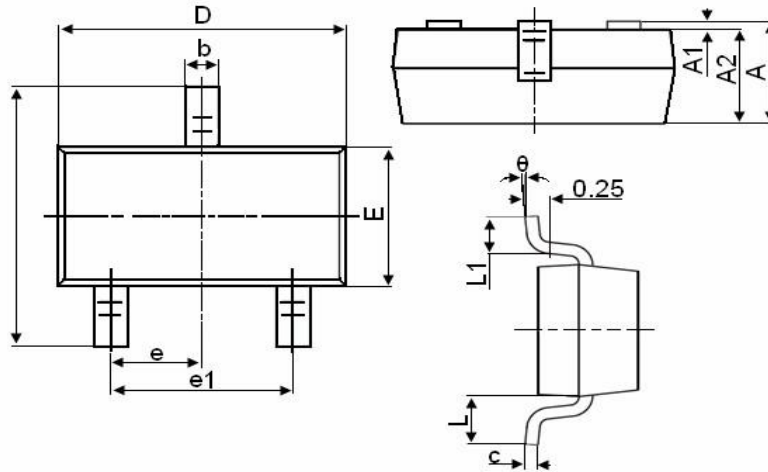


Figure 12: Peak Current Capacity

Package Mechanical Data-SOT23-XC-Single



Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
θ	0°	8°

-20V P-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
Rve1.0	2023/4/31	Initial release

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